



JEPPIAAR
INSTITUTE OF TECHNOLOGY
“Self-Belief | Self Discipline | Self Respect”



QUESTION BANK

Regulation : 2017

Year/Semester : II

Semester : 03

Batch : 2018-2022

**DEPARTMENT OF ELECTRONICS &
COMMUNICATION ENGINEERING**

Vision of the Institution:

Jeppiaar Institute of Technology aspires to provide technical education in futuristic technologies with the perspective of innovative, industrial and social application for the betterment of humanity.

Mission of the Institution:

- To produce competent and disciplined high-quality professionals with the practical skills necessary to excel as innovative professionals and entrepreneurs for the benefit of the society.
- To improve the quality of education through excellence in teaching and learning, research, leadership and by promoting the principles of scientific analysis, and creative thinking.
- To provide excellent infrastructure, serene and stimulating environment that is most conducive to learning.
- To strive for productive partnership between the Industry and the Institute for research and development in the emerging fields and creating opportunities for employability.
- To serve the global community by instilling ethics, values and life skills among the students needed to enrich their lives.

Department Vision

To enhance and impart futuristic and innovative technological education for the excellence of Electronics and Communication Engineering with new ideas and innovation to meet industrial expectation and social needs with ethical and global awareness reinforced by an efficiency through research platform for the advancement of humanity.

Department Mission

M1: To produce competent and high quality professional Engineers in the field of Electronics and Communication Engineering for the benefit of the society globally.

M2: To provide a conducive infrastructure and environment for faculty and students with enhanced laboratories, to create high quality professionals

M3: To provide Prerequisite Skills in multidisciplinary areas for the needs of Industries, higher education and research establishments and entrepreneurship

M4: To handle Socio Economic Challenges of Society by Imparting Human Values and Ethical Responsibilities.

PEO's of the Department:

PEO 1: Graduate Engineers will have knowledge and skills required for employment and an advantage platform for lifelong learning process.

PEO 2: Graduate Engineers will be provided with futuristic education along with the perspective research and application based on global requirements.

PEO 3: Graduate Engineers will have effective communication skills and work in multidisciplinary team.

PEO 4: Graduate Engineers will develop entrepreneurship skills and practice the profession with integrity, leadership, ethics and social responsibility.

Program Specific Outcomes (PSO's):

PSO 1 : Ability to develop and utilize novel, compact and power efficient coherent theoretical and practical methodologies in the field of analog and digital electronics.

PSO 2: Ability to implement analog, digital and hybrid communication Protocol to aspect the challenges in the field of Telecommunication and Networking.

BLOOM'S TAXONOMY

Definition:

Bloom's taxonomy is a classification system used to define and distinguish different levels of human cognition like thinking, learning, and understanding.

Objectives:

- To classify educational learning objectives into levels of complexity and specificity. The classification covers the learning objectives in cognitive, affective and sensory domains.
- To structure curriculum learning objectives, assessments and activities.

Levels in Bloom's Taxonomy:

- **BTL 1 – Remember** - The learner recalls, restate and remember the learned information.
- **BTL 2 – Understand** - The learner embraces the meaning of the information by interpreting and translating what has been learned.
- **BTL 3 – Apply** - The learner makes use of the information in a context similar to the one in which it was learned.
- **BTL 4 – Analyze** - The learner breaks the learned information into its parts to understand the information better.
- **BTL 5 – Evaluate** - The learner makes decisions based on in-depth reflection, criticism and assessment.
- **BTL 6 – Create** - The learner creates new ideas and information using what has been previously learned.

TABLE OF CONTENT

MA8352 -Linear Algebra and Partial Differential Equations		
Unit No.	Topic	Page No.
	Syllabus	1.1
I	Vector Spaces	1.3
II	Linear Transformation and Diagonalization	1.11
III	Inner Product Spaces	1.18
IV	Partial Differential Equations	1.27
V	Fourier Series Solutions of Partial Differential Equations	1.34
EC8393-Fundamentals of Data Structures In C		
	Syllabus	2.1
I	C Programming Basics	2.2
II	Functions, Pointers, Structures and Unions	2.9
III	Linear Data Structures	2.27
IV	Non-Linear Data Structures	2.48
V	Searching and Sorting Algorithms	2.76
EC8351- Electronic Circuits- I		
	Syllabus	3.1
I	Biasing of Discrete BJT, JFET and MOSFET	3.3
II	BJT Amplifiers	3.14
III	Single Stage FET, MOSFET amplifiers	3.24
IV	Frequency Response of Amplifiers	3.35
V	Power Supplies and Electronic Device testing	3.49
EC8352 - Signals and Systems		
	Syllabus	4.1
I	Classification of Signals and Systems	4.2
II	Analysis of Continuous Time Signals	4.29
III	Linear Time Invariant Continuous Time Systems	4.52
IV	Analysis of Discrete Time Signals	4.76
V	Linear Time Invariant-Discrete Time Systems	4.103
EC8392 - Digital Electronics		
	Syllabus	5.1
I	Digital Fundamentals	5.3
II	Combinational Circuit Design	5.11
III	Synchronous Sequential Circuits	5.19
IV	Asynchronous Sequential Circuits	5.27
V	Memory Devices and Digital Integrated Circuits	5.31

EC8391 - Control Systems Engineering		
	Syllabus	6.1
I	Systems components and their representation	6.2
II	Time Response Analysis	6.18
III	Frequency Response and System analysis	6.30
IV	Concepts of Stability Analysis	6.39
V	Control System Analysis using State Variable methods	6.51

MA8352

**LINEAR ALGEBRA AND PARTIAL
DIFFERENTIAL EQUATIONS**

L T P C

4 0 0 4

OBJECTIVES:

- To introduce the basic notions of groups, rings, fields which will then be used to solve related problems.
- To understand the concepts of vector space, linear transformations and diagonalization.
- To apply the concept of inner product spaces in orthogonalization.
- To understand the procedure to solve partial differential equations.
- To give an integrated approach to number theory and abstract algebra, and provide a firm basis for further reading and study in the subject.

UNIT I**VECTOR SPACES****12**

Vector spaces – Subspaces – Linear combinations and linear system of equations – Linear independence and linear dependence – Bases and dimensions.

UNIT II**LINEAR TRANSFORMATION AND DIAGONALIZATION****12**

Linear transformation - Null spaces and ranges - Dimension theorem - Matrix representation of a linear transformations - Eigenvalues and eigenvectors - Diagonalizability.

UNIT III**INNER PRODUCT SPACES****12**

Inner product, norms - Gram Schmidt orthogonalization process - Adjoint of linear operations - Least square approximation.

UNIT IV**PARTIAL DIFFERENTIAL EQUATIONS****12**

Formation – Solutions of first order equations – Standard types and equations reducible to standard types – Singular solutions – Lagrange’s linear equation – Integral surface passing through a given curve – Classification of partial differential equations - Solution of linear equations of higher order with constant coefficients – Linear non-homogeneous partial differential equations.

UNIT V FOURIER SERIES SOLUTIONS OF PARTIAL DIFFERENTIAL EQUATIONS **12**

Dirichlet’s conditions – General Fourier series – Half range sine and cosine series - Method of separation of variables – Solutions of one dimensional wave equation and one-dimensional heat equation – Steady state solution of two-dimensional heat equation – Fourier series solutions in Cartesian coordinates.

TOTAL: 60 PERIODS**OUTCOMES:**

Upon successful completion of the course, students should be able to:

- Explain the fundamental concepts of advanced algebra and their role in modern mathematics and applied contexts.
- Demonstrate accurate and efficient use of advanced algebraic techniques.
- Demonstrate their mastery by solving non - trivial problems related to the concepts and by proving simple theorems about the statements proven by the text.
- Able to solve various types of partial differential equations. Able to solve engineering problems using Fourier series.

TEXTBOOKS:

1. Grewal B.S., “Higher Engineering Mathematics”, Khanna Publishers, New Delhi, 43rd Edition, 2014.
2. Friedberg, A.H., Insel, A.J. and Spence, L., “Linear Algebra”, Prentice Hall of India, New Delhi, 2004.

REFERENCES:

1. James, G. “Advanced Modern Engineering Mathematics”, Pearson Education, 2007.
2. Kolman, B. Hill, D.R., “Introductory Linear Algebra”, Pearson Education, New Delhi, 2009.

SUBJECT CODE : MA8352

YEAR/SEMESTER : II/03

SUBJECT NAME : LINEAR ALGEBRA AND PARTIAL DIFFERENTIAL EQUATIONS

SUBJECT HANDLER : MR.M. RANJITHKUMAR

JIT-2106

UNIT I – VECTOR SPACES	
Vector spaces – Subspaces – Linear combinations and linear system of equations – Linear independence and linear dependence – Bases and dimensions.	
PART * A	
Q.NO.	QUESTIONS
1.	<p>Define vector space. BTL1</p> <p>A vector space V over a field F consists of a set on which two operations (additions and scalar multiplication) are defined</p> <p>i. $x + y \in V$ for each pair of elements $x, y \in V$</p> <p>ii. $a \cdot x \in V$ for each element $a \in F$ and $x \in V$.</p>
2	<p>Prove cancellation law for vector addition. BTL2</p> <p>Let $x, y, z \in V$, where V is a vector space over a field F.</p> <p>Assume $x + z = y + z$ to prove $x = y$.</p> <p>There exists a vector v in V such that $z + v = 0$.</p> $\Rightarrow x = x + 0 = x + (z + v) = (x + z) + v$ $= (y + z) + v = y + (z + v) = y + 0 = y.$
3	<p>Prove that the identity element of the vector space is unique. BTL2</p> <p>Let $x \in V$ and $e, e' \in V$</p> $x + e = x \text{ and } x + e' = x$ $\Rightarrow x + e = x + e'$ <p>By left cancellation law, $\Rightarrow e = e'$</p>
4	<p>Prove that the inverse element of the vector space is unique. BTL3</p> <p>Let $x \in V$ and $y, y' \in V$</p> $x + y = e \text{ and } x + y' = e$ $\Rightarrow x + y = x + y'$ <p>By left cancellation law, $\Rightarrow y = y'$.</p>
5	<p>Write the distributive law for vector space. BTL1</p> <p>i. $a(x + y) = ax + ay$</p> <p>ii. $(a + b)x = ax + bx$</p>
6	<p>Let $S = \{0, 1\}$ and $F = R$. Show that $f = g$ where $f(t) = 2t + 1, g(t) = 1 + 4t - 2t^2$. BTL1</p> <p>i. $f(0) = g(0)$</p> <p>ii. $f(1) = g(1)$.</p> <p>Here $f(0) = 1$ and $g(0) = 1$</p> $f(1) = 3 \text{ and } g(1) = 3$
7	<p>Define subspace of a vector space. BTL1</p> <p>A subset W of a vector space V over a field F is called a subspace of V, if W is a vector space over F with operations of addition and scalar multiplication defined on V.</p>
8	<p>Define direct sum. BTL1</p> <p>A vector space V is called the direct sum of the subspaces W_1 and W_2 such that $W_1 \cap W_2 = \{0\}$ and $W_1 + W_2 = V$. We denote that V is the direct sum of W_1 and W_2 by writing $V = W_1 \oplus W_2$.</p>

9	<p>How many matrices are there in the vector space $M_{m \times n}(z_2)$? BTL3</p> <p>There are 2^{mn} vectors in the given vector space.</p>
10	<p>Prove that $(A^t)^t = A$ for each $A \in M_{m \times n}(F)$. BTL2</p> <p>We have $(A^t)_{ij} = A_{ji}$</p> <p>Thus $\left[(A^t)^t \right]_{ij} = (A^t)_{ji} = A_{ij}$</p> <p>So that $(A^t)^t = A$ as required.</p>
11	<p>Prove that $tr(aA + bB) = a tr(A) + b tr(B)$. BTL2</p> $tr(aA + bB) = \sum_{i=1}^n (aA + bB)_{ii}$ $= \sum_{i=1}^n aA_{ii} + bB_{ii}$ $= a \sum_{i=1}^n A_{ii} + b \sum_{i=1}^n B_{ii}$ $= a tr(A) + b tr(B).$
12	<p>Define Linear combination. BTL1</p> <p>Let V be a vector space and S be a non-empty subset of V. A vector $v \in V$ is called a linear combination of vectors of S if there exists a finite number of vectors v_1, v_2, \dots, v_n in S and scalars a_1, a_2, \dots, a_n in F such that $v = a_1v_1 + a_2v_2 + \dots + a_nv_n$</p>
13	<p>Define linear span with example. BTL1</p> <p>Let S be a non-empty subset of a vector space V. The span of S denoted as $L(S)$, is the set consisting of all linear combinations of the vectors in S.</p> <p>Example: $L(S) = \{ \alpha(1, 2) + \beta(2, 1) / \alpha, \beta \in F \}$.</p>
14	<p>Let V be a vector space over F and $S_1 \subseteq S_2 \subseteq V$ then prove $L(S_1) \subseteq L(S_2)$. BTL3</p> <p>Let $v_i \in S_1$ then $\alpha_i v_i \in L(S_1)$.</p> <p>$S_1 \subseteq S_2 \Rightarrow v_i \in S_2$ and $\alpha_i v_i \in L(S_2)$</p> <p>This implies $L(S_1) \subseteq L(S_2)$.</p>
15	<p>Define linear dependence and linear independence. BTL1</p> <p>A subset S of a vector space V is called linearly dependent if there exist a finite number of distinct vectors u_1, u_2, \dots, u_n in S and scalars a_1, a_2, \dots, a_n not all zero, such that $a_1u_1 + a_2u_2 + \dots + a_nu_n = 0$.</p> <p>If the subset S is not linear dependent is called linearly independent.</p>
16	<p>Verify whether the given set in $M_{2 \times 3}(R)$ is linearly dependent or not. Where</p> $S = \left\{ \begin{bmatrix} 1 & -3 & 2 \\ -4 & 0 & 5 \end{bmatrix}, \begin{bmatrix} -3 & 7 & 4 \\ 6 & -2 & -7 \end{bmatrix}, \begin{bmatrix} -2 & 3 & 11 \\ -1 & -3 & 2 \end{bmatrix} \right\} .$ BTL3

	$a_1 \begin{bmatrix} 1 & -3 & 2 \\ -4 & 0 & 5 \end{bmatrix} + a_2 \begin{bmatrix} -3 & 7 & 4 \\ 6 & -2 & -7 \end{bmatrix} + a_3 \begin{bmatrix} -2 & 3 & 11 \\ -1 & -3 & 2 \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix}$ $a_1 = 5, a_2 = 3, a_3 = -2, \text{ therefore } S \text{ is linearly dependent.}$
17	<p>Define Minimal generating set. BTL1</p> <p>Let V be a vector space over F and S contained in V then S is called minimal generating set for V if</p> <p>(i). $L(S) = V$</p> <p>(ii). No proper subset of S will generate.</p>
18	<p>Define basis of a vector space. BTL1</p> <p>A basis B for a vector space V is a linearly independent subset of V that generates V. If B is a basis for V,</p> <p>(i). If B consists of linearly independent vectors.</p> <p>(ii). $L(B) = V$.</p>
19	<p>Define finite dimensional vector space. BTL1</p> <p>A vector space is called finite dimensional if it has a basis consisting of a finite number of vectors. The unique number of vectors in each basis for V is called the dimension of V and is denoted by $\dim(V)$.</p>
20	<p>Find the dimensions of W, where $W = \{(x_1, x_2, x_3) / x_1 + x_2 + x_3 = 0\}$. BTL4</p> <p>Here $(x_1, x_2, -x_1 - x_2) = x_1(1, 0, -1) + x_2(0, 1, -1)$</p> <p>Therefore, $B = \{(1, 0, -1), (0, 1, -1)\}$ is a basis of W.</p>
PART * B	
1	<p>In any vector space V, prove the following statements are true:</p> <p>i. $0 \cdot x = 0$ for each $x \in V$.</p> <p>ii. $(-a)x = -ax = a(-x)$ for each $a \in F$ and each $x \in V$.</p> <p>iii. $a(0) = 0$ for each $a \in F$</p> <p>iv. $ax = 0$ either $a = 0$ or $x = 0$. (8 M) BTL1</p> <p>Answer : Page : 1.7 – Dr.M. Chandrasekar</p> <ul style="list-style-type: none"> • Commutative law. (2 M) • Identity law. (2 M) • Distributive law (2 M) • Inverse law (2 M)
2	<p>Verify that the set V of all ordered triples of real numbers of the form $(x, y, 0)$ and defined the operations $+$ and \square by</p> <p>i. $(x, y, 0) + (x', y', 0) = (x + x', y + y', 0)$</p> <p>ii. $c \cdot (x, y, 0) = (cx, cy, 0)$ is a vector space or not. (8 M) BTL3</p> <p>Answer : Page : 1.11– Dr.M. Chandrasekar</p> <ol style="list-style-type: none"> a. Closure axiom (2 M) b. Associative axiom (2 M) c. Existence of identity element (2 M)

	d. Existence of inverse element (2 M)
3	<p>Let V be a vector space and W a subset of V. then prove that W is subspace of V if and only if the following 3 conditions hold.</p> <p>a. $0 \in W$ b. $x + y \in W$ whenever $x, y \in W$ c. $cx \in W$ whenever $x \in W, c \in F$. (8 M) BTL4</p> <p>Answer : Page : 1.14– Dr.M. Chandrasekar</p> <p>i. Definition of vector space (2 M) ii. Cancellation law (2M) iii. To prove (a), (b) and (c) uses the properties of vector space. (2 M) iv. Converse part: use the axioms (a), (b) and (c). (2 M)</p>
4	<p>Prove that a subset W of a vector space V is a subspace of V if and only if $ax + by \in W$ for all $x, y \in W, a, b \in F$. (8 M) BTL5</p> <p>Answer : Page : 1.15 – Dr.M. Chandrasekar</p> <p>i. Proof of necessary part: $ax + by \in W$ (4 M) ii. Proof of sufficient part: (4 M)</p>
5	<p>Let $V = R^3$; $W = \{(a_1, a_2, a_3) / 2a_1 - 7a_2 + a_3 = 0\}$ verify whether it is a subspace or not. (8 M) BTL5</p> <p>Answer : Page : 1.18</p> <ul style="list-style-type: none"> • Definition of subspace (2 M) • $\alpha w_1 + \beta w_2 = (\alpha a_1 + \beta b_1, \alpha a_2 + \beta b_2, \alpha a_3 + \beta b_3) = 0$ • W - subspace of V. (6 M)
6	<p>Let $V = R^3$; $W = \{(a_1, a_2, a_3) / a_1 = a_3 + 2\}$ verify whether it is a subspace or not. (8 M) BTL5</p> <p>Answer : Page : 1.19 – Dr.M. Chandrasekar</p> <ul style="list-style-type: none"> • Definition of subspace (2 M) • $\alpha w_1 + \beta w_2 = (\alpha a_1 + \beta b_1, \alpha a_2 + \beta b_2, \alpha a_3 + \beta b_3)$ $= 2\alpha + 2\beta - 2$ $\alpha w_1 + \beta w_2 \notin W$ • W - not a subspace. (6 M)
7	<p>Prove that the intersection of subspace of a vector space is a subspace of V. (8 M) BTL4</p> <p>Answer : Page : 1.19 – Dr.M. Chandrasekar</p> <ul style="list-style-type: none"> • Definition of subspace (2 M) • Let $W = \{\cap W_i / W_i \text{ - subspace of } V\}$ • $x, y \in W \Rightarrow x + y \in W$ $x \in W, \alpha \in F \Rightarrow \alpha x \in W$ W - subspace. (6 M)
8	<p>Prove that the union of two subspaces of V need not be a subspace of V. (8 M) BTL3</p> <p>Answer : Page : 1.20 – Dr.M. Chandrasekar</p> <ul style="list-style-type: none"> • Definition of subspace (2 M)

	<ul style="list-style-type: none"> • $W_1 = \{(0, x, y) / x, y \in R\}$ subspaces of V • $W_2 = \{(x, 0, y) / x, y \in R\}$ • $W_1 \cup W_2 = \{(x, y, z) / \text{either } x=0 \text{ or } y=0\}$ - not a subspace of V (6 M)
9	<p>Let W_1 and W_2 be subspaces of V . Prove that $W_1 \cup W_2$ is a subspaces of V if and only if $W_1 \subseteq W_2$ (or) $W_2 \subseteq W_1$. (8 M) BTL4</p> <p>Answer : Page : 1.21 – Dr.M. Chandrasekar</p> <ul style="list-style-type: none"> • Definition of vector space (2 M) • Definition of subspace (2 M) • Proof of the theorem (4 M)
10	<p>Show that F^n is the direct sum of the subspaces $W_1 = \{(a_1, a_2, \dots, a_n) \in F^n, a_n = 0\}$ and $W_2 = \{(a_1, a_2, \dots, a_n) \in F^n, a_1 = a_2 = \dots = a_{n-1} = 0\}$. (8 M) BTL5</p> <p>Answer : Page : 1.22 – Dr.M. Chandrasekar</p> <ul style="list-style-type: none"> • Definition of subspace (2 M) • $\alpha p + \beta q = \alpha(a_1, a_2, \dots, 0) + \beta(0, 0, \dots, 0)$ $= (\alpha a_1 + \beta a_1, \alpha a_2 + \beta a_2, \dots, 0) \in W_1$ • W_1 - subspace of $V = F^n$ • Definition of direct sum (2 M) • Proof of the problem (4 M)
11	<p>Let $V = R^2$, $S = \{(1, 2), (2, 1)\}$, $v = (2, 2) \in V$ and $a, b \in F$. Check whether V is a linear combination. (8 M) BTL3</p> <p>Answer : Page : 1.26 – Dr.M. Chandrasekar</p> <ul style="list-style-type: none"> • Definition of linear combination (2 M) • $v = \alpha v_1 + \beta v_2 \Rightarrow (2, 2) = (\alpha + 2\beta, 2\alpha + \beta)$ • $\alpha = \frac{2}{3}, \beta = \frac{2}{3}$ (2 M) • v - a linear combination of v_1 & v_2 (4 M)
12	<p>Write the vector $v = (1, -2, 5)$ as a linear combination of the vectors $e_1 = (1, 1, 1)$; $e_2 = (1, 2, 3)$; $e_3 = (2, -1, 1)$. (8 M) BTL5</p> <p>Answer : Page : 1.29 – Dr.M. Chandrasekar</p> <ul style="list-style-type: none"> (i). Definition of linear combination (2 M) (ii). $v = -6e_1 + 3e_2 + 2e_3$ (iii). Solved the problems based on (i). (6 M) <p>Note: use the Cramer's rule for solving the equations.</p>

13	<p>Write the matrix $E = \begin{bmatrix} 3 & 1 \\ 1 & -1 \end{bmatrix}$ as a linear combination of the matrices $A = \begin{bmatrix} 1 & 1 \\ 1 & 0 \end{bmatrix}$; $B = \begin{bmatrix} 0 & 0 \\ 1 & 1 \end{bmatrix}$; $C = \begin{bmatrix} 0 & 2 \\ 0 & -1 \end{bmatrix}$. (8 M) BTL5</p> <p>Answer : Page : 1.30 – Dr.M. Chandrasekar</p> <ul style="list-style-type: none"> • Definition of linear combination (2 M) • $E = \alpha A + \beta B + \gamma C$ • $\begin{pmatrix} 3 & 1 \\ 1 & -1 \end{pmatrix} = \begin{pmatrix} \alpha & \alpha + 2\gamma \\ \alpha + \beta & \beta - \gamma \end{pmatrix}$ • $\alpha = 3, \beta = -2, \gamma = -1$ (2 M) • $E = 3A - 2B - C$ (4 M)
14	<p>State and prove direct sum theorem. (8 M) BTL5</p> <p>Answer : Page : 1.30 – Dr.M. Chandrasekar</p> <ul style="list-style-type: none"> (i). Definition of direct sum (2 M) (ii). Statement (2 M) (iii). Proof of the theorem (4 M)
15	<p>Verify whether the given set in $M_{2 \times 3}(R)$ is linearly dependent or not. Where</p> <p>$S = \left\{ \begin{bmatrix} 1 & -3 & 2 \\ -4 & 0 & 5 \end{bmatrix}, \begin{bmatrix} -3 & 7 & 4 \\ 6 & -2 & -7 \end{bmatrix}, \begin{bmatrix} -2 & 3 & 11 \\ -1 & -3 & 2 \end{bmatrix} \right\}$. (8 M) BTL2</p> <p>Answer : Page : 1.45 – Dr.M. Chandrasekar</p> <ul style="list-style-type: none"> (i). Definition of linear independent and dependent (2 M) (ii). Solution of problem based on (i) (6 M)
16	<p>Prove that the set $S = \{(1,0,0,-1), (0,1,0,-1), (0,0,1,-1), (0,0,0,1)\}$ is linearly independent. (8 M) BTL3</p> <p>Answer : Page : 1.46 – Dr.M. Chandrasekar</p> <ul style="list-style-type: none"> (i). Definition of linear independent and dependent (2 M) (ii). Solution of problem based on (i) (6 M)
17	<p>Let $S = \{v_1, v_2, v_3\}$ where $v_1 = (2,1,0)$, $v_2 = (-3,-3,1)$ and $v_3 = (-2,1,-1)$. Show that S is a basis of R^3. (8 M)</p> <p>Answer : Page : 1.52 – Dr.M. Chandrasekar</p> <ul style="list-style-type: none"> (i). Definition of linearly independent (2 M) (ii). Definition of basis (2 M) (iii). $v = \alpha_1 v_1 + \alpha_2 v_2 + \alpha_3 v_3$ & Conclusion (4 M)
18	<p>Let V be a vector space having a finite basis, then prove that every basis for V contains the same number of vectors. (8 M) BTL4</p> <p>Answer : Page : 1.58 – Dr.M. Chandrasekar</p> <ul style="list-style-type: none"> (i). Definition of linearly independent (2 M) (ii). Definition of finite basis (2 M) (iii). Proof of the theorem (4 M)
19	<p>Let W be a subspace of a finite dimensional vector space V. Then prove that W is finite dimensional and $\dim(W) \leq \dim(V)$. Moreover if $\dim(W) = \dim(V)$ then $V=W$. (8 M) BTL5</p> <p>Answer : Page : 1.59 – Dr.M. Chandrasekar</p>

	(i). Definition of linear independent (2 M) (ii). Definition of finite basis (2 M) (iii). Proof of the theorem (4 M)
20	<p>Let V be a vector space with dimension n. Then prove the following: (a). Any finite generating set for V contains atleast n vectors, and a generating set for V that contains exactly n vectors is a basis for V. (b). any linearly independent subset of V that contains exactly n vectors is a basis for V. (8 M) BTL4 Answer : Page : 1.63 – Dr.M. Chandrasekar (i). Definition of linear independent (2 M) (ii). Definition of finite basis (2 M) (iii). Proof of the theorem (a) (2 M) (iv). Proof of the theorem (b) (2 M)</p>
21	<p>Let V be a finite dimensional vector space over a field F and A & B are subspaces V then prove that $\dim(A+B) = \dim(A) + \dim(B) - \dim(A \cap B)$. (16 M) BTL4 Answer : Page :1.44 – Mr. Friedberg (i). Definition of linear independent (2 M) (ii). $\dim(A+B) \leq \dim(V)$ (2 M) (iii). Definition of span. (2 M) $A+B = \text{span}(\alpha)$ (4 M) (iv). Definition of finite basis (2 M) (v). Prove of $\dim(A+B) = \dim(A) + \dim(B) - \dim(A \cap B)$ (4 M)</p>
22	<p>Is $\{(1, 4, -6), (1, 5, 8), (2, 1, 1), (0, 1, 0)\}$ a linearly independent subset of R^3 ? Justify your answer. (8M) BTL1 Answer : Page :1.66 – Dr.M. Chandrasekar (i). Definition of linear combination (2 M) (ii). Solved the problems based on (i). (6 M)</p>
23	<p>Show that the matrices $\begin{bmatrix} 1 & 0 \\ 0 & 0 \end{bmatrix}, \begin{bmatrix} 0 & 1 \\ 0 & 0 \end{bmatrix}, \begin{bmatrix} 0 & 0 \\ 1 & 0 \end{bmatrix}$ and $\begin{bmatrix} 0 & 0 \\ 0 & 1 \end{bmatrix}$ generate $M_{2 \times 2}(F)$. (8 M) BTL2 Answer : Page : 1.65 – Dr.M. Chandrasekar (i). Definition of linear combination (2 M) (ii). Solution of the problems based on (i). (4 M) (iii). Conclusion: Linearly independent (2 M)</p>
24	<p>Determine the following set is linearly dependent or linearly independent $\{x^3 + 2x^2, -x^2 + 3x + 1, x^3 - x^2 + 2x - 1\}$ in $P_3(R)$. (8 M) (Nov/Dec 2018) BTL3 Answer : Page :1.65 – Dr.M. Chandrasekar (i). Definition of linear dependent & independent (2 M) (ii). Solution of the problem (4 M) (iii). Conclusion: Linearly independent (2 M)</p>
25	<p>Find the dimension of W where W is given by $W = \{(a, b, c) : 2a + 3b = c; 7c + 9b = a\}$. (8 M) BTL4 Answer : Page : 1.62 – Dr.M. Chandrasekar</p>

	(i). Definition of linear dependent & independent	(2 M)
	(ii). $a = k; c = 2k + 3b; b = -(13/30)k$	(4 M)
	(iii). $\text{Dim}(W)=1$	(2 M)

JIT-2106

UNIT II – LINEAR TRANSFORMATIONS AND DIAGONALIZATION

Linear transformation - Null spaces and ranges - Dimension theorem - Matrix representation of a linear transformations - Eigenvalues and eigenvectors - Diagonalizability.

PART * A

Q.No.	Questions
1.	<p>Define linear transformation. BTL1 Let V and W be vector spaces over F. A function $T:V \rightarrow W$ a linear transformation from V to W if for all $x, y \in V$ and $c \in F$, we have</p> <p>(i) $T(x+y) = T(x) + T(y)$ (ii) $T(ax) = aT(x)$</p>
2	<p>Show that T is linear wen $T:R^2 \rightarrow R^2$ is defined $T(x, y) = (2x + y, x)$. BTL4 Let $x = (a_1, b_1)$ & $y = (a_2, b_2)$ To prove: $T(cx + y) = cT(x) + T(y)$ LHS = $T(cx + y) = T(ca_1 + a_2, cb_1 + b_2) = (2(ca_1 + a_2) + cb_1 + b_2, ca_1 + a_2)$ RHS = $cT(x) + T(y) = cT(a_1, b_1) + T(a_2, b_2) = c((2a_1 + b_1), a_1) + (2a_2 + b_2, a_2)$ LHS=RHS, this implies T is linear.</p>
3	<p>Define Null space. BTL2 Let V and W be the vector spaces and $T:V \rightarrow W$ be linear, the null space or Kernel of T defined by $N(t) = \{x \in V / T(x) = 0\}$</p>
4	<p>Define range of the transformation. BTL2 Let V and W be the vector spaces and $T:V \rightarrow W$ be linear, the range of T defined by $R(T) = \{T(x) : x \in V\}$.</p>
5	<p>Define nullity of T. BTL2 Let V and W be the vector spaces and $T:V \rightarrow W$ be linear, the null space or Kernel of T defined by $N(t) = \{x \in V / T(x) = 0\}$. And the nullity of T to be the dimensional of $N(T)$.</p>
6	<p>Define rank of T. BTL2 Let V and W be the vector spaces and $T:V \rightarrow W$ be linear, the range of T defined by $R(T) = \{T(x) : x \in V\}$. And the rank of T to be the dimensional of $R(T)$.</p>
7	<p>Define matrix representation of linear transformation. BTL1 Let $T:V \rightarrow W$ be any linear transformation and $B_1 = \{u_1, u_2, \dots, u_n\}$, $B_2 = \{w_1, w_2, \dots, w_n\}$ be the basis for V and W respectively. $T(u_i) = a_{i1}w_1 + a_{i2}w_2 + \dots + a_{in}w_n \in W$</p> $[T]_{B_1}^{B_2} = \begin{bmatrix} a_{11} & a_{12} & \cdots & a_{1n} \\ a_{21} & a_{22} & \cdots & a_{2n} \\ \vdots & \vdots & \vdots & \vdots \\ a_{m1} & a_{m2} & \cdots & a_{mn} \end{bmatrix} .$

8	<p>Find the algebraic multiplicity of all Eigen values from $\begin{bmatrix} 3 & 1 & 0 \\ 0 & 3 & 4 \\ 0 & 0 & 4 \end{bmatrix}$. BTL2</p> <p>Let $A = \begin{bmatrix} 3 & 1 & 0 \\ 0 & 3 & 4 \\ 0 & 0 & 4 \end{bmatrix}$ and solve $A - \lambda I = 0$.</p> $\Rightarrow (3 - \lambda)^2 (4 - \lambda) = 0$ <p>Therefore the Eigen values are $\lambda = 3, 3, 4$. The algebraic multiplicity of 3 is 2 The algebraic multiplicity of 4 is 1.</p>
9	<p>Test the matrix $A = \begin{pmatrix} 1 & 1 \\ 1 & 1 \end{pmatrix} \in M_{2 \times 2}(R)$ for diagonalizable. BTL3</p> $ A - tI_n = \begin{vmatrix} 1-t & 1 \\ 1 & 1-t \end{vmatrix} = t_2 - 2t = t(t-2)$ <p>$t = 0, 2$, the eigenvalues are distinct. They are diagonalizable.</p>
10	<p>Define Eigen space. BTL1</p> <p>Let T be a linear operator on a vector space V and let λ be an eigenvalue of T. Define $E_\lambda = \{x \in V : T(x) = \lambda x\} = N(T - \lambda I_V)$. The set E_λ is called the Eigen space of T, corresponding to the Eigenvalue λ .</p>
11	<p>Is there a linear transformation $T : R^3 \rightarrow R^2$ such that $T(1, 0, 3) = (1, 1)$ and $T(-2, 0, -6) = (2, 1)$? BTL4</p> <p>Ans: $T(-2, 0, -6) = T(-2(1, 0, 3)) = -2T(1, 0, 3)$ $= -2(1, 1) = (-2, -2)$ $(2, 1) \neq (-2, -2)$ therefore the given transformation is not linear.</p>
12	<p>Define diagonalizable. BTL1</p> <p>A linear operator T on a finite dimensional vector space V is called diagonalizable if there is an ordered basis B for V such that $[T]_B$ is a diagonal matrix.</p>
13	<p>Define Eigenvalues and Eigenvectors of the transformation. BTL1</p> <p>Let T be a linear operator on a vector space V. A non-zero vector $v \in V$ is called an Eigenvector of T if there exists a scalar λ such that $T(v) = \lambda v$. The scalar λ is called the Eigenvalue corresponding to the Eigenvector v .</p>
14	<p>Define dimension theorem. BTL1</p> <p>Let V and W be the vector spaces and $T : V \rightarrow W$ be linear. If V is finite-dimensional then $\text{nullity}(T) + \text{rank}(T) = \dim(V)$.</p>
15	<p>Define algebraic multiplicity. BTL1</p> <p>Let λ be an Eigenvalue of a linear operator or matrix with characteristic polynomial $f(t)$. The algebraic multiplicity of λ is the largest positive integer k for which $(t - \lambda)^k$ is a factor of $f(t)$.</p>

Part-B	
1	<p>Define $T : R^2 \rightarrow R^3$ by $T(x, y) = (x+2y, 2x-y, x+5y)$ show that T is linear. (8 M) BTL2</p> <p>Answer : Page : 2.3 – Dr.M. Chandrasekar</p> <ul style="list-style-type: none"> • Definition of linear transformation (2 M) Let V and W be vector spaces over F. A function $T : V \rightarrow W$ a linear transformation from V to W if for all $x, y \in V$ and $c \in F$, we have $T(x+y) = T(x) + T(y)$ and $T(ax) = aT(x)$ • $T(cx+y) = cT(x) + T(y)$ (2 M) • Proof of the linear (4 M)
2	<p>Let V and W be the vector spaces and $T : V \rightarrow W$ be linear. then prove that $N(T)$ and $R(T)$ are subspaces of V and W respectively. (8 M)BTL5</p> <p>Answer : Page : 2.5– Dr.M. Chandrasekar</p> <ul style="list-style-type: none"> • Definition of Null space and Range. (1 M) • $T(cx+y) = cT(x) + T(y)$ (1 M) • To prove N(T) is subspace (3 M) • To prove R(T) is subspace (3 M)
3	<p>State and prove dimension theorem. (16 M) (Nov/Dec 2018) BTL4</p> <p>Answer : Page : 2.8– Dr.M. Chandrasekar</p> <ul style="list-style-type: none"> • Statement (2 M) Let V and W be the vector spaces and $T : V \rightarrow W$ be linear. If V is finite-dimensional then $\text{nullity}(T) + \text{rank}(T) = \dim(V)$. • Definition of Null space and Range. (2 M) • $T(cx+y) = cT(x) + T(y)$ (2 M) • Proof of the theorem (10 M)
4	<p>Let V and W be the vector spaces and $T : V \rightarrow W$ be linear. Then T is one-t-one iff $N(T) = \{0\}$. (8 M) BTL4</p> <p>Answer : Page : 2.8– Dr.M. Chandrasekar</p> <ul style="list-style-type: none"> • Definition of linear transformation (2 M) $T(cx+y) = cT(x) + T(y)$ • Sufficient part (3 M) • Necessary part (3 M)
5	<p>Let V and W be vector spaces of equal dimension and let $T : V \rightarrow W$ be linear then the following are equivalent.</p> <p>(i) T is 1-1 (ii) T is onto (iii) $\text{Rank}(T) = \dim(V)$ (8 M) BTL3</p> <p>Answer : Page : 2.8– Dr.M. Chandrasekar</p> <ul style="list-style-type: none"> • Dimension Theorem (2 M) $\text{nullity}(T) + \text{rank}(T) = \dim(V)$ • Proof of (i) to (ii) (2 M) • Proof of (ii) to (iii) (2 M) • Proof of (iii) to (i) (2 M)

6	<p>Let $T : R^2 \rightarrow R^3$ such that $T(1,1) = (1,0,2)$; $T(2,3) = (1,-1,4)$ find $T(8,11)$. (8 M) BTL2</p> <p>Answer : Page : 2.13– Dr.M. Chandrasekar</p> <ul style="list-style-type: none"> • Definition of linear transformation (2 M) $T(cx + y) = cT(x) + T(y)$ • Solution of problem $T(8,11) = (5, -3, 16)$. (6 M)
7	<p>Let V and W be finite dimensional vector spaces with ordered bases B_1 and B_2 respectively and let $T, U : V \rightarrow W$ be linear transformations. Then prove that</p> <p>(i) $[T + U]_{B_1}^{B_2} = [T]_{B_1}^{B_2} + [U]_{B_1}^{B_2}$</p> <p>(ii) $[aT]_{B_1}^{B_2} = a[T]_{B_1}^{B_2}$ for all scalars. (8 M) (Nov/Dec 2018) BTL4</p> <p>Answer : Page : 2.22– Dr.M. Chandrasekar</p> <ul style="list-style-type: none"> • Definition of linear transformation (2 M) $T(cx + y) = cT(x) + T(y)$ • Solution of problem $[T + U]_{B_1}^{B_2} = [T]_{B_1}^{B_2} + [U]_{B_1}^{B_2}$ (2M) • $T(8,11) = (5, -3, 16)$. (4 M)
8	<p>Let $T : R^2 \rightarrow R^3$ and $U : R^2 \rightarrow R^3$ be the linear transformations respectively defined by $T(a_1, a_2) = (a_1 + 3a_2, 0, 2a_1 - 4a_2)$ and $U(a_1, a_2) = (a_1 - a_2, 2a_1, 3a_1 + 2a_2)$ then prove that $[T + U]_{B_1}^{B_2} = [T]_{B_1}^{B_2} + [U]_{B_1}^{B_2}$. (8 M) BTL2</p> <p>Answer : Page : 2.22– Dr.M. Chandrasekar</p> <ul style="list-style-type: none"> • Obtain T, $[T]_{B_1}^{B_2} = \begin{bmatrix} 1 & 3 \\ 0 & 0 \\ 2 & -4 \end{bmatrix}$ (3 M) • Obtain U, $[U]_{B_1}^{B_2} = \begin{bmatrix} 1 & -1 \\ 2 & 0 \\ 3 & 2 \end{bmatrix}$ (3 M) • Solution: $[T + U]_{B_1}^{B_2} = [T]_{B_1}^{B_2} + [U]_{B_1}^{B_2} = \begin{bmatrix} 2 & 2 \\ 2 & 0 \\ 5 & -2 \end{bmatrix}$ (2 M)
9	<p>Let $T : R^2 \rightarrow R^3$ be the linear transformation defined by $T(a_1, a_2) = (a_1 + 3a_2, 0, 2a_1 - 4a_2)$. Let B be the standard ordered basis of R^2 and R^3. Then prove that $[aT]_{B_1}^{B_2} = a[T]_{B_1}^{B_2}$ for all scalars a. (8M)BTL2</p> <p>Answer : Page : 2.24– Dr.M. Chandrasekar</p> <ul style="list-style-type: none"> • Obtain T, $[T]_{B_1}^{B_2} = \begin{bmatrix} 1 & 3 \\ 0 & 0 \\ 2 & -4 \end{bmatrix}$ (3 M)

	<ul style="list-style-type: none"> Obtain $[aT], [aT]_{B_1}^{B_2} = \begin{bmatrix} a & 3a \\ 0 & 0 \\ 2a & -4a \end{bmatrix}$ (3 M) Solution: $[aT]_{B_1}^{B_2} = a[T]_{B_1}^{B_2}$ (2 M)
10	<p>Let $A \in M_{m \times n}(F)$ then a scalar λ is an eigenvalue of A if and only if $\det(A - \lambda I_n) = 0$. (8M)BTL2</p> <p>Answer : Page : 2.28– Dr.M. Chandrasekar</p> <ul style="list-style-type: none"> Obtain $Av = \lambda v$, (2 M) Definition of Linear Transformation (2 M) To prove T is not invertible. (4 M) <p>$\det(A - \lambda I) = 0$.</p>
11	<p>Find all the Eigenvectors of the matrix $A = \begin{bmatrix} 1 & 1 \\ 4 & 1 \end{bmatrix}$. (8 M)BTL2</p> <p>Answer : Page : 2.31– Dr.M. Chandrasekar</p> <ul style="list-style-type: none"> Obtain v from $Av = \lambda v$. (2 M) Find the λ, from the equation $\det(A - \lambda I) = 0$. (2 M) Find the Eigen Vectors from the respective Eigen values (4 M) <p>$\lambda_1 = 3 \Rightarrow v_1 = \begin{bmatrix} 1 \\ 2 \end{bmatrix} \quad \lambda_2 = -1 \Rightarrow v_2 = \begin{bmatrix} 1 \\ -2 \end{bmatrix}$.</p>
12	<p>Determine T is diagonalizable or not. Let T be a linear operator on $P_2(R)$ defined by $T(f(x)) = f'(x)$, the matrix representation of T with respect to the standard basis B for $P_2(R)$. (8M)BTL2</p> <p>Answer : Page : 2.38– Dr.M. Chandrasekar</p> <ul style="list-style-type: none"> Obtain v from $Av = \lambda v$. (2 M) Find the λ, from the equation $\det(A - \lambda I) = 0$. (2 M) Find the Eigen Vectors from the respective Eigen values <p>$\lambda_1 = 3 \Rightarrow v_1 = \begin{bmatrix} 1 \\ 2 \end{bmatrix} \quad \lambda_2 = -1 \Rightarrow v_2 = \begin{bmatrix} 1 \\ -2 \end{bmatrix}$. (4 M)</p>
13	<p>Let T be the linear operator of R^3 defined by $T \begin{pmatrix} a_1 \\ a_2 \\ a_3 \end{pmatrix} = \begin{pmatrix} 4a_1 + a_3 \\ 2a_1 + 3a_2 + 2a_3 \\ a_1 + 4a_3 \end{pmatrix}$. Determine the Eigen space of T corresponding to each Eigenvalue. Let B be the standard ordered basis for R^3. (16M)BTL4</p> <p>Answer : Page : 2.39– Dr.M. Chandrasekar</p> <ul style="list-style-type: none"> Obtain v from $Av = \lambda v$. (2 M) Find the λ, from the equation $\det(A - \lambda I) = 0$. (2 M) Find the Eigen Vectors from the respective Eigen values

	$\lambda_1 = 3 \Rightarrow v_1 = \begin{bmatrix} 1 \\ 2 \end{bmatrix} \quad \lambda_1 = -1 \Rightarrow v_1 = \begin{bmatrix} 1 \\ -2 \end{bmatrix}. \quad (4 \text{ M})$
14	<p>Test the matrix $A = \begin{bmatrix} 3 & 1 & 0 \\ 0 & 3 & 0 \\ 0 & 0 & 4 \end{bmatrix} \in M_{3 \times 3}(R)$ for diagonalizability. (8M) BTL3</p> <p>Answer : Page : 2.44– Dr.M. Chandrasekar</p> <ul style="list-style-type: none"> Eigenvalue of A $\det(A - \lambda I) = 0.$, $\lambda = 3, 3, 4$ (2 M) Obtain the multiplicity of the Eigenvalue. (4 M) Conclusion: Not diagonalizable (2 M)
15	<p>Let T be a linear operator on $P_2(R)$ defined by $T[f(x)] = f(1) + f'(0)x + [f'(0) + f''(0)]x^2$. Test for diagonalizability. (8M) BTL3</p> <p>Answer : Page : 2.44– Dr.M. Chandrasekar</p> <ul style="list-style-type: none"> Matrix of the given transformation $B = \begin{bmatrix} 1 & 1 & 1 \\ 0 & 1 & 0 \\ 0 & 1 & 2 \end{bmatrix}$. (2 M) Eigenvalue of B: $\det(B - \lambda I) = 0.$, $\lambda = 1, 1, 2$ (2 M) Obtain the multiplicity of the Eigenvalue. (2 M) Conclusion: Diagonalizable $[T]_B = \begin{bmatrix} 2 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix}$ (2 M)
16	<p>Find A^n for the matrix A. Verify the matrix $A = \begin{pmatrix} 0 & -2 \\ 1 & 3 \end{pmatrix}$ is diagonalisable or not. (8M) BTL3</p> <p>Answer : Page : 2.48– Dr.M. Chandrasekar</p> <ul style="list-style-type: none"> Eigenvalue of A: $\det(A - \lambda I) = 0.$, $\lambda = 1, 2$ (2 M) Obtain the Eigenvector of the respective Eigenvalue. $\lambda = 1 \Rightarrow X_1 = \begin{bmatrix} -2 \\ 1 \end{bmatrix}$ and $\lambda = 2 \Rightarrow X_1 = \begin{bmatrix} 1 \\ -1 \end{bmatrix}$ (2 M) Conclusion: Diagonalizable $[T]_A = \begin{bmatrix} 1 & 0 \\ 0 & 2 \end{bmatrix}$ (2 M) $A^n = \begin{bmatrix} 2 - 2^n & 2 - 2^{n+1} \\ -1 + 2^n & -1 + 2^{n+1} \end{bmatrix}$ (2 M)
17	<p>Find the general solution for the following system of differential equations</p> $\begin{aligned} x_1' &= x_1 + x_3 \\ x_2' &= x_2 + x_3 \\ x_3' &= 2x_3 \end{aligned} \quad . \quad (16\text{M})\text{BTL6}$

	<p>Answer : Page : 2.56– Dr.M. Chandrasekar</p> <ul style="list-style-type: none"> Find the coefficient Matrix of the given system. (2 M) Eigenvalue of A: $\det(A - \lambda I) = 0.$, $\lambda = 1, 1, 2$ (2 M) Eigenvalues and Eigen vectors $X_1 = \begin{bmatrix} 1 \\ 0 \\ 0 \end{bmatrix}$, $X_2 = \begin{bmatrix} 0 \\ 1 \\ 0 \end{bmatrix}$, $X_3 = \begin{bmatrix} 1 \\ 1 \\ 1 \end{bmatrix}$ (4 M) $x(t) = e^t c_1 \begin{bmatrix} 1 \\ 0 \\ 0 \end{bmatrix} + c_2 e^t \begin{bmatrix} 0 \\ 1 \\ 0 \end{bmatrix} + c_3 e^{2t} \begin{bmatrix} 1 \\ 1 \\ 1 \end{bmatrix}$ (8 M)
18	<p>Find the general solution for the following system of differential equations</p> $\begin{aligned} x_1' &= 3x_1 + x_2 + x_3 \\ x_2' &= 2x_1 + 4x_2 + 2x_3 \quad \text{(16M)BTL6} \\ x_3' &= -x_1 - x_2 + x_3 \end{aligned}$ <p>Answer : Page : 2.48– Dr.M. Chandrasekar</p> <ul style="list-style-type: none"> Find the coefficient Matrix of the given system. (2 M) Eigenvalue of A: $\det(A - \lambda I) = 0.$, $\lambda = 2, 2, 4$ (2 M) Eigen vectors $X_1 = \begin{bmatrix} -1 \\ 0 \\ 1 \end{bmatrix}$, $X_2 = \begin{bmatrix} 0 \\ -1 \\ 1 \end{bmatrix}$, $X_3 = \begin{bmatrix} -1 \\ -2 \\ 1 \end{bmatrix}$ (4 M) $x(t) = e^t c_1 \begin{bmatrix} 1 \\ 0 \\ 0 \end{bmatrix} + c_2 e^t \begin{bmatrix} 0 \\ 1 \\ 0 \end{bmatrix} + c_3 e^{2t} \begin{bmatrix} 1 \\ 1 \\ 1 \end{bmatrix}$ (8 M)
19	<p>Let T be linear operator on a finite dimensional vector space V such that the characteristic polynomial of T splits. Let $\lambda_1, \lambda_2, \dots, \lambda_k$ be the distinct eigenvalues of T. Then prove that T is diagonalizable iff the multiplicity of λ_i is equal to $\dim(E_{\lambda_i})$ for all i. (8 M) BTL3</p> <p>Answer : Page : 2.43– Dr.M. Chandrasekar</p> <ul style="list-style-type: none"> Dimension Theorem $\text{nullity}(T) + \text{rank}(T) = \dim(V)$ (2 M) Sufficient Part (3 M) Necessary Part $\text{multiplicity of } \lambda_i \text{ is equal to } \dim(E_{\lambda_i}) \text{ for all } i.$ (3 M)
20	<p>Let T be a linear operator on a vector space V and let $\lambda_1, \lambda_2, \dots, \lambda_k$ be distinct Eigenvalues of T. if v_1, v_2, \dots, v_k are Eigenvectors of T such that λ_i corresponds to v_i then prove that $\{v_1, v_2, \dots, v_k\}$ is linearly independent. (12 M) BTL3</p> <p>Answer : Page : 2.43– Dr.M. Chandrasekar</p>

<ul style="list-style-type: none">• Prove by mathematical induction rule. (2 M)• Definition of linearly independent and dependent. (2 M)• To prove $a_1(\lambda_1 - \lambda_k) = a_2(\lambda_2 - \lambda_k) = \dots = a_{k-1}(\lambda_{k-1} - \lambda_k) = 0$ (6 M)• Conclusion: $\{v_1, v_2, \dots, v_{k-1}, v_k\}$ is linearly independent. (2 M)
--

JIT-2106

UNIT III – INNER PRODUCT SPACES

Inner product, norms - Gram Schmidt orthogonalization process - Adjoint of linear operations - Least square approximation.

PART * A

Q.No.	Questions
1.	<p>Define inner product space. (Nov/Dec 2018) BTL1</p> <p>A vector space V over F, an inner product on V is a function that assigns to every ordered pair of vectors $x, y \in V$ and a scalar in F, denoted by $\langle x, y \rangle$ such that the following conditions hold.</p> <p>(i) $\langle x, x \rangle > 0$ iff $x \neq 0$</p> <p>(ii) $\langle x+z, y \rangle = \langle x, y \rangle + \langle z, y \rangle$</p> <p>(iii) $\langle cx, y \rangle = c \langle x, y \rangle$</p> <p>(iv) $\overline{\langle x, y \rangle} = \langle y, x \rangle$</p>
2	<p>Define Dot product. BTL1</p> <p>Let $U = (u_1, u_2, \dots, u_n)$ and $V = (v_1, v_2, \dots, v_n)$ then the dot product of U, V is defined as $U \cdot V$, $U \cdot V = u_1 v_1 + u_2 v_2 + \dots + u_n v_n$.</p>
3	<p>For any non-zero vector, $x \in V$ prove that $y = \frac{x}{\ x\ }$ is a vector such that $\ y\ = 1$. BTL2</p> <p>Consider $\langle y, y \rangle = \left\langle \frac{x}{\ x\ }, \frac{x}{\ x\ } \right\rangle = \frac{1}{\ x\ } \frac{1}{\ x\ } \langle x, x \rangle$</p> $= \frac{1}{\ x\ ^2} \ x\ ^2 = 1 .$
4	<p>Define orthonormal. BTL1</p> <p>Let V be an inner product space. A subset of V is an orthonormal basis for V if it is an ordered basis that is orthonormal.</p>
5	<p>Show that in R^3, the vectors $(1, 1, 0)$, $(1, -1, 1)$, $(-1, 1, 2)$ are orthogonal. Are they orthonormal? Justify. BTL2</p> <p>Clearly $\langle x, y \rangle = \langle x, z \rangle = \langle y, z \rangle = 0$ therefore x, y, z are orthogonal vectors.</p> <p>$\ x\ = \sqrt{2}$, $\ y\ = \sqrt{3}$, $\ z\ = \sqrt{6}$, therefore x, y, z are not orthonormal.</p>
6	<p>Let $V = R^2$ and $S = \{(1,0), (0,1)\}$. Check whether S is orthonormal basis or not. BTL4</p> <p>$\langle x, y \rangle = 0$, $\ x\ = 1$ and $\ y\ = 1$</p> <p>Therefore S is an orthonormal basis.</p>
7	<p>Define conjugate transpose. BTL2</p> <p>Let $A \in M_{m \times n}(F)$, the conjugate transpose of A to be the $(n \times m)$ matrix defined by $(A^*)_{ij} = \overline{A_{ji}}$.</p>
8	<p>Let $A = \begin{pmatrix} i & 1+2i \\ 2 & 3+4i \end{pmatrix}$. Find the conjugate transpose. BTL4</p> <p>$\overline{A} = \begin{pmatrix} -i & 1-2i \\ 2 & 3-4i \end{pmatrix}$</p>

	$A^* = \begin{pmatrix} -i & 2 \\ 1-2i & 3-4i \end{pmatrix}.$
9	<p>State Gram Schmidt orthogonalization. (Nov/Dec 2018) BTL1</p> <p>Let V be an inner product space and $S = \{w_1, w_2, \dots, w_n\}$ be a linear independent subset of V. Define $S' = \{v_1, v_2, \dots, v_n\}$. Where $v_1 = w_1$ and $v_k = w_k - \sum_{j=1}^{k-1} \frac{\langle w_k, v_j \rangle}{\ v_j\ ^2} v_j$ for $2 \leq k \leq n$. Then S' is an orthogonal set of non-zero vectors such that $\text{span}(S') = \text{span}(S)$.</p>
10	<p>Define orthogonal complement. BTL2</p> <p>Let S be a non-empty subset of an inner product space V. We define S^\perp to be the set of all vectors in V that are orthogonal to every vector in S.</p>
11	<p>State and prove projection theorem. BTL4</p> <p>Let W be a finite dimensional subspace of an inner product space V and let $y \in V$. Then there exists unique vectors $u \in W$ and $z \in W^\perp$ such that $y = u + z$. Furthermore, if $\{v_1, v_2, \dots, v_k\}$ is an orthonormal basis for W, then $u = \sum_{i=1}^k \langle y, v_i \rangle v_i$.</p>
12	<p>Define adjoint of linear operator. BTL1</p> <p>Let V be a finite dimensional inner product space and let T be a linear operator on V. Then there exist a unique function $T^* : V \rightarrow V$ such that $\langle T(x), y \rangle = \langle x, T^*(y) \rangle$ for all $x, y \in V$. The linear operator T^* is called adjoint of operator T.</p>
13	<p>If A be an $n \times n$ matrix. Then prove $L_{A^*} = (L_A)^*$. BTL2</p> <p>If B is the standard ordered basis for F^n, then $[L_A]_B = A$. Hence $[(L_A)_B]^* = [L_A]_B^* = A^* = [L_{A^*}]_B$ and so $L_{A^*} = (L_A)^*$.</p>
14	<p>Verify the Cauchy-Schwartz inequality for $x = (1, -1, 3)$ and $y = (2, 0, -1)$. BTL3</p> <p>By Cauchy-Schwartz inequality is $\langle x, y \rangle \leq \ x\ \ y\$ Here $\langle x, y \rangle = -1 = 1$, $\ x\ = \sqrt{11}$, $\ y\ = \sqrt{5}$ Cauchy-Schwartz inequality is satisfied.</p>
15	<p>Define least squares approximation. BTL1</p> <p>Error value $E = \sum_{i=1}^m (y_i - ct_i - d)^2$, the line $y = ct + d$ is called the least square line.</p>
16	<p>If T is a linear operator on V, then prove that $[T^*]_B = [T]_B^*$. BTL2</p> $[T^*]_B = \langle T^*(v_i), v_j \rangle = \overline{\langle v_i, T^*(v_j) \rangle}$ $= \overline{\langle T(v_i), v_j \rangle} = [T]_B^*.$
17	<p>Let V be an inner product space and let S be an orthogonal subset of V consisting of non-zero vectors then S is linearly independent. BTL4</p> $\sum_{i=1}^k a_i v_i = 0$

	$a_j = \frac{\langle y, v_j \rangle}{\ v_j\ ^2} = \frac{\langle 0, v_j \rangle}{\ v_j\ ^2} = 0$ for all j . Therefore S is linearly independent.
18	<p>State Cauchy's and Triangle inequality. BTL1</p> <p>(i) Cauchy's inequality $\langle x, y \rangle \leq \ x\ \ y\$</p> <p>(ii) Triangle Inequality $\ x + y\ \leq \ x\ + \ y\$</p>
19	<p>If $S = \left\{ \left(\frac{1}{\sqrt{5}}, \frac{2}{\sqrt{5}} \right), \left(\frac{2}{\sqrt{5}}, \frac{-1}{\sqrt{5}} \right) \right\}$. Verify S is orthonormal basis. BTL3</p> <p>$\begin{vmatrix} \frac{1}{\sqrt{5}} & \frac{2}{\sqrt{5}} \\ \frac{2}{\sqrt{5}} & \frac{-1}{\sqrt{5}} \end{vmatrix} = -1 \neq 0$, therefore S is linearly independent.</p> <p>$\langle x, y \rangle = 0$, $\ x\ = 1$, $\ y\ = 1$, therefore S is an orthonormal basis.</p>
20	<p>Consider $V = R^3$. Let $y_1 = (1, 1, 0)$, $y_2 = (2, 0, 1)$, $y_3 = (2, 2, 1)$. Check $\{y_1, y_2, y_3\}$ is linearly independent or not. BTL2</p> <p>$\Delta = \begin{vmatrix} 1 & 2 & 2 \\ 1 & 0 & 2 \\ 0 & 1 & 1 \end{vmatrix} = -2 \neq 0$.</p> <p>Therefore $\{y_1, y_2, y_3\}$ is linearly independent.</p>
Part-B	
1	<p>Let V be a inner product space then for $x, y, z \in V$ and $c \in F$ then prove the following statements are true:</p> <p>(i) $\langle x, y + z \rangle = \langle x, y \rangle + \langle x, z \rangle$</p> <p>(ii) $\langle x, cy \rangle = \bar{c} \langle x, y \rangle$</p> <p>(iii) $\langle x, x \rangle = 0$ iff $x = 0$</p> <p>(iv) If $\langle x, y \rangle = \langle x, z \rangle$ for all $x \in V$ then $y = z$. (8 M) BTL3</p> <p>Answer : Page : 3.4 – Dr.M. Chandrasekar</p> <ul style="list-style-type: none"> • To prove (i) use $\overline{\langle x, y \rangle} = \langle y, x \rangle$ (2 M) • To prove (ii) use $\overline{\langle x, y \rangle} = \langle y, x \rangle$ and $\langle cx, y \rangle = c \langle x, y \rangle$ (2 M) • To prove (iii) use $\langle x, x \rangle > 0$ iff $x \neq 0$ (2 M) • To prove (iv) use $\langle x + z, y \rangle = \langle x, y \rangle + \langle z, y \rangle$ (2 M)
2	<p>Let V be a inner product space then for $x, y, z \in V$ and $c \in F$ then prove the following statements are true:</p> <p>(i) $\ cx\ = c \ x\$</p>

	<p>(ii) $\ x\ = 0$ iff $x = 0$</p> <p>(iii) $\langle x, y \rangle \leq \ x\ \ y\$</p> <p>(iv) $\ x + y\ \leq \ x\ + \ y\$ for all $x \in V$ then $x = z$. (8 M) BTL3</p> <p>Answer : Page : 3.5– Dr.M. Chandrasekar</p> <ul style="list-style-type: none"> To prove (i) use $\langle cx, y \rangle = c \langle x, y \rangle$ and $\langle x, cy \rangle = \bar{c} \langle x, y \rangle$ (2 M) To prove (ii) use $\langle x, x \rangle = 0$ iff $x = 0$ (2 M) To prove (iii) use $\langle x, y + z \rangle = \langle x, y \rangle + \langle x, z \rangle$ (2 M) To prove (iv) use the Cauchy-Schwartz inequality (iii) (2 M)
3	<p>Prove that</p> <p>(i) $\left \sum_{i=1}^n a_i \bar{b}_i \right \leq \left[\sum_{i=1}^n a_i ^2 \right]^{1/2} \left[\sum_{i=1}^n b_i ^2 \right]^{1/2}$</p> <p>(ii) $\left[\sum_{i=1}^n a_i + b_i ^2 \right]^{1/2} \leq \left[\sum_{i=1}^n a_i ^2 \right]^{1/2} + \left[\sum_{i=1}^n b_i ^2 \right]^{1/2}$. (8 M) BTL3</p> <p>Answer : Page : 3.7– Dr.M. Chandrasekar</p> <ul style="list-style-type: none"> Prove (i) by Cauchy-Schwartz inequality $\langle x, y \rangle \leq \ x\ \ y\$ (4 M) Prove (ii) by Triangle inequality $\ x + y\ \leq \ x\ + \ y\$ (4 M)
4	<p>Let $V = C^3$ with inner product $\langle x, y \rangle = x_1 \bar{y}_1 + x_2 \bar{y}_2 + x_3 \bar{y}_3$. Let $x = (2, 1+i, i)$ and $y = (2-i, 2, 1+2i)$ compute</p> <p>(i) $\langle x, y \rangle$</p> <p>(ii) $\ x\$ & $\ y\$</p> <p>(iii) $\ x + y\$</p> <p>(iv) Verify Cauchy's inequality & Triangle inequality. (8M)BTL4</p> <p>Answer : Page : 3.9– Dr.M. Chandrasekar</p> <ul style="list-style-type: none"> $\langle x, y \rangle = 8 + 5i$ (2 M) $\ x\ = \sqrt{7}$ & $\ y\ = \sqrt{14}$ (2 M) $\ x + y\ = \sqrt{37}$ (2 M) $\langle x, y \rangle = \sqrt{98}$ (2 M)
5	<p>Let V be the vector space of polynomial with inner product given by $\langle f, g \rangle = \int_0^1 f(t) g(t) dt$. If $f(t) = t + 2$, $g(t) = t^2 - 2t - 3$. Find $\langle f, g \rangle$ & $\ f\$. (8 M) BTL4</p> <p>Answer : Page : 3.12– Dr.M. Chandrasekar</p> <ul style="list-style-type: none"> $\langle f, g \rangle = \int_0^1 f(t) g(t) dt = \frac{-37}{4}$ (4 M)

	<ul style="list-style-type: none"> • $\ f\ = \sqrt{\langle f, f \rangle} = \sqrt{\int_0^1 f(t)^2 dt} = \sqrt{\frac{19}{3}}$ (4 M)
6	<p>Consider the set of all continuous complex valued function in $[0,1]$ and denoted it as V.</p> <p>Let $f(t) & g(t) \in V$. Define $\langle f, g \rangle = \int_0^1 f(t) \overline{g(t)} dt$.</p> <p>Verify the conditions of inner product space. (8 M) BTL5 Answer : Page : 3.13– Dr.M. Chandrasekar</p> <ul style="list-style-type: none"> • $\langle f+g, h \rangle = \langle f, h \rangle + \langle g, h \rangle$ (2 M) • $\langle cf, g \rangle = c \langle f, g \rangle$ (2 M) • $\langle f, g \rangle = \overline{\langle g, f \rangle}$ (2 M) • $\langle f, f \rangle = 0 \Leftrightarrow f = 0$ (2 M)
7	<p>Let $V = C^3$ with inner product $\langle x, y \rangle = x_1 \overline{y_1} + x_2 \overline{y_2} + x_3 \overline{y_3}$. Verify the inner product space. (8M) BTL5 Answer : Page : 3.13– Dr.M. Chandrasekar.</p> <ul style="list-style-type: none"> (i) $\langle x, x \rangle > 0$ iff $x \neq 0$ (2 M) (ii) $\langle x+z, y \rangle = \langle x, y \rangle + \langle z, y \rangle$ (2 M) (iii) $\langle cx, y \rangle = c \langle x, y \rangle$ (2 M) (iv) $\overline{\langle x, y \rangle} = \langle y, x \rangle$ (2 M)
8	<p>Let $V = M_{n \times n}(F)$ and define $\langle A, B \rangle = \text{trace}(B^* A)$ for $A, B \in V$. Verify whether V is an inner product space or not. (8 M) BTL3 Answer : Page : 3.16– Dr.M. Chandrasekar</p> <ul style="list-style-type: none"> • $\langle A, A \rangle > 0$ iff $A \neq 0$ (2 M) • $\langle A+B, C \rangle = \langle A, C \rangle + \langle B, C \rangle$ (2 M) • $\langle cA, B \rangle = c \langle A, B \rangle$ (2 M) • $\overline{\langle A, B \rangle} = \langle B, A \rangle$ (2 M)
9	<p>Let V be an inner product space and $S = \{v_1, v_2, \dots, v_k\}$ be an orthogonal subset of V consisting of non-zero vectors. If $y \in \text{span}(S)$ then prove that $y = \sum_{i=1}^k \frac{\langle y, v_i \rangle}{\ v_i\ ^2} v_i$. (8 M) (Nov/Dec 2018) BTL2 Answer : Page : 3.17 – Dr.M. Chandrasekar.</p> <ul style="list-style-type: none"> • Definition of span (2 M) • $\langle y, v_j \rangle = a_j \ v_j\ ^2$ and $\langle y, v_j \rangle = \sum_{i=1}^k a_i \langle v_i, v_j \rangle$ (4 M)

	<ul style="list-style-type: none"> • $y = \sum_{i=1}^k \frac{\langle y, v_i \rangle}{\ v_i\ ^2} v_i$ (2 M)
10	<p>State and prove Gram Schmidt orthogonalization theorem. Answer : Page : 3.19– Dr.M. Chandrasekar (16 M) (Nov/Dec 2018) BTL2</p> <ul style="list-style-type: none"> • Statement: Let V be an inner product space and $S = \{w_1, w_2, \dots, w_n\}$ be a linear independent subset of V. Define $S' = \{v_1, v_2, \dots, v_n\}$. Where $v_1 = w_1$ and $v_k = w_k - \sum_{j=1}^{k-1} \frac{\langle w_k, v_j \rangle}{\ v_j\ ^2} v_j$ for $2 \leq k \leq n$. (8 M) • Then S' is an orthogonal set of non-zero vectors such that $\text{span}(S') = \text{span}(S)$. (8 M)
11	<p>Consider $V = \mathbb{R}^3$. Let $y_1 = (1, 1, 0)$, $y_2 = (2, 0, 1)$, $y_3 = (2, 2, 1)$. Check $\{y_1, y_2, y_3\}$ is linearly independent, using Gram Schmidt process. Compute orthogonal vectors from $\{y_1, y_2, y_3\}$. (8 M)BTL2 Answer : Page : 3.22– Dr.M. Chandrasekar</p> <ul style="list-style-type: none"> • $\Delta = \begin{vmatrix} 1 & 2 & 2 \\ 1 & 0 & 2 \\ 0 & 1 & 1 \end{vmatrix} = -2 \neq 0$. (2 M) • $x_1 = y_1 = \begin{pmatrix} 1 \\ 1 \\ 0 \end{pmatrix}$, • $x_2 = y_2 - \frac{\langle y_2, x_1 \rangle}{\ x_1\ ^2} x_1 = \begin{pmatrix} 1 \\ -1 \\ 1 \end{pmatrix}$, (2 M) • $x_3 = y_3 - \frac{\langle y_3, x_1 \rangle}{\ x_1\ ^2} x_1 - \frac{\langle y_3, x_2 \rangle}{\ x_2\ ^2} x_2 = \frac{1}{3} \begin{pmatrix} -1 \\ 1 \\ 2 \end{pmatrix}$ (2 M) • $\{x_1, x_2, x_3\}$ is an orthogonal set. (2 M)
12	<p>State and prove projection theorem. (8 M) BTL4 Answer : Page : 3.29– Dr.M. Chandrasekar</p> <ul style="list-style-type: none"> • Let W be a finite dimensional subspace of an inner product space V and let $y \in V$. Then there exists unique vectors $u \in W$ and $z \in W^\perp$ such that $y = u + z$. Furthermore, if $\{v_1, v_2, \dots, v_k\}$ is an orthonormal basis for W, then $u = \sum_{i=1}^k \langle y, v_i \rangle v_i$. (2 M)

	<ul style="list-style-type: none"> • $\langle z, v_j \rangle = \left\langle \left(y - \sum_{i=1}^k \langle y, v_i \rangle v_i \right), v_j \right\rangle = 0 \Rightarrow z \in W^\perp$ (4 M) • Uniqueness of u and z. (2 M)
13	<p>Let V be an inner product space and let T and U be a linear operator on V then prove that</p> <p>(i) $(T+U)^* = T^* + U^*$</p> <p>(ii) $(cT)^* = \bar{c}T^*$</p> <p>(iii) $(TU)^* = U^*T^*$</p> <p>(iv) $(T^*)^* = T$. (8 M) BTL4</p> <p>Answer : Page : 3.34– Dr.M. Chandrasekar</p> <p>(i) $\langle x, (T+U)^*(y) \rangle = \langle (T+U)(x), y \rangle = \langle x, (T^* + U^*)y \rangle$ (2 M)</p> <p>(ii) $\langle x, (cT)^*(y) \rangle = \langle cT(x), y \rangle = \langle x, \bar{c}T^*y \rangle = \bar{c} \langle x, T^*y \rangle$ (2 M)</p> <p>(iii) $\langle x, (TU)^*(y) \rangle = \langle (TU)(x), y \rangle = \langle T(x), y \rangle \langle U(x), y \rangle = \langle x, U^*(y)T^*(y) \rangle$ (2 M)</p> <p>(iv) $\langle x, T(y) \rangle = \langle T^*(x), y \rangle = \langle x, T^{**}(y) \rangle$ (2 M)</p>
14	<p>Let V be a finite dimensional inner product space, and let T be a linear operator on V. Then prove that there exists a unique function $T^* : V \rightarrow V$ such that $\langle x, T^*(y) \rangle = \langle T(x), y \rangle$ and T^* is linear. (8 M) BTL5</p> <p>Answer : Page : 3.36– Dr.M. Chandrasekar</p> <ul style="list-style-type: none"> • Define $g : V \rightarrow F$ by $g(x) = \langle T(x), y \rangle$ • To Show g is linear. $g(cx_1 + x_2) = \langle T(cx_1 + x_2), y \rangle = c \langle T(x_1), y \rangle + \langle T(x_2), y \rangle = cg(x_1) + g(x_2)$ (4 M) <ul style="list-style-type: none"> • To show T^* is linear $\langle x, T^*(cy_1 + y_2) \rangle = \langle T(x), cy_1 + y_2 \rangle = \langle x, cT^*(y_1) + T^*(y_2) \rangle$ (4 M)
15	<p>Find the least squares line and error for the following data (1, 2), (2, 3), (3, 5), (4, 7). (8 M)BTL3</p> <p>Answer : Page : 3.41– Dr.M. Chandrasekar</p> <ul style="list-style-type: none"> • $A = \begin{pmatrix} 1 & 1 \\ 2 & 1 \\ 3 & 1 \\ 4 & 1 \end{pmatrix}$, $x_0 = \begin{pmatrix} c \\ d \end{pmatrix}$, $y = \begin{pmatrix} 2 \\ 3 \\ 5 \\ 7 \end{pmatrix}$ and $A^* = [A]^T = \begin{bmatrix} 1 & 2 & 3 & 4 \\ 1 & 1 & 1 & 1 \end{bmatrix}$ (2 M) • $(A^*A)^{-1} = \frac{1}{ A^*A } \text{adj}(A^*A) = \frac{1}{10} \begin{pmatrix} 2 & -5 \\ -5 & 15 \end{pmatrix}$ (2 M)

	<ul style="list-style-type: none"> • $(A^*A)^{-1} A^*y = \frac{1}{10} \begin{pmatrix} 2 & -5 \\ -5 & 15 \end{pmatrix} \begin{bmatrix} 1 & 2 & 3 & 4 \\ 1 & 1 & 1 & 1 \end{bmatrix} \begin{pmatrix} 2 \\ 3 \\ 5 \\ 7 \end{pmatrix} = \begin{pmatrix} 1.7 \\ 0 \end{pmatrix} = \begin{pmatrix} c \\ d \end{pmatrix}$ (2 M) • $y = ct + d = 1.7t + 0$ is the least squares line. (2 M)
16	<p>Show that the following function defines an inner product on R^2, where $u = (u_1, u_2)$ and $v = (v_1, v_2)$ and $\langle u, v \rangle = u_1v_1 + 2u_2v_2$. (8 M)BTL2</p> <p>Answer : Page : 3.46– Dr.M. Chandrasekar</p> <ul style="list-style-type: none"> • $\langle u, v \rangle = \langle v, u \rangle$ (2 M) • $\langle u, v + w \rangle = \langle u, v \rangle + \langle u, w \rangle$ (2 M) • $c\langle u, v \rangle = \langle cu, v \rangle$ (2 M) • $\langle v, v \rangle = v_1^2 + 2v_2^2 \geq 0$ this expression is equal to zero iff $v = 0$. (2 M)

UNIT IV – PARTIAL DIFFERENTIAL EQUATIONS

Formation – Solutions of first order equations – Standard types and equations reducible to standard types – Singular solutions – Lagrange’s linear equation – Integral surface passing through a given curve – Classification of partial differential equations - Solution of linear equations of higher order with constant coefficients – Linear non-homogeneous partial differential equations.

PART * A

1.	<p>Form a PDE by eliminating the arbitrary constants a and b from $z = ax + by$. BTL2</p> <p>Given $z = ax + by$ (1)</p> <p>Differentiate (1) partially w.r.to x and y, we get</p> $p = \frac{\partial z}{\partial x} = a \quad \text{and} \quad q = \frac{\partial z}{\partial y} = b$ <p>Substituting in (1) we get the required p.d.e $z = px + qy$.</p>
2	<p>Form a PDE by eliminating the constants a and b from $z = (x+a)^2 + (y+b)^2$. BTL2</p> <p>Given $z = (x+a)^2 + (y+b)^2$ (1)</p> <p>Differentiate (1) partially w.r.to x and y, we get</p> $p = \frac{\partial z}{\partial x} = 2(x+a) \Rightarrow (x+a) = \frac{p}{2}$ $q = \frac{\partial z}{\partial y} = 2(y+b) \Rightarrow (y+b) = \frac{q}{2}$ <p>Substituting in (1) we get the required p.d.e $4z = p^2 + q^2$.</p>
3	<p>Eliminate the arbitrary function f from $z = f\left(\frac{y}{x}\right)$ and form a p.d.e. BTL2</p> <p>Given $z = f\left(\frac{y}{x}\right)$ (1)</p> <p>Differentiate (1) partially w.r.to x and y, we get</p> $p = \frac{\partial z}{\partial x} = f'\left(\frac{y}{x}\right) \cdot \left(\frac{-y}{x^2}\right) \dots\dots\dots (2)$ $q = \frac{\partial z}{\partial y} = f'\left(\frac{y}{x}\right) \cdot \left(\frac{1}{x}\right) \dots\dots\dots (3)$ <p>(2)/(3), we get the required p.d.e $\frac{p}{q} = \frac{-y}{x}$.</p>
4	<p>Obtain the complete solution of the equation $z = px + qy - 2\sqrt{pq}$. BTL1</p> <p>Given: $z = px + qy - 2\sqrt{pq}$</p> <p>This is of the form $z = px + qy + f(p, q)$ [Clairaut’s form]</p> <p>Hence the complete integral is $z = ax + by - 2\sqrt{ab}$.</p>
5	<p>Solve $(D^2 - 2DD' + D'^2)z = 0$. BTL2</p> <p>The A.E. is $m^2 - 2m + 1 = 0$</p> <p>Therefore, the roots are $m = 1, 1$</p>

	Hence $z = f_1(y+x) + xf_2(y+x)$.
6	<p>Solve $(D^4 - D'^4)z = 0$. BTL2</p> <p>The A.E. is $m^4 - 1 = 0$ Therefore, the roots are $m = 1, -1, i, -i$ Hence $z = f_1(y+x) + f_2(y-x) + f_3(y+ix) + f_4(y-ix)$.</p>
7	<p>Find the P.I. of $(D^2 + 4DD')z = e^x$. BTL3</p> <p>P.I. = $\frac{e^x}{D^2 + 4DD'}$</p> <p>↓ put $D=1, D'=0$ $= e^x$.</p>
8	<p>Solve $(D + D' - 2)z = 0$. BTL2</p> <p>Given $(D + D' - 2)z = 0$ $[D - (-1)D' - 2]z = 0$ If $[D - mD' - c]z = 0$ then $z = e^{cx} f(y + mx)$. Therefore, $z = e^{2x} f(y - x)$.</p>
9	<p>Form the partial differential equation by eliminating a and b from $z = a^2 x + a y^2 + b$. BTL3</p> <p>Given $z = a^2 x + a y^2 + b$ Differentiating (1) partially with respect to x, we have $\frac{\partial z}{\partial x} = a^2 \Rightarrow p = a^2$(2) Differentiating (1) partially with respect to y, we have $\frac{\partial z}{\partial y} = 2a y \Rightarrow q = 2a y \Rightarrow a = \frac{q}{2y}$(3) Using (3) in (2), we have $p = \left(\frac{q}{2y}\right)^2 \Rightarrow p = \frac{q^2}{4y^2} \Rightarrow 4p y^2 = q^2$ which is the required partial differential equation.</p>
10	<p>Eliminate the arbitrary function f from $z = f\left(\frac{x}{y}\right)$ and form the pde. BTL2</p> <p>Given $z = f\left(\frac{x}{y}\right)$ ----- (1)</p> <p>Differentiating (1) partially with respect to y, we have $\frac{\partial z}{\partial y} = f'\left(\frac{y}{x}\right)\left[-\frac{y}{x^2}\right] \Rightarrow q = -\frac{y}{x^2} f'\left(\frac{y}{x}\right)$ ----- (2)</p> <p>Differentiating (1) partially with respect to x, we have</p>

	$\frac{\partial z}{\partial x} = f' \left(\frac{y}{x} \right) \left[\frac{1}{x} \right] \implies p = \frac{1}{x} f' \left(\frac{y}{x} \right) \text{ ----- (3)}$ <p>Equations (2) implies $\frac{q}{p} = \frac{-\frac{y}{x^2} f' \left(\frac{y}{x} \right)}{\frac{1}{x} f' \left(\frac{y}{x} \right)}$</p> $\implies xq = -yp$ <p>$xq + yp = 0$, which is the required partial differential equation.</p>
11	<p>Form the pde by eliminating the arbitrary function from $\phi(x^2 - y^2, z) = 0$. BTL4</p> <p>The given relation is of the form $\phi(u, v) = 0$ where $u = x^2 - y^2$ and $v = z$</p> <p>Hence the required pde is of the form $Pp + Qq = R$</p> <p>Where $P = \frac{\partial u}{\partial y} \frac{\partial v}{\partial z} - \frac{\partial u}{\partial z} \frac{\partial v}{\partial y}$</p> $P = (-2y)(1) - (0)(0) \implies P = -2y$ $Q = \frac{\partial u}{\partial z} \frac{\partial v}{\partial x} - \frac{\partial u}{\partial x} \frac{\partial v}{\partial z}$ $Q = (0)(0) - (2x)(1) \implies Q = -2x$ $R = \frac{\partial u}{\partial x} \frac{\partial v}{\partial y} - \frac{\partial u}{\partial y} \frac{\partial v}{\partial x}$ $R = (2x)(0) - (-2y)(0) \implies R = 0$ <p>Therefore, the required equation is</p> $-2yp - 2xq = 0$ <p>$yp + xq = 0$, which is the required partial differential equation.</p>
12	<p>Find the complete integral of $p + q = 1$. BTL3</p> <p>Given $p + q = 1$</p> <p>This is of the form $F(p, q) = 0$</p> <p>Hence, the complete integral is $z = ax + by + c$ where $a + b = 1$ (ie) $b = 1 - a$</p> <p>Therefore, the complete solution is $z = ax + (1 - a)y + c$.</p>
13	<p>Find the complete integral of $\sqrt{p} + \sqrt{q} = 1$. BTL4</p> <p>Given $\sqrt{p} + \sqrt{q} = 1$</p> <p>This is of the form $F(p, q) = 0$</p> <p>Hence, the complete integral is $z = ax + by + c$ where $\sqrt{a} + \sqrt{b} = 1$ (ie) $\sqrt{b} = 1 - \sqrt{a} \implies b = (1 - \sqrt{a})^2$</p> <p>Therefore, the complete solution is $z = ax + (1 - \sqrt{a})^2 y + c$.</p>
14	<p>Find the complete solution of the partial differential equation $p^3 - q^3 = 0$. BTL1</p> <p>Given $p^3 - q^3 = 0$</p>

	<p>This is of the form $F(p, q) = 0$</p> <p>Hence, the complete integral is $z = ax + by + c$ where $a^3 - b^3 = 0$ (ie) $b = a$</p>
15	<p>Find the complete integral of $p + q = pq$. BTL1</p> <p>Given $p + q = pq$</p> <p>This is of the form $F(p, q) = 0$.</p> <p>Hence the complete integral is $z = ax + by + c$</p> $b = \frac{-a}{1-a}$ $b = \frac{a}{a-1}$ <p>Therefore, the complete solution is $z = ax + \frac{a}{a-1}y + c$.</p>
16	<p>Find the complete integral of $\frac{z}{pq} = \frac{x}{q} + \frac{y}{p} + \sqrt{pq}$. BTL3</p> <p>Solution: Given $\frac{z}{pq} = \frac{x}{q} + \frac{y}{p} + \sqrt{pq}$ -----(1)</p> $(1) \times pq \Rightarrow z = px + qy + pq\sqrt{pq}$ <p>This is of the form $z = px + qy + f(p, q)$</p> <p>Hence, the complete solution is $z = ax + by + ab\sqrt{ab}$</p>
17	<p>Solve $px^2 + qy^2 = z^2$. BTL4</p> <p>Given $px^2 + qy^2 = z^2$</p> <p>This is of Lagrange's type. Here $P = x^2$ $Q = y^2$ $R = z^2$</p> <p>The subsidiary equations are $\frac{dx}{P} = \frac{dy}{Q} = \frac{dz}{R}$</p> $\frac{dx}{x^2} = \frac{dy}{y^2} = \frac{dz}{z^2}$ $\frac{dx}{x^2} = \frac{dy}{y^2} \qquad \frac{dy}{y^2} = \frac{dz}{z^2}$ <p>Integrating, we have</p> $\frac{1}{x} - \frac{1}{y} = a \qquad \frac{1}{y} - \frac{1}{z} = b$ <p>Hence the solution is $\varphi\left(\frac{1}{x} - \frac{1}{y}, \frac{1}{y} - \frac{1}{z}\right) = 0$.</p>
18	<p>Find the general solution of $(4D^2 - 12DD' + 9D'^2)z = 0$. BTL2</p> <p>Auxiliary equation is $4m^2 - 12m + 9 = 0$</p> $(2m-3)(2m-3) = 0$

	$m = \frac{3}{2}, m = \frac{3}{2}$ <p>Hence the solution is $z = \phi_1\left(y + \frac{3}{2}x\right) + x\phi_2\left(y + \frac{3}{2}x\right)$.</p>
19	<p>Solve $(D^3 - 2D^2 D')z = 0$. BTL5</p> <p>The auxiliary equation is $m^3 - 2m^2 = 0$</p> $m^2(m-2) = 0$ $m = 0, 0, 2$ <p>Hence the solution is $z = \phi_1(y) + x\phi_2(y) + \phi_3(y+2x)$.</p>
20	<p>Solve $(D^4 - D'^4)z = 0$. BTL5</p> <p>The auxiliary equation is $m^4 - 1 = 0$</p> $(m^2 + 1)(m^2 - 1) = 0$ $m = 1, -1, i, -i$ <p>Hence the solution is $z = \phi_1(y+x) + \phi_2(y-x) + \phi_3(y+ix) + \phi_4(y-ix)$.</p>
	Part-B
1	<p>Form the partial differential equation by eliminating the arbitrary functions f and ϕ from $z = f(x+t) + \phi(x-t)$. (8 M) BTL2</p> <p>Answer: Page 4.30 – Dr.M. Chandrasekar</p> <ul style="list-style-type: none"> • Find p, q (2 M) • Find the second derivatives r, s and t (2 M) • Obtain the PDE: $r = t$ (4 M)
2	<p>Find the partial differential equation of all planes which are at a constant distance 'a' from the origin. (8 M) BTL2</p> <p>Answer: Page 4.10 – Dr.M. Chandrasekar</p> <ul style="list-style-type: none"> • $\frac{x}{a} + \frac{y}{b} + \frac{z}{c} = 1$ (1 M) • Find p, q (1 M) • Find the second derivatives r, s and t (2 M) • Obtain the PDE $z = px + qy - \frac{pq}{p+q-pq}$ (4 M)
3	<p>Form the partial differential equation by eliminating the arbitrary function ϕ from $\phi(x^2 + y^2 + z^2, ax + by + cz) = 0$. (8 M) BTL2</p> <p>Answer: Page 4.26 – Dr.M. Chandrasekar</p> <ul style="list-style-type: none"> • Find p, q. (4 M) • Obtain the PDE $(cy - bz)p + (az - cx)q = (bx - ay)$ (4 M)
4	<p>Solve $z = px + qy + \sqrt{1 + p^2 + q^2}$. (8 M) BTL4</p> <p>Answer: Page 4.56 – Dr.M. Chandrasekar</p>

	<ul style="list-style-type: none"> • Complete Integral : $z = ax + by + \sqrt{1 + a^2 + b^2}$. (2 M) • Singular integral : $x^2 + y^2 + z^2 = 1$ (4 M) • General solution (2 M)
5	<p>Find the singular integral of $z = px + qy + p^2 + pq + q^2$. (8 M) (Nov/Dec 2017)BTL2 Answer : Page : 4.59 – Dr.M. Chandrasekar</p> <ul style="list-style-type: none"> • Find Complete Integral $z = ax + by + a^2 + ab + b^2$. (4 M) • Find singular integral $3z = xy - x^2 - y^2$ (4 M)
6	<p>Solve $z = px + qy + p^2 - q^2$. (8 M) BTL4 Answer : Page : 4.58 – Dr.M. Chandrasekar</p> <ul style="list-style-type: none"> • Find Complete Integral $z = ax + by + a^2 - b^2$. (2 M) • Find singular integral $4z - y^2 + x^2 = 0$ (2 M) • Obtain the general solution (4 M)
7	<p>Solve $z = px + qy + p^2q^2$. (8 M) BTL4 Answer : Page : 4.60 – Dr.M. Chandrasekar</p> <ul style="list-style-type: none"> • Find Complete Integral $z = ax + py + a^2b^2$ (2 M) • Find singular integral (4 M) • Obtain the general solution (2 M)
8	<p>Solve $p^2 + q^2 = x^2 + y^2$. (8 M) BTL2 Answer : Page :4.77 – Dr.M. Chandrasekar</p> <ul style="list-style-type: none"> • Find Complete Integral. (2 M) • Find singular integral (4 M) • Obtain the general solution (2 M)
9	<p>Solve $(mz - ny)p + (nx - lz)q = ly - mx$. (8 M) BTL4 Answer : Page : 4.106 – Dr.M. Chandrasekar</p> <ul style="list-style-type: none"> • Apply the Lagrange's multipliers method (4 M) • Obtain the solutions $\varphi(x^2 + y^2 + z^2, lx + my + nz) = 0$ (4 M)
10	<p>Solve $x(z^2 - y^2)p + y(x^2 - z^2)q = z(y^2 - x^2)$ (8 M) (June 2016)BTL2 Answer : Page : 4.116 – Dr. A. Singaravelu</p> <ul style="list-style-type: none"> • Apply the Lagrange's multipliers method (4 M) • Obtain the solutions $\varphi(x^2 + y^2 + z^2, xyz) = 0$ (4 M)
11	<p>Solve $x(y - z)p + y(z - x)q = z(x - y)$ (8 M) BTL5 Answer : Page : 4.113 – Dr.A. Singaravelu</p> <ul style="list-style-type: none"> • Apply the Lagrange's multipliers method (4 M) • Obtain the solution $\varphi(x + y + z, xyz) = 0$ (4 M)
12	<p>Find the general solution $(3z - 4y)p + (4x - 2z)q = 2y - 3x$. (8 M) BTL6 Answer : Page : 4. 105 – Dr.M. Chandrasekar</p> <ul style="list-style-type: none"> • Apply the Lagrange's multipliers method (4 M)

	<ul style="list-style-type: none"> Obtain the solutions $\varphi(x^2 + y^2 + z^2, 2x + 3y + 4z) = 0$ (4 M)
13	<p>Solve $x^2(y-z)p + y^2(z-x)q = z^2(x-y)$. (8 M) BTL2 Answer : Page : 4.103 – Dr.M. Chandrasekar</p> <ul style="list-style-type: none"> Apply the Lagrange's multipliers method (4 M) Obtain the solutions $\varphi\left(xyz, \frac{1}{x} + \frac{1}{y} + \frac{1}{z}\right) = 0$ (4 M)
14	<p>Solve $x(y^2 + z^2)p + y(z^2 + x^2)q = z(y^2 - x^2)$. (8 M) BTL5 Answer : Page : 4.108 – Dr.M. Chandrasekar</p> <ul style="list-style-type: none"> Apply the Lagrange's multipliers method (4 M) Obtain the solutions $\varphi\left(x - y + z, \frac{xz}{y}\right) = 0$ (4 M)
15	<p>Find the general solution of $z(x-y) = px^2 - qy^2$. (8 M) BTL2 Answer : Page : 4.112 – Dr.M. Chandrasekar</p> <ul style="list-style-type: none"> Apply the Lagrange's multipliers method (4 M) Obtain the solutions $\varphi\left(\frac{1}{x} + \frac{1}{y}, \frac{x+y}{z}\right)$ (4 M)
16	<p>Find the general solution of $(y-z)p + (z-x)q = x-y$. (8 M) BTL2 Answer : Page : 4.112 – Dr.M. Chandrasekar</p> <ul style="list-style-type: none"> Apply the Lagrange's multipliers method (4 M) Obtain the solutions $\varphi(x + y + z, x^2 + y^2 + z^2) = 0$ (4 M)
17	<p>Solve $(D^2 - DD' - 20D'^2)z = e^{5x+y} + \sin(4x-y)$. (8 M) (Nov/Dec 2018) BTL2 Answer : Page : 4.169 – Dr.M. Chandrasekar</p> <ul style="list-style-type: none"> Find A.E. and $CF = f_1(y+5x) + f_2(y-4x)$ (3 M) Obtain the $PI = \frac{x}{9}e^{5x+y} - \frac{x}{9}\cos(4x-y)$ (4 M) Obtain the general solution (1 M)
18	<p>Solve $(D^2 - D'^2)z = e^{x-y} \sin(2x+3y)$. (8 M) BTL2 Answer : Page : 4.156 – Dr.M. Chandrasekar</p> <ul style="list-style-type: none"> Find A.E. and $CF = f_1(y+x) + f_2(y-x)$ (3 M) Obtain the $PI = \frac{e^{x-y}}{25} [\sin(2x+3y) - 2\cos(2x+3y)]$ (4 M) Obtain the general solution (1 M)
19	<p>Solve $(D^2 - 2DD' + D'^2)z = x^2 y e^{x+y}$. (8 M) BTL2 Answer : Page : 4.155 – Dr.M. Chandrasekar</p> <ul style="list-style-type: none"> Find A.E. and $CF = f_1(y+x) + x f_2(y+x)$ (3 M) Obtain the $PI = e^{x+y} \left[\frac{x^4 y^2}{12} + \frac{x^5 y}{15} + \frac{x^6}{60} \right]$ (4 M) Obtain the general solution (1 M)

20	<p>Solve $\frac{\partial^2 z}{\partial x^2} - 7 \frac{\partial^2 z}{\partial x \partial y} + 6 \frac{\partial^2 z}{\partial y^2} = \sinh(x+y) + xy$. (8 M) BTL2</p> <p>Answer : Page :4.149 – Dr.M. Chandrasekar</p> <ul style="list-style-type: none"> • A.E. and $CF = f_1(y+6x) + f_2(y+x)$ (3 M) • Obtain the $PI = \frac{x^3}{24}[4y+7x]$. (4 M) • Obtain the general solution (1 M)
21	<p>Solve $(D^2 + DD' - 2D'^2)z = y \sin x$. (8 M) BTL2</p> <p>Answer : Page : 4.160 – Dr.M. Chandrasekar</p> <ul style="list-style-type: none"> • Find A.E. and C.F $CF = f_1(y-2x) + f_2(y+x)$ (3 M) • Obtain the P.I. $PI = -y \sin x - \cos x$ (4 M) • Obtain the general solution (1 M)
22	<p>Solve $(D^2 + D'^2 + 2DD' + 2D + 2D' + 1)z = e^{2x+y}$. (8 M) BTL2</p> <p>Answer : Page : 4.188 – Dr.M. Chandrasekar</p> <ul style="list-style-type: none"> • Find A.E. and C.F $CF = e^{-x} f_1(y-x) + x e^{-x} f_2(y-x)$ (3 M) • Obtain the P.I. $PI = \frac{e^{2x+y}}{16}$ (4 M) • Obtain the general solution (1 M)
23	<p>Solve $(D^2 - D'^2 - 3D + 3D')z = xy + 7$. (8 M) BTL2</p> <p>Answer : Page :4.189 – Dr.M. Chandrasekar</p> <ul style="list-style-type: none"> • Find A.E. and C.F. $CF = f_1(x+y) + e^{3x} f_2(y-x)$ (3 M) • Obtain the P.I. $\frac{-1}{3} \left(\frac{x^2 y}{2} + \frac{xy}{3} + \frac{x^3}{6} + \frac{x^2}{3} + \frac{65x}{9} \right)$ (4 M) • Obtain the general solution (1 M)
24	<p>Solve $(D^2 - DD')$ $z = \sin x \cdot \sin 2y$. (8 M) BTL2</p> <p>Answer : Page : 4.145 – Dr.M. Chandrasekar</p> <ul style="list-style-type: none"> • Find A.E. and C.F. $CF = f_1(y) + f_2(x+y)$ (3 M) • Obtain the P.I. $PI = \frac{-\cos(x-2y)}{6} - \frac{\cos(x+2y)}{2}$ (4 M) • Obtain the general solution $y = f_1(y) + f_2(x+y) - \frac{\cos(x-2y)}{6} - \frac{\cos(x+2y)}{2}$ (1 M)

25	<p>Solve $(D^3 + D^2D' - 4DD'^2 - 4D'^3)z = e^{2x+y} + \cos(2x+y)$ (8 M) BTL2</p> <p>Answer : Page :4.170 – Dr.M. Chandrasekar</p> <ul style="list-style-type: none"> • Find A.E. and C.F, $CF = f_1(y+x) + f_2(y-x) + xf_3(y-x)$ (3 M) • Obtain the P.I. $PI = \frac{e^{2x+y}}{9} - \frac{x \cos(x+y)}{4}$ (4 M) • Obtain the general solution (1 M)
----	--

UNIT V – FOURIER SERIES SOLUTIONS OF PARTIAL DIFFERENTIAL EQUATIONS	
Dirichlet's conditions – General Fourier series – Half range sine and cosine series - Method of separation of variables – Solutions of one dimensional wave equation and one-dimensional heat equation – Steady state solution of two-dimensional heat equation – Fourier series solutions in Cartesian coordinates.	
Q.No.	Part-A
1.	<p>Write down all possible solutions of one dimensional wave equation. BTL2</p> <p>(i) $y(x, t) = (c_1 e^{px} + c_2 e^{-px})(c_3 e^{pat} + c_4 e^{-pat})$</p> <p>(ii) $y(x, t) = (c_5 \cos px + c_6 \sin px)(c_7 \cos pat + c_8 \sin pat)$</p> <p>(iii) $y(x, t) = (c_9 x + c_{10})(c_{11} t + c_{12})$</p>
2	<p>Classify the PDE $4u_{xx} = u_t$. BTL4</p> <p>Given $4u_{xx} - u_t = 0$.</p> <p>Here $A = 4, B = 0, C = 0$ then $B^2 - 4AC = 0$</p> <p>Therefore the given PDE is <i>parabolic</i>.</p>
3	<p>Classify the PDE $x^2 u_{xx} + 2xy u_{xy} + (1 + y^2) u_{yy} - 2u_x = 0$. BTL3</p> <p>Given $x^2 u_{xx} + 2xy u_{xy} + (1 + y^2) u_{yy} - 2u_x = 0$</p> <p>Here $A = x^2, B = 2xy, C = 1 + y^2$ then $B^2 - 4AC = -4x^2 < 0$</p> <p>Therefore the given PDE is <i>Elliptic</i>.</p>
4	<p>A rod 20cm long with insulated sides has its ends A and B kept at 30°C and 90°C respectively. Find the steady state temperature distribution of the rod. BTL4</p> <p>When steady state condition exists the heat flow equation is $u_{xx} = 0$.</p> <p><i>i.e., $u(x) = ax + b$ (1)</i></p> <p>The boundary conditions are</p> <p>(i) $u(0) = 30$</p> <p>(ii) $u(20) = 90$</p> <p>Applying (i) and (ii) in (1), we get $a = 3, b = 30$</p> <p>Therefore the required steady state equation is $u = 3x + 30$.</p>
5	<p>What is the basic difference between the solutions of one dimensional wave equation and one dimensional heat equation? BTL2</p> <p>Solution of the one dimensional wave equation is of periodic in nature. But Solution of the one dimensional heat equation is not of periodic in nature.</p>
6	<p>Classify the PDE $u_{xx} + 2u_{xy} + u_{yy} = e^{(2x+3y)}$. (Nov/Dec 2018) BTL3</p> <p>Here $A = 1, B = 2, C = 1$</p> <p>$B^2 - 4AC = 0$</p> <p>Then the given PDE is <i>parabolic</i>.</p>
7	<p>In the wave equation $u_{tt} = c^2 u_{xx}$, what does c^2 stand for? BTL2</p> <p>$c^2 = \frac{T}{m} = \frac{\text{Tension}}{\text{mass per unit length}}$</p>

8	What are the basic assumption in 2-d heat equation (or) Laplace equation? BTL2 When the heat flow is along curves instead of straight lines, the curves lying in parallel planes the flow is called two dimensional.
9	State any two laws which are assumed to derive one dimensional heat equation. BTL3 (i) The sides of the bar are insulated so that the loss or gain of heat from the sides by conduction or radiation is negligible. (ii) The same amount of heat is applied at all points of the face.
10	Classify the PDE $u_{xx} + xu_{yy} = 0$. BTL1 Here $A=1, B=0, C=x$ therefore $B^2 - 4AC = -4x$ (i) If $x=0$ then the given PDE is <i>Parabolic</i> (ii) If $x<0$ then the given PDE is <i>Elliptic</i> (iii) If $x>0$ then the given PDE is <i>Hyperbolic</i>
11	Define steady state temperature distribution. BTL2 If the temperature will not change when time varies is called steady state temperature distribution.
12	In one dimensional heat equation $u_t = \alpha^2 u_{xx}$. What does α^2 stands for? BTL1 $\alpha^2 =$ thermal diffusivity.
13	State Dirichlet's conditions for a given function to expand in Fourier series. BTL4 A function $f(x)$ defined in $c \leq x \leq c + 2l$ can be expanded as an infinite trigonometric series of the form $\frac{a_0}{2} + \sum_{n=1}^{\infty} a_n \cos\left(\frac{n\pi}{l}\right)x + \sum_{n=1}^{\infty} b_n \sin\left(\frac{n\pi}{l}\right)x$ provided (i) $f(x)$ is single-valued and finite in $(c, c + 2l)$ (ii) $f(x)$ is continuous or piecewise continuous with finite number of finite discontinuities in $(c, c + 2l)$. $f(x)$ has no or finite number of maxima or minima in $(c, c + 2l)$.
14	State Euler's formula for Fourier coefficients of a function defined in $(c, c + 2l)$. BTL2 If a function $f(x)$ defined in $(c, c + 2l)$ can be expanded as the infinite trigonometric series $\frac{a_0}{2} + \sum_{n=1}^{\infty} a_n \cos\left(\frac{n\pi}{l}\right)x + \sum_{n=1}^{\infty} b_n \sin\left(\frac{n\pi}{l}\right)x$, then $a_0 = \frac{1}{l} \int_c^{c+2l} f(x) dx$ $a_n = \frac{1}{l} \int_c^{c+2l} f(x) \cos\left(\frac{n\pi}{l}\right)x dx$ $b_n = \frac{1}{l} \int_c^{c+2l} f(x) \sin\left(\frac{n\pi}{l}\right)x dx$
15	Does $f(x) = \tan x$ possess a Fourier series expansion? BTL5

	No, $f(x) = \tan x$ does not possess a Fourier expansion. Because $f(x) = \tan x$ has an infinite discontinuity. (ie) Dirichlet's condition is not satisfied.
16	<p>If $x^2 = \frac{\pi^2}{3} - 4 \sum_{n=1}^{\infty} (-1)^{n+1} \frac{\cos nx}{n^2}$ in $-\pi < x < \pi$, then find $\sum_{n=1}^{\infty} \frac{1}{n^2}$. BTL5</p> <p>Given $x^2 = \frac{\pi^2}{3} - 4 \sum_{n=1}^{\infty} \frac{(-1)^{n+1}}{n^2} \cos nx$</p> $x^2 = \frac{\pi^2}{3} - 4 \left[\frac{1}{1^2} \cos x - \frac{1}{2^2} \cos 2x + \frac{1}{3^2} \cos 3x + \dots \right]$ <p>The point $x = \pi$ is the point of discontinuity (right extreme point)</p> $\pi^2 = \frac{\pi^2}{3} - 4 \left[\frac{1}{1^2} \cos \pi - \frac{1}{2^2} \cos 2\pi + \frac{1}{3^2} \cos 3\pi + \dots \right]$ $\frac{2\pi^2}{3} = 4 \left[\frac{1}{1^2} + \frac{1}{2^2} + \frac{1}{3^2} + \dots \right]$ $\frac{\pi^2}{6} = \frac{1}{1^2} + \frac{1}{2^2} + \frac{1}{3^2} + \dots$ <p>Therefore, $\frac{1}{1^2} + \frac{1}{2^2} + \frac{1}{3^2} + \dots = \frac{\pi^2}{6}$</p>
17	<p>Find the constant term in the Fourier series corresponding to $f(x) = \cos^2 x$ expressed in $(-\pi, \pi)$.</p> <p>BTL6</p> <p>Given $f(x) = \cos^2 x$</p> $f(x) = (\cos x)^2$ $f(x) = (\cos(-x))^2 = \cos^2 x = f(x)$ <p>Therefore, $f(x)$ is an even function.</p> <p>The constant term in the Fourier series is $\frac{a_0}{2}$ where</p> $a_0 = \frac{2}{\pi} \int_0^{\pi} \cos^2 x dx$ $= \frac{2}{\pi} \int_0^{\pi} \frac{1 + \cos 2x}{2} dx$ $= \frac{1}{\pi} \left[(x)_0^{\pi} + \left(\frac{\sin 2x}{2} \right)_0^{\pi} \right] = \frac{1}{\pi} \left[(\pi - 0) + \frac{1}{2} (0 - 0) \right] = \frac{1}{\pi} (\pi) = 1$ <p>Therefore, the constant term $\frac{a_0}{2}$ is $\frac{1}{2}$.</p>
18	<p>If $f(x) = x^2 + x$ is expressed as a Fourier series in the interval $(-2, 2)$, to which value this series converges at $x = 2$? BTL4</p> <p>Fourier series of $f(x)$ converges at $x = 2$ is $= \frac{f(-2) + f(2)}{2}$</p>

	$= \frac{(-2)^2 - 2}{2} + \frac{2^2 + 2}{2} = \frac{4 - 2 + 4 + 2}{2} = 4.$
19	<p>Find the half range sine series expansion of $f(x) = 1$ in $(0, 2)$. (Nov/Dec 2018) BTL3</p> $f(x) = \sum_{n=1}^{\infty} b_n \sin\left(\frac{n\pi}{l}\right)x$ $f(x) = \sum_{n=1}^{\infty} b_n \sin\left(\frac{n\pi}{2}\right)x$ <p>where $b_n = \frac{2}{l} \int_0^l f(x) \sin\left(\frac{n\pi}{l}\right)x dx = \frac{2}{2} \int_0^2 1 \sin\left(\frac{n\pi}{2}\right)x dx = \int_0^2 \sin\left(\frac{n\pi}{2}\right)x dx$</p> <p>Therefore $f(x) = \sum_{n=1,3,5}^{\infty} \frac{4}{n\pi} \sin\left(\frac{n\pi}{2}\right)x = \frac{4}{\pi} \sum_{n=1,3,5}^{\infty} \frac{1}{n} \sin\left(\frac{n\pi}{2}\right)x.$</p>
20	<p>Find the root mean square value of $f(x) = x(l-x)$ in $0 \leq x \leq l$. BTL2</p> <p>The root mean square value of a function $f(x) = lx - x^2$ in $0 \leq x \leq l$ is given by</p> $\bar{y} = \sqrt{\frac{1}{l-0} \int_0^l [f(x)]^2 dx} = \sqrt{\frac{1}{l} \int_0^l [lx - x^2]^2 dx} = \sqrt{\frac{1}{l} \int_0^l [l^2x^2 + x^4 - 2lx^3] dx}$ $= \sqrt{\frac{1}{l} \left[l^2 \left(\frac{x^3}{3}\right)_0^l + \left(\frac{x^5}{5}\right)_0^l - 2l \left(\frac{x^4}{4}\right)_0^l \right]}$ $= \sqrt{\frac{1}{l} \left[\frac{l^5}{3} + \frac{l^5}{5} - \frac{l^5}{2} \right]} = \sqrt{\frac{1}{l} \left(\frac{l^5}{30} \right)} = \sqrt{\frac{l^4}{30}} = \frac{l^2}{\sqrt{30}}.$
Part-B	
1	<p>Express $f(x) = \frac{(\pi-x)^2}{2}$ as a Fourier Series of period 2π in the interval $0 < x < 2\pi$. Hence deduce the sum of the series $\frac{1}{1^2} + \frac{1}{2^2} + \frac{1}{3^2} + \dots$. (8 M) BTL4</p> <p>Answer : Page :5.12 – Dr.M. Chandrasekar</p> <ul style="list-style-type: none"> • Find $a_0 = \frac{\pi^2}{6}$ (2 M) • Obtain $a_n = \frac{1}{n^2}, b_n = 0$ (5 M) • Deduction Part (1 M)
2	<p>Obtain the Fourier Series of period 2π for the function $f(x) = x^2$ in $(-\pi, \pi)$. Deduce that (i) $\frac{1}{1^2} + \frac{1}{2^2} + \frac{1}{3^2} + \dots$ (ii) $\frac{1}{1^2} - \frac{1}{2^2} + \frac{1}{3^2} - \dots$ (iii) $\frac{1}{1^2} + \frac{1}{3^2} + \frac{1}{5^2} + \dots$ (8 M) BTL5</p> <p>Answer : Page :5.40 – Dr.M. Chandrasekar</p> <ul style="list-style-type: none"> • Find $a_0 = \frac{2\pi^2}{3}, a_n = \frac{4}{n^2}(-1)^n$ & $b_n = 0$ (6 M) • Obtain $f(x)$. (1 M) • Deduction Part (1 M)

3	<p>Obtain the Fourier Series to represent the function $f(x) = x$, $-\pi < x < \pi$ and deduce $\frac{1}{1^2} + \frac{1}{3^2} + \frac{1}{5^2} + \dots = \frac{\pi^2}{8}$. (8 M) BTL4</p> <p>Answer : Page :5.52 – Dr.M. Chandrasekar</p> <ul style="list-style-type: none"> Find $a_0 = \pi$, $a_n = \frac{2[(-1)^n - 1]}{n^2\pi}$ & $b_n = 0$ (6 M) Obtain $f(x)$. (1 M) Deduction Part (1 M)
4	<p>Obtain the Fourier Series of $f(x) = x \sin x$ in $(-\pi, \pi)$. Deduce $\frac{1}{1.3} - \frac{1}{3.5} + \frac{1}{5.7} - \dots$ (8 M) BTL2</p> <p>Answer : Page :5.58 – Dr.M. Chandrasekar</p> <ul style="list-style-type: none"> Find $a_0 = 2$, $a_n = \frac{2(-1)^{n+1}}{(n+1)(n-1)}$, $a_1 = -1/2$ & $b_n = 0$ (6 M) Obtain $f(x)$. (1 M) Deduction Part (1 M)
5	<p>Obtain the Fourier Series of $f(x) = \begin{cases} 1 + \frac{2x}{\pi}, & -\pi \leq x \leq 0 \\ 1 - \frac{2x}{\pi}, & 0 \leq x \leq \pi \end{cases}$ and hence deduce $\frac{1}{1^2} + \frac{1}{3^2} + \frac{1}{5^2} + \dots = \frac{\pi^2}{8}$. (8 M) BTL5</p> <p>Answer : Page :5.72 – Dr.M. Chandrasekar</p> <ul style="list-style-type: none"> Find $a_0 = 0$, $a_n = \frac{8}{n^2\pi^2}$ (n is odd) & $b_n = 0$ (6 M) Obtain $f(x)$. (1 M) Deduction Part (1 M)
6	<p>If $f(x) = \begin{cases} 0, & -\pi \leq x \leq 0 \\ \sin x, & 0 \leq x \leq \pi \end{cases}$, Prove that $f(x) = \frac{1}{\pi} + \frac{1}{2} \sin x - \frac{2}{\pi} \sum_{n=1}^{\infty} \frac{\cos nx}{4n^2-1}$</p> <p>Hence show that (i) $\frac{1}{1.3} + \frac{1}{3.5} + \frac{1}{5.7} - \dots = \frac{1}{2}$ (ii) $\frac{1}{1.3} - \frac{1}{3.5} + \frac{1}{5.7} - \dots = \frac{\pi-2}{4}$. (8M)BTL4</p> <p>Answer : Page :5.64 – Dr.M. Chandrasekar</p> <ul style="list-style-type: none"> Find $a_0 = \frac{2}{\pi}$, $a_n = \frac{-[(-1)^n + 1]}{\pi(n^2 - 1)}$, $a_1 = 0$, $b_n = 0$ & $b_1 = \frac{1}{2}$ (6 M) Obtain $f(x)$. (1 M) Deduction Part (1 M)
7	<p>Find half range sine series for $f(x) = x(\pi - x)$ in $(0, \pi)$. Deduce $\frac{1}{1^3} - \frac{1}{3^3} + \frac{1}{5^3} - \dots$ (8M)BTL3</p> <p>Answer : Page :5.143 – Dr.M. Chandrasekar</p> <ul style="list-style-type: none"> Find $b_n = \frac{4[1 - (-1)^n]}{n^3\pi}$ (6 M) Obtain $f(x)$. (1 M)

	<ul style="list-style-type: none"> Deduction Part : $x = \frac{\pi}{2}$ (1 M)
8	<p>Find the Fourier series for $f(x) = x + x^2$ in $-\pi < x < \pi$ and find the R.M.S value. (8M)BTL3 Answer : Page :5.41 – Dr.M. Chandrasekar</p> <ul style="list-style-type: none"> Find $a_0 = \frac{2\pi^2}{3}$, $a_n = \frac{4(-1)^n}{n^2}$ & $b_n = \frac{2(-1)^{n+1}}{n}$ (6 M) Obtain $f(x)$. (1 M) RMS Part (1 M)
9	<p>Obtain the Fourier Series of $f(x) = \begin{cases} l-x, & 0 < x \leq l \\ 0, & l \leq x \leq 2l \end{cases}$ and hence deduce $\sum_{n=0}^{\infty} \frac{1}{(2n+1)^2}$ (8M)BTL3 Answer : Page : 5.85 – Dr.M. Chandrasekar</p> <ul style="list-style-type: none"> Find $a_0 = \frac{l}{2}$, $a_n = \frac{l[1-(-1)^n]}{n^2\pi}$ & $b_n = \frac{l}{n\pi}$ (6 M) Obtain $f(x)$. (1 M) Deduction Part: $x = l$ $\sum_{n=0}^{\infty} \frac{1}{(2n+1)^2} = \frac{\pi^2}{8}$ (1 M)
10	<p>Obtain the half range sine series of the function $f(x) = \begin{cases} x, & 0 < x \leq \frac{l}{2} \\ l-x, & \frac{l}{2} \leq x \leq l \end{cases}$ (8M) BTL4 Answer : Page :5.153 – Dr.M. Chandrasekar</p> <ul style="list-style-type: none"> Find $b_n = \frac{4l}{n^2\pi^2} \sin\left(\frac{n\pi}{2}\right)$ (7 M) Obtain $f(x)$ (1 M)
11	<p>Obtain the half range sine series of the function $f(x) = kx(x-l)$ in $0 \leq x \leq l$. (8M)BTL2 Answer : Page :5.133 – Dr.M. Chandrasekar</p> <ul style="list-style-type: none"> Find $b_n = \frac{4kl^2}{n^3\pi^3} [1-(-1)^n]$ (7 M) Obtain $f(x)$ (1 M)
12	<p>A string is stretched and fastened to two points l apart. Motion is started by displacing the string into the form $y = k(lx - x^2)$ from which it is released at time $t = 0$. Find the displacement of any point of the string at a distance x from one end at any time t. (16M)BTL3 Answer : Page :5.191 – Dr.M. Chandrasekar</p> <ul style="list-style-type: none"> General solution (2 M) Find boundary conditions (2 M) Determine the values of unknowns $f(x) = \sum_{n=1}^{\infty} b_n \sin\left(\frac{n\pi}{2}\right)x$ <p>where $b_n = \frac{2}{l} \int_0^l f(x) \sin\left(\frac{n\pi}{l}\right)x dx$ (12 M)</p>

13	<p>A tightly stretched string with fixed end points $x = 0$ and $x = l$ is initially in a position given by $y = y_0 \sin^3(\pi x/l)$. If it is released from rest from this position, find the displacement $y(x, t)$. (16M)BTL2</p> <p>Answer : Page :5.196 – Dr.M. Chandrasekar</p> <ul style="list-style-type: none"> • General solution (2 M) • Find boundary conditions (2 M) • Determine the values of unknowns $f(x) = \sum_{n=1}^{\infty} b_n \sin\left(\frac{n\pi}{2}\right)x$ <p>where $b_n = \frac{2}{l} \int_0^l f(x) \sin\left(\frac{n\pi}{l}\right)x dx$ (12 M)</p>
14	<p>A tightly stretched string of length L is fixed at both ends. The midpoint of the string is displaced by a distance “b” transversely and the string is released from rest in this position. Find the displacement of any point of the string at any subsequent time. (16M)BTL2</p> <p>Answer : Page :5.197 – Dr.M. Chandrasekar</p> <ul style="list-style-type: none"> • General solution (2 M) • Find boundary conditions (2 M) • Determine the values of unknowns $f(x) = \sum_{n=1}^{\infty} b_n \sin\left(\frac{n\pi}{2}\right)x$ <p>where $b_n = \frac{2}{l} \int_0^l f(x) \sin\left(\frac{n\pi}{l}\right)x dx$ (12 M)</p>
15	<p>A taut string of length l has its ends $x = 0, x = l$ fixed. The point where $x = \frac{l}{3}$ is drawn aside a small distance h, the displacement $y(x, t)$ satisfies $\frac{\partial^2 y}{\partial t^2} = a^2 \frac{\partial^2 y}{\partial x^2}$. Determine $y(x, t)$ at any time t. (16M)BTL4</p> <p>Answer : Page :5.200 – Dr.M. Chandrasekar</p> <ul style="list-style-type: none"> • General solution (2 M) • Find boundary conditions (2 M) • Determine the values of unknowns (12 M)
16	<p>A tightly stretched string with fixed end points $x = 0$ and $x = l$ is initially at rest in its equilibrium position. It is set vibrating by giving each point a velocity $\lambda x(l-x)$, find the displacement $y(x, t)$ at any distance x and at any time t. (16M)BTL3</p> <p>Answer : Page : 5.123 - Dr.M. Chandrasekar</p> <ul style="list-style-type: none"> • General solution (2 M) • Find boundary conditions (2 M) • Determine the values of unknowns (12 M)
17	<p>If a string of length l is initially at rest in its equilibrium position and each of its points is given the velocity $\left(\frac{\partial y}{\partial t}\right)_{t=0} = v_0 \sin^3 \frac{\pi x}{l}, 0 < x < l$. Determine the displacement function $y(x, t)$. (16M)BTL5</p> <p>Answer : Page :5.217 – Dr.M. Chandrasekar</p> <ul style="list-style-type: none"> • General solution (2 M) • Find boundary conditions (2 M)

	<ul style="list-style-type: none"> Determine the values of unknowns (12 M)
18	<p>A string is stretched between two fixed points at a distance $2l$ apart and the points of the string are given initial velocities $v = \begin{cases} \frac{cx}{l} \text{ in } 0 < x < l \\ \frac{c}{l}(2l-x) \text{ in } l < x < 2l \end{cases}$, where x being the distance from an end point. Find the displacement of the string at any time. (16M)BTL5</p> <p>Answer : Page :5.224 – Dr.M. Chandrasekar</p> <ul style="list-style-type: none"> General solution (2 M) Find boundary conditions (2 M) Determine the values of unknowns (12 M)
19	<p>A rod of length l has its ends A and B kept at 0°C and 100°C until steady state condition prevail. If the temperature at B is suddenly reduced to 0°C and kept so while that of A is maintained, find the temperature $u(x,t)$ at a distance x from A at time t. (16M)BTL5</p> <p>Answer : Page :5.255 – Dr.M. Chandrasekar</p> <ul style="list-style-type: none"> General solution (2 M) Find boundary conditions (2 M) Determine the values of unknowns (12 M)
20	<p>A rod, 30 cm long has its ends A and B kept at 20°C and 80°C respectively, until steady state conditions prevail. The temperature at each end is then suddenly reduced to 0°C and kept so. Find the resulting temperature function $u(x,t)$ taking $x = 0$ at A. (16M)BTL3</p> <p>Answer : Page :5.239 – Dr.M. Chandrasekar</p> <ul style="list-style-type: none"> General solution (2 M) Find boundary conditions (2 M) Determine the values of unknowns (12 M)
21	<p>A metal bar 10 cm long with insulated sides, has its ends A and B kept at 20°C and 40°C respectively until steady state conditions prevail. The temperature at A is then suddenly raised to 50°C and at the same instant B is lowered to 10°C. Find the subsequent temperature at any point at the bar at any time. (16M)BTL4</p> <p>Answer : Page : 5.250 – Dr.M. Chandrasekar</p> <ul style="list-style-type: none"> General solution (2 M) Find boundary conditions (2 M) Determine the values of unknowns (12 M)
22	<p>The ends A and B of a rod l cm long have their temperatures kept at 30°C and 80°C, until steady state conditions prevail. The temperature of the end B is suddenly reduced to 60°C and that of A is increased to 40°C. Find the temperature distribution in the rod after time t. (16M)BTL4</p> <p>Answer : Page : 5.250 – Dr.M. Chandrasekar</p> <ul style="list-style-type: none"> General solution (2 M) Find boundary conditions (2 M) Determine the values of unknowns (12 M)
23	<p>An infinitely long rectangular plate with insulated surface is 10cm wide. The two long edges and one short edge are kept at zero temperature while the other short edge $x = 0$ is kept at temperature given by</p> $U(x,t) = \begin{cases} 20y \text{ for } 0 \leq y \leq 5 \\ 20(10-y) \text{ for } 5 \leq y \leq 10. \end{cases}$

	<p>Error! Digit expected. Find the steady state temperature distribution in the plate. (16M)BTL5 Answer : Page : 5.277 – Dr.M. Chandrasekar</p> <ul style="list-style-type: none"> • General solution (2 M) • Find boundary conditions (2 M) • Determine the values of unknowns (12 M)
24	<p>An infinitely long rectangular plate with insulated surface is 10cm wide. The two long edges and one short edge are kept at zero temperature while the other short edge $y = 0$ is kept at temperature given by $u = 20x$ for $0 \leq x \leq 5$ $= 20(10 - x)$ for $5 \leq x \leq 10$</p> <p>Find the steady state temperature distribution in the plate. (16M) (Nov/Dec 2018)BTL4 Answer : Page : 5.271 – Dr.M. Chandrasekar</p> <ul style="list-style-type: none"> • General solution (2 M) • Find boundary conditions (2 M) • Determine the values of unknowns (12 M)
25	<p>A long rectangular plate with insulated surface l cm wide. If the temperature along one short edge is $u(x,0) = k(lx - x^2)$ degrees for $0 < x < l$, while the other two long edges as well as the other short edge are kept at 0°C, find the steady state temperature $u(x,y)$. (16M)BTL4 Answer : Page : 5.269 – Dr.M. Chandrasekar</p> <ul style="list-style-type: none"> • General solution (2 M) • Find boundary conditions (2 M) • Determine the values of unknowns (12 M)

EC8393

FUNDAMENTALS OF DATA STRUCTURES IN C

L T P C

3 0 0 3

OBJECTIVES:

- To learn the features of C
- To learn the linear and non-linear data structures
- To explore the applications of linear and non-linear data structures
- To learn to represent data using graph data structure
- To learn the basic sorting and searching algorithms

UNIT I C PROGRAMMING BASICS**9**

Structure of a C program – compilation and linking processes – Constants, Variables – Data Types– Expressions using operators in C – Managing Input and Output operations – Decision Making and Branching – Looping statements. Arrays – Initialization – Declaration – One dimensional and Two-dimensional arrays. Strings- String operations – String Arrays. Simple programs- sorting-searching – matrix operations.

UNIT II FUNCTIONS, POINTERS, STRUCTURES AND UNIONS**9**

Functions – Pass by value – Pass by reference – Recursion – Pointers - Definition – Initialization –Pointers arithmetic. Structures and unions - definition – Structure within a structure - Union -Programs using structures and Unions – Storage classes, Pre-processor directives.

UNIT III LINEAR DATA STRUCTURES**9**

Arrays and its representations – Stacks and Queues – Linked lists – Linked list-based implementation of Stacks and Queues – Evaluation of Expressions – Linked list based polynomial addition.

UNIT IV NON-LINEAR DATA STRUCTURES**9**

Trees – Binary Trees – Binary tree representation and traversals –Binary Search Trees – Applications of trees. Set representations - Union-Find operations. Graph and its representations – Graph Traversals.

UNIT V SEARCHING AND SORTING ALGORITHMS**9**

Linear Search – Binary Search. Bubble Sort, Insertion sort – Merge sort – Quick sort - Hash tables– Overflow handling.

TEXTBOOKS:

1. Pradip Dey and Manas Ghosh, —Programming in C, Second Edition, Oxford University Press, 2011.
2. Ellis Horowitz, Sartaj Sahni, Susan Anderson-Freed, —Fundamentals of Data Structures in C, Second Edition, University Press, 2008.

REFERENCES:

1. Mark Allen Weiss, —Data Structures and Algorithm Analysis in C, Second Edition, Pearson Education, 1996
2. Alfred V. Aho, John E. Hopcroft and Jeffrey D. Ullman, —Data Structures and Algorithms, Pearson Education, 1983.
3. Robert Kruse, C.L.Tondo, Bruce Leung, Shashi Mogalla , — Data Structures and Program Design in C, Second Edition, Pearson Education, 2007
4. Jean-Paul Tremblay and Paul G. Sorenson, —An Introduction to Data Structures with Applications, Second Edition, Tata McGraw-Hill, 1991.

Subject Code: EC8393**Year/Semester: II /03****Subject Name : FUNDAMENTALS OF DATA STRUCTURE IN C****Subject Handler: /Ms.Sonia Jenifer Rayen**

UNIT I - C PROGRAMMING BASICS	
Structure of a C program – compilation and linking processes – Constants, Variables – Data Types– Expressions using operators in C – Managing Input and Output operations – Decision Making and Branching – Looping statements. Arrays – Initialization – Declaration – One dimensional and Two-dimensional arrays. Strings- String operations – String Arrays. Simple programs- sorting-searching – matrix operations.	
PART * A	
1	<p>What are the different data types available in “C”? BTL1(NOV/DEC 2018)</p> <p>There are four basic data types available in “C”.</p> <p>Int, float, char , double</p>
2	<p>What are Keywords? BTL1</p> <p>Keywords are certain reserved words that have standard and pre-defined meaning in “C”. These keywords can be used only for their intended purpose.</p>
3	<p>What is meant by Enumerated data type. BTL1</p> <p>Enumerated data is a user defined data type in C language.</p> <p>Enumerated data type variables can only assume values which have been previously declared.</p> <p>Example :</p> <pre>enum month { jan = 1, feb, mar, apr, may, jun, jul, aug, sep, oct, nov, dec };</pre>
4	<p>Difference between Local and Global variable in C. BTL1</p> <p>Local</p> <p>These variables only exist inside the specific function that creates them. They are unknown to other functions and to the main program. As such, they are normally implemented using a stack. Local variables cease to exist once the function that created them is completed. They are recreated each time a function is executed or called.</p> <p>Global</p> <p>These variables can be accessed (ie known) by any function comprising the program. They are implemented by associating memory locations with variable names. They do not get recreated if the function is recalled.</p>
5	<p>What are Operators? Mention their types in C. BTL1</p> <p>An operator is a symbol that tells the compiler to perform specific mathematical or logical manipulations. C language is rich in built-in operators and provides following type of operators: Arithmetic Operators, Relational Operators, Logical Operators, Bitwise Operator,s Assignment Operators, Misc Operators</p>
6	<p>What is the difference between “=” and “==” operator?</p> <p>Where = is an assignment operator and == is a relational operator.</p>

	<p>Example:</p> <ul style="list-style-type: none"> while (i=5) is an infinite loop because it is a non zero value and while (i==5) is true only when i=5.
7	<p>What is the difference between ++a and a++? ++a means do the increment before the operation (pre increment) a++ means do the increment after the operation (post increment) Example: a=5; x=a++; /* assign x=5*/ y=a; /*now y assigns y=6*/ x=++a; /*assigns x=7*/</p>
8	<p>What is an Abstract Data Type? (Nov 2014) BTL1 An abstract data type (ADT) is a set of operations and mathematical abstractions, which can be viewed as how the set of operations is implemented. Objects like lists, sets and graphs, along with their operation, can be viewed as abstract data types, just as integers, real numbers and Booleans.</p>
9	<p>Mention the advantages of ADT. (May 2014) BTL1</p> <ul style="list-style-type: none"> Modularity Code Reuse Easy to change the implementation
10	<p>What is the difference between while loop and do...while loop? In the while loop the condition is first executed. If the condition is true then it executes the body of the loop. When the condition is false it comes out of the loop. In the do...while loop first the statement is executed and then the condition is checked. The do...while loop will execute at least one time even though the condition is false at the very first time.</p>
11	<p>List out the operations of the list ADT. (May 2006) BTL1 The operations of the list ADT are Insert, Delete, Find, Next, Previous, Make_empty, and Print_list.</p>
12	<p>List out the operations of set ADT? (May 2012) BTL1 Union and Find are the two operations on set ADT.</p>
13	<p>Give the syntax for the "for" loop statement for (Initialize counter; Test condition; Increment / Decrement) { statements; }</p>
14	<p>How to initialize an array? You can initialize array in C either one by one or using a single statement as follows: double balance[5] = {1000.0, 2.0, 3.4, 17.0, 50.0};</p>

15	<p>Give the applications of linked list. (May 2012) BTL2</p> <ul style="list-style-type: none"> • It is used in Polynomial manipulations such as addition, subtraction, multiplication and division. • It is used to implement stack, queue, trees and graphs. • Implement the symbol table in compiler construction. 												
16	<p>What are the merits and demerits in array implementation of a list? (May 2012) BTL4</p> <p>Merits</p> <ul style="list-style-type: none"> • Fast, random access of elements • Memory efficient – very less amount of memory is required <p>Demerits</p> <ul style="list-style-type: none"> • Insertion and deletion operations are very slow since the elements should be moved. • Redundant memory space – difficult to estimate the size of array. 												
17	<p>State the difference between array and linked list. (Nov 2011) BTL4</p> <table border="1" data-bbox="337 730 1487 1331"> <thead> <tr> <th data-bbox="337 730 959 800">Array</th> <th data-bbox="959 730 1487 800">Linked List</th> </tr> </thead> <tbody> <tr> <td data-bbox="337 800 959 888">Size of an array is fixed</td> <td data-bbox="959 800 1487 888">Size of a list is dynamic</td> </tr> <tr> <td data-bbox="337 888 959 961">Memory is allocated from stack</td> <td data-bbox="959 888 1487 961">Memory is allocated from heap</td> </tr> <tr> <td data-bbox="337 961 959 1108">It is necessary to specify the number of elements during declaration (i.e., during compile time).</td> <td data-bbox="959 961 1487 1108">It is not necessary to specify the number of elements during declaration (i.e., memory is allocated during run time).</td> </tr> <tr> <td data-bbox="337 1108 959 1182">It occupies less memory than a linked list for the same number of elements.</td> <td data-bbox="959 1108 1487 1182">It occupies more memory.</td> </tr> <tr> <td data-bbox="337 1182 959 1331">Inserting new elements at the front is potentially expensive because existing elements need to be shifted over to make room.</td> <td data-bbox="959 1182 1487 1331">Inserting a new element at any position can be carried out easily.</td> </tr> </tbody> </table>	Array	Linked List	Size of an array is fixed	Size of a list is dynamic	Memory is allocated from stack	Memory is allocated from heap	It is necessary to specify the number of elements during declaration (i.e., during compile time).	It is not necessary to specify the number of elements during declaration (i.e., memory is allocated during run time).	It occupies less memory than a linked list for the same number of elements.	It occupies more memory.	Inserting new elements at the front is potentially expensive because existing elements need to be shifted over to make room.	Inserting a new element at any position can be carried out easily.
Array	Linked List												
Size of an array is fixed	Size of a list is dynamic												
Memory is allocated from stack	Memory is allocated from heap												
It is necessary to specify the number of elements during declaration (i.e., during compile time).	It is not necessary to specify the number of elements during declaration (i.e., memory is allocated during run time).												
It occupies less memory than a linked list for the same number of elements.	It occupies more memory.												
Inserting new elements at the front is potentially expensive because existing elements need to be shifted over to make room.	Inserting a new element at any position can be carried out easily.												
18	<p>List out the advantages and disadvantages of linked list over arrays. (Nov 2011) BTL4</p> <p>Advantages</p> <ol style="list-style-type: none"> It is not necessary to specify the number of elements in a linked list during its declaration Linked list can grow and shrink in size depending upon the insertion and deletion that occurs in the list. Insertions and deletions at any place in a list can be handled easily and efficiently A linked list does not waste any memory space <p>Disadvantages</p> <ol style="list-style-type: none"> Searching a particular element in a list is difficult and time consuming A linked list will use more storage space than an array to store the same number of elements 												
	<p>PART * B</p>												
1.	<p>Explain the array implementation of a list and perform create, insert, delete, find and display operations. (13M) BTL3</p> <p>Answer : Page : 9 to 11 - Sartaj Sahni</p> <ul style="list-style-type: none"> • Definition of array and its operations (3 M) <p>An Array is a data structure which can store a fixed-size sequential collection of elements of the</p>												

	<p>same type.</p> <ul style="list-style-type: none"> • Create, Insert, Delete, Find And Display algorithm/Routines (2*5=10M) <p>The basic operations supported by an array:</p> <ul style="list-style-type: none"> • Create – To create a list in the array. • Insertion – Adds an element at the given index. • Deletion – Deletes an element at the given index. • Display – Print all the array elements one by one. • Find – Searches an element using the given index or by the value.
2	<p>Illustrate the algorithms to create the singly linked list and perform all the operations on the created list. (13M) (Dec 2016) BTL2</p> <p>Answer : Page : 11 to 13 - Sartaj Sahni</p> <ul style="list-style-type: none"> • Definition of Singly Linked List and its operations (3 M) <p>A singly linked list is a list structure in which each node contains a single pointer field that points to the next node in the list, along with a data field.</p> <ul style="list-style-type: none"> • Create, Insert, Delete And Display Algorithm /Routines (2.5*4=10M) <p>The basic operations carried out in a singly linked list include:</p> <ul style="list-style-type: none"> • Create – to create a new list. • Insert – to add new element in the list • Delete – to delete a element in the list • display – to print the elements in the list
3	<p>Write C code for circular linked list with create, insert, delete and display operations using structure pointer. (13M) (May 2015) BTL2</p> <p>Answer : Page : 15 to 17 - Sartaj Sahni</p> <ul style="list-style-type: none"> • Definitions (3 M) <p>Circular linked list is a linked list where all nodes are connected to form a circle. There is no NULL at the end. A circular linked list can be a singly circular linked list or doubly circular linked list.</p> <p>Program</p> <p>The basic operations carried out in a singly linked list include(10 M)</p> <ul style="list-style-type: none"> • Create – to create a new list. • Insert – to add new element in the list • Delete – to delete a element in the list • display – to print the elements in the list
4	<p>Illustrate the necessary algorithms to implement doubly linked list and perform all the operations on the created list. (13M) (Dec 2016) BTL2</p> <p>Answer : Page : 21 to 26 - Sartaj Sahni</p> <ul style="list-style-type: none"> • Definition of doubly Linked List and its operations (3 M) <p>a doubly linked list is a linked data structure that consists of a set of sequentially linked records called nodes. Each node contains two fields, called links, That are references to the previous and to the next node in the sequence of nodes.</p> <ul style="list-style-type: none"> • Create, Insert, Delete And Display Algorithm / Routines (2.5*4=10M) <p>A doubly linked list is a list structure in which each node contains two pointer fields along with a</p>

	<p>data field namely,</p> <p>BLINK – Points to the previous node in the list</p> <p>FLINK – Points to the successive node in the list</p> <p>The basic operations carried out in a doubly linked list include:</p> <ul style="list-style-type: none"> • Create – to create a new list. • Insert – to add new element in the list • Delete – to delete a element in the list • display – to print the elements in the list 				
<p>5</p>	<p>Write a C program to perform addition and multiplication operations on Polynomial using linked list. (13M) (May 15) BTL3</p> <p>Answer : Page : 31 to 34 - Sartaj Sahni Definition of Polynomial (3 M)</p> <p>Each node of the list holds the coefficient and exponent for one term. The terms are kept in order from smallest to largest exponent. Each polynomial also maintains a pointer to the most recently accessed node.</p> <p>Addition Operation Program(5M) Multiplication Operation Program(5 M)</p>				
	<p>Part – C</p>				
<p>1</p>	<p>Compare the following with suitable example. BTL4</p> <ul style="list-style-type: none"> • Linked list and array. (7M) • Singly linked list and doubly linked list. (8M) <p>Answer : Page : 9,35 to 37 - Sartaj Sahni Definitions of Array & Linked List (3M)</p> <p>Array is a data type which is widely implemented as a default type, in almost all the modern programming languages, and is used to store data of similar type. But there are many use cases, like the one where we don't know the quantity of data to be stored, for which advanced data structures are required, and one such data structure is linked list.</p> <p>Linked List vs. Array Comparison (4M)</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 50%; text-align: center;">ARRAY</th> <th style="width: 50%; text-align: center;">LINKED LIST</th> </tr> </thead> <tbody> <tr> <td style="padding: 5px;">Array is a collection of elements of similar data type.</td> <td style="padding: 5px;">Linked List is an ordered collection of elements of same type, which are connected to each other using pointers.</td> </tr> </tbody> </table> <p>Singly linked list Vs doubly linked list Definition of Singly & Doubly linked list (3M)</p> <p>A singly linked list is a linked list where the node contains some data and a pointer to the next node in the list. A doubly linked list is complex type of linked list where the node contains some data and a pointer to the next as well as the previous node in the list</p> <p>Comparison of singly and doubly list(5Marks)</p>	ARRAY	LINKED LIST	Array is a collection of elements of similar data type.	Linked List is an ordered collection of elements of same type, which are connected to each other using pointers.
ARRAY	LINKED LIST				
Array is a collection of elements of similar data type.	Linked List is an ordered collection of elements of same type, which are connected to each other using pointers.				

2	<p>Explain about Bubble sort implementation in detail with example. (15M) BTL2</p> <p>Answer : Page : 37 to 39 - Sartaj Sahni</p> <p>Bubble sort Definition(5 M) Bubble sort is based on the idea of repeatedly comparing pairs of adjacent elements and then swapping their positions if they exist in the wrong order.</p> <p>Algorithm & Example(5+5M)</p> <pre>void bubble_sort(int A[], int n) { int temp; for(int k = 0; k < n-1; k++) { for(int i = 0; i < n-k-1; i++) { if(A[i] > A[i+1]) { // here swapping of positions is being done. temp = A[i]; A[i] = A[i+1]; A[i+1] = temp; } } } }</pre>
3	<p>BINARY SEARCH</p> <pre>#include <stdio.h> void binary_search(); int a[50], n, item, loc, beg, mid, end, i; void main() { printf("\nEnter size of an array: "); scanf("%d", &n); printf("\nEnter elements of an array in sorted form:\n"); for(i=0; i<n; i++) scanf("%d", &a[i]); . printf("\nEnter ITEM to be searched: "); scanf("%d", &item); binary_search(); getch(); }</pre>

```
}  
  
void binary_search()  
{  
    beg = 0; end  
    = n-1;  
    mid = (beg + end) / 2;  
    while ((beg<=end) && (a[mid]!=item))  
    {  
        if (item < a[mid])  
            end = mid - 1;  
        else  
            beg = mid + 1;  
        mid = (beg + end) / 2;  
    }  
    if (a[mid] == item)  
        printf("\n\nITEM found at location %d", mid+1);  
    else  
        printf("\n\nITEM doesn't exist");  
}
```

UNIT II - FUNCTIONS, POINTERS, STRUCTURES AND UNIONS

Functions – Pass by value – Pass by reference – Recursion – Pointers - Definition – Initialization – Pointers arithmetic. Structures and unions - definition – Structure within a structure - Union - Programs using structures and Unions – Storage classes, Pre-processor directives.

PART * A

1 Define Recursion (MAY-2014) BTL1

A function that calls itself is known as recursive function and the process of calling function itself is known as recursion in C programming.

Example:

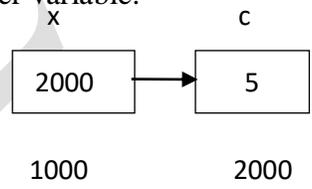
```
void rec()
{
rec();
}
void main()
{
rec();
}
```

2 What is a Pointer? How a variable is declared to the pointer? BTL1

Pointer is a variable which holds the address of another variable.

Pointer declaration:

```
datatype *variable-name;
```



Example:

```
int *x, c=5; x=&c;
```

3 How can you return more than one value from a function? BTL 2

A function returns only one value. By using pointer we can return more than one value. If we want the function to return multiple values of same data types, we could return the pointer to array of that data types

4 What is the difference between an array and pointer? BTL4

Array	Pointer
It's a data structure that stores elements of same data type in contiguous memory locations	It's a variable that stores address of another variable
Array declaration: int a[6]; Memory allocation is static	Pointer declaration: int *a; Memory allocation can be dynamic
Array can be initialized at definition. Example int num[] = { 2, 4, 5 }	Pointers can't be initialized at definition
Array elements are accessed using subscripts	Pointers variables can be accessed using indirection operator(*)

5 What is the need for function?(JAN-2014) BTL1

Modularization: Divide complex problems to simple sub problems
Reusability of Code: reuse code rather than developing it from scratch.

	Remove Redundancy: reduce usage of same set of code repeatedly						
6	<p>What is the necessity of a function prototype? BTL2</p> <p>A function prototype tells the compiler what kind of arguments a function is looking to receive and what kind of return value a function is going to give back.</p> <p>This approach helps the compiler ensure that calls to a function are made correctly and that no erroneous type conversions are taking place.</p>						
7	<p>How do you use a pointer to a function? BTL3</p> <p>The format of a function pointer goes like this: <code>return_type (*pointer_name)(parameter_list);</code></p> <pre>#include<stdio.h> int func (int a) { printf("\n a = %d\n",a); return 0; } int main(void) { <i>int(*fptr)(int); // Function pointer</i> <i>fptr = func; // Assign address to function pointer</i> func(2); return 0; }</pre>						
8	<p>What is the difference between call by value and call by reference? (MAY-2014) BTL2</p> <table border="1"> <thead> <tr> <th>Call by Value</th> <th>Call by Reference</th> </tr> </thead> <tbody> <tr> <td>The value of variables are passed as parameters in the function call</td> <td>The address of the variables are passed as parameters in the function call</td> </tr> <tr> <td>Changes made in the formal parameters (in called function) will not affect the actual arguments in the calling function</td> <td>Changes made in the formal parameters (in called function) will affect the actual arguments in the calling function</td> </tr> </tbody> </table>	Call by Value	Call by Reference	The value of variables are passed as parameters in the function call	The address of the variables are passed as parameters in the function call	Changes made in the formal parameters (in called function) will not affect the actual arguments in the calling function	Changes made in the formal parameters (in called function) will affect the actual arguments in the calling function
Call by Value	Call by Reference						
The value of variables are passed as parameters in the function call	The address of the variables are passed as parameters in the function call						
Changes made in the formal parameters (in called function) will not affect the actual arguments in the calling function	Changes made in the formal parameters (in called function) will affect the actual arguments in the calling function						
9	<p>What is return statement? BTL2</p> <p>A return statement returns result of computations performed in called function and transfers the program control back to the calling function, assigns returned value to the variable in the left side of the calling function. If a function does not return a value, the return type in the function definition and declaration is specified as void.</p> <p>Two forms:</p> <pre>return;</pre> <pre>return expression;</pre>						
10	<p>What is a structure? BTL2</p> <ul style="list-style-type: none"> It's a User defined data type Can hold many data objects of different data types (heterogeneous) may contain the integer elements, float elements and character elements. etc. 						

	<ul style="list-style-type: none"> • Collection of variables under single name • Can conveniently used to represent a record
11	<p>Give syntax for structure definition BTL4 Syntax:</p> <pre><i>[storage class specifier][data type] struct [structure name]</i> { <i>Data _type memeber_name[, member name 2,..];</i> <i>Data _type memeber_name[, member name 2,..];</i> } <i>[variable name];</i></pre> <p>Example:</p> <pre>struct Books { char title[50]; char author[50]; char subject[100]; int book_id; } book;</pre>
12	<p>Define structure declaration. BTL2</p> <ul style="list-style-type: none"> • Variables/constants for structure types can be declared at definition or after definition • <i>[storage class specifier] struct named_Structure-type identifier name [=initialization list];</i> • Struct key word mandatory • A structure must end with a semicolon <p>Example: Declare variables Book1,Book2 of type Books</p> <pre>struct Books Book1; struct Books Book2;</pre>
13	<p>Write the rules for declaring a structure. BTL3</p> <ul style="list-style-type: none"> • A structure must end with a semicolon • Struct key word mandatory • Each structure member must be terminated. • The structure variable must be accessed with dot(.) operator. • Structure decaoration list (structure members): • Can have char, float, double, int, array[], pointer* other structure types • Cannot have void, function type, same structure instance • Can have pointer to an instance of itself which is called as self referential structures.
14	<p>Differentiate between array and structure. BTL4</p>

	<p>Array</p> <p>An array is a collection of variables of same data type</p> <p>An array is a derived data type</p> <p>The individual data members of an array can be initialized.</p> <p>Array elements can be accessed by indexing the array name.</p>	<p>Structure</p> <p>A structure is a collection of variables of different data types</p> <p>It is a user defined data type.</p> <p>The individual data members of the structure cannot be initialized.</p> <p>Structure members can be accessed using dot operator / arrow operator</p>															
15	<p>Give rules for initializing structure. BTL3</p> <ul style="list-style-type: none"> The individual data members of the structure cannot be initialized. The structure variables can be initialized at compile time only. The order of data members in a structure must match the order of values in enclosed brackets We can initialize only some of the data members of the structure. The uninitialized data members can be initialized by default with zero(0) for int and float 0.0 and '\0' for character and strings. 																
16	<p>Define Union. BTL2</p> <ul style="list-style-type: none"> It's a user defined data types Same as a structure in definition, declaration, usage and performing operations <p><u>Difference:</u></p> <ul style="list-style-type: none"> Keyword union must be used while definition and declaration In Union all members of an object share same memory In Structures each member is allocated separate memory 																
17	<p>Give the comparison between union and structure. (JAN-2014) BTL3 (NOV/DEC 2018)</p> <table border="1"> <thead> <tr> <th>Structure</th> <th>Union</th> </tr> </thead> <tbody> <tr> <td>1.The keyword struct is used to define a structure</td> <td>1. The keyword union is used to define a union.</td> </tr> <tr> <td>2. Each member within a structure is assigned separate storage area of location.</td> <td>2. Memory allocated is shared by individual members of union.</td> </tr> <tr> <td>3. The address of each member will be different</td> <td>3. The address is same for all the members</td> </tr> <tr> <td>4 Altering the value of a member will not affect other members of the structure.</td> <td>4. Altering the value of any of the member will alter other member values.</td> </tr> <tr> <td>5. Individual member can be accessed at a time</td> <td>5. Only one member can be accessed at a time.</td> </tr> <tr> <td>6. Several members of a structure can initialize at once.</td> <td>6. Only the first member of a union can be initialized.</td> </tr> </tbody> </table>			Structure	Union	1.The keyword struct is used to define a structure	1. The keyword union is used to define a union.	2. Each member within a structure is assigned separate storage area of location.	2. Memory allocated is shared by individual members of union.	3. The address of each member will be different	3. The address is same for all the members	4 Altering the value of a member will not affect other members of the structure.	4. Altering the value of any of the member will alter other member values.	5. Individual member can be accessed at a time	5. Only one member can be accessed at a time.	6. Several members of a structure can initialize at once.	6. Only the first member of a union can be initialized.
Structure	Union																
1.The keyword struct is used to define a structure	1. The keyword union is used to define a union.																
2. Each member within a structure is assigned separate storage area of location.	2. Memory allocated is shared by individual members of union.																
3. The address of each member will be different	3. The address is same for all the members																
4 Altering the value of a member will not affect other members of the structure.	4. Altering the value of any of the member will alter other member values.																
5. Individual member can be accessed at a time	5. Only one member can be accessed at a time.																
6. Several members of a structure can initialize at once.	6. Only the first member of a union can be initialized.																

18	<p>Declare the Structure with an example. BTL2</p> <pre>struct Books { char title[50]; char author[50]; char subject[100]; int book_id; } b1,b2;</pre>
19	<p>Declare the Union with an example. BTL2</p> <pre>union Books { char title[50]; char author[50]; char subject[100]; int book_id; } b1,b2;</pre>
20	<p>Write any two preprocessor directives in C.(JAN-2014) BTL4</p> <ul style="list-style-type: none"> • Macro Replacement Directive (#define,#undef) • Source File Inclusion Directive (#include) • Line Directive (#line) • Error Directive (#error)
21	<p>Give the rules for defining preprocessor. BTL2</p> <ul style="list-style-type: none"> • # pound symbol used before preprocessor directive • # must be first character in source file or first non white space character in a line • New line character ends preprocessor directive • Only single space/tab space allowed between preprocessing tokens • Can appear anywhere in program but generally paced in beginning of program • The preprocessor cannot have termination with semicolon.
22	<p>What are self referential structures? BTL2</p> <p>A structure consisting of at least a pointer member pointing to the same structure is known as self-referential structure.</p> <p>Example:</p> <pre>struct Books</pre>

	<pre> { int book_id; struct Books* ptr; //ptr is a pointer pointing to structure type Books }; </pre>						
23	<p>What is meant by Preprocessor Directives? BTL2</p> <ul style="list-style-type: none"> • Preprocessor is controlled by directives (commands) known as Preprocessor Directives • Preprocessor directives are not part of C language • It consists of various preprocessing tokens • Begins with pound symbol(#) 						
24	<p>Difference between Storage class and data type. BTL3</p> <table border="1"> <thead> <tr> <th>Data type</th> <th>Storage class</th> </tr> </thead> <tbody> <tr> <td>It refers to the type of information represented by a variable</td> <td>It refers to the scope and lifetime of the variable within the program</td> </tr> <tr> <td>Example: int, char, float</td> <td>Example: register, static, extern</td> </tr> </tbody> </table>	Data type	Storage class	It refers to the type of information represented by a variable	It refers to the scope and lifetime of the variable within the program	Example: int, char, float	Example: register, static, extern
Data type	Storage class						
It refers to the type of information represented by a variable	It refers to the scope and lifetime of the variable within the program						
Example: int, char, float	Example: register, static, extern						
25	<p>What is the purpose of Unions in C? (MAY-2014) BTL2</p> <p>The purpose of union is to save memory by using the same memory region for storing different objects at different times. Unions provide an efficient way of using the same memory location for multi-purpose.</p>						
26	<p>What is the use of pre-processor directives? (MAY-2014) BTL2</p> <ul style="list-style-type: none"> • It makes programs easier to develop, • easier to read, • easier to modify • C code more transportable between different machine architectures. 						
27	<p>What is the use of #define processor? (DEC 2014) BTL2</p> <p>#define directive is used to define Macros –which are tokens that can be replaced for user defined sequence of characters</p> <p>Syntax:</p> <p><i>#define macro-name replacement-list</i></p>						
	PART * B						
1.	<p>Explain function. Write program on pass by value and pass by reference with example(13M) BTL3</p> <p>Answer : Page : 34 - 37 - Sartaj Sahni</p> <p>A function is a sub-program that contains one or more statements and it performs some task when it is called.</p>						

Types of Functions

- Pre defined or Library functions
- User Defined Functions

Parameter Passing Methods in functions

- Call by value
- Call by reference

Call by value

- Actual argument passed to the formal argument.
- Any changes to the formal argument do not affect the actual argument.

```
#include <stdio.h>
#include<conio.h>
Void swap(int a,int b);
void main()
{
    intx,y;
    printf("\nEnter value of x and y:");
    scanf("%d%d",&x,&y);
    swap(x,y);
    printf("\n\nValues in the Main()-->x=%d,y=%d",x,y);
}

int swap(inta,int b)
{
int c;
c=a;
a=b;
b=c;
printf("\nValues in the Fuction -->x=%d,y=%d",a,b);
}
```

Output

Enter value of x:5

Enter value of y:6

Values in the Function -->x=6,y=5

Values in the Main()-->x=5,y=6

Call by Reference

When, argument is passed using pointer, address of the memory location is passed instead of value.

```
#include <stdio.h>
```

```
void swap(int *a,int *b);
```

```
void main()
```

```
{
```

```
    int num1=5,num2=10;
```

```
    swap(&num1,&num2); /* address of num1 and num2 is passed to swap function */
```

```
    printf("Number1 = %d\n",num1);
```

```
    printf("Number2 = %d",num2);
```

```
}
```

```
void swap(int *a,int *b) /* pointer a and b points to address of num1 and num2 respectively */
```

```
{
```

```
int temp;
```

```
temp=*a;
```

```
*a=*b;
```

```
*b=temp;
```

```
}
```

Output

(13M)

```
Number1 = 10
```

```
Number2 = 5
```

Explain Recursive Function with program and example (13M) (Dec 2016) BTL2

Answer : Page : 41 - 43 - Sartaj Sahni

2

- It is a process of calling the same function itself again and again until some condition is satisfied.

- **Syntax:**

```
func1()
```

```
{
```

```
.....
```

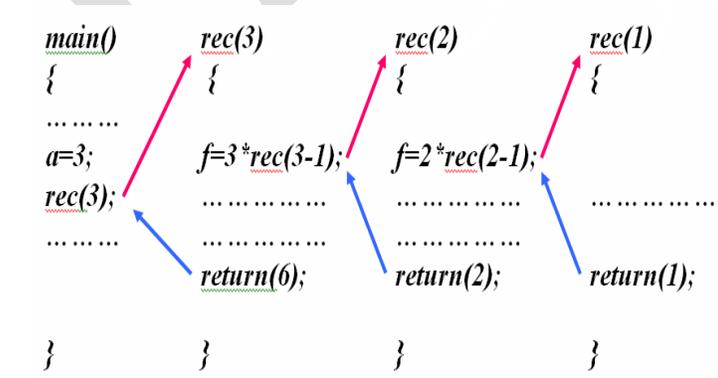
```

        func1();
    }

/* Program for recursive function */
#include<stdio.h>
#include<conio.h>

void main()
{
int a;
int rec(int);
printf("\nEnter the number:");
scanf("%d",&a);
printf("The factorial of %d! is %d",a,rec(a));
}

int rec(int x)
{
int f;
if(x==1)
    return(1);
else
    f=x*rec(x-1);
return(f);
}
    
```



	<p style="text-align: right;">(13M)</p> <p>Output:</p> <p>Enter the number:5</p> <p>The factorial of 5! is 120</p>
3	<p>Explain Pointers with syntax and program with example (13M) (May 2015) BTL2</p> <p>Answer : Page : 45 - 47 - Sartaj Sahni</p> <ul style="list-style-type: none"> • Pointer is a variable that contains the memory address of another variable. <p>Example:</p> <pre> x=5 x Variable 5 Value [] Address 1002 </pre> <p>Example program</p> <pre> #include<stdio.h> #include<conio.h> void main() { int x=5; printf("\n The Address of x = %d",&x); printf("\n The Value of x = %d",x); } </pre> <p>Output</p> <p>The Address of x = 8714</p> <p>The Value of x = 5</p> <p>Pointer Declaration</p> <ul style="list-style-type: none"> • Syntax

data-type *pointer-name;

data-type- Type of the data to which the pointer points.

pointer-name - Name of the pointer

- Example: int *a;

Accessing Variable through Pointer

- If a pointer is declared and assigned to a variable, then the variable can be accessed through the pointer.

- Example:

```
int *a;
```

```
x=5;
```

```
a=&x;
```

```
#include<stdio.h>
```

```
#include<conio.h>
```

```
void main()
```

```
{
```

```
int x=5;
```

```
int *a;
```

```
a=&x;
```

```
printf("\n The Value of x = %d",x);
```

```
printf("\n The Address of x = %u",&x);
```

```
printf("\n The Value of a = %d",a);
```

```
printf("\n The Value of x = %d",*a);
```

```
}
```

```
The Value of x = 5
```

```
The Address of x = 8758
```

```
The Value of a = 8758
```

```
The Value of x = 5
```

Null Pointer

- A pointer is said to be null pointer if zero is assigned to the pointer.

	<ul style="list-style-type: none"> Example <pre>int *a,*b; a=b=0;</pre> <p style="text-align: right;">(13M)</p>
4	<p>Write a C program to find the factorial of a given number (Recursive function) (13M) BTL2</p> <p>Answer : Page : 52 - Sartaj Sahni</p> <pre>#include<stdio.h> #include<conio.h> int rec(int); void main() { int a,fact; printf("\nEnter the number:"); scanf("%d",&a); fact=rec(a); printf("The factorial %d!is %d",a,fact); } int rec(int x) { int f; if(x==1) return(1); else f=x*rec(x-1); return(f); }</pre> <p>Output: Enter the number:5 The factorial of 5! is 120</p>
	Part * C
1	<p>Write a C program for Matrix multiplication(Two dimensional array) (14M) BTL3</p> <p>Answer : Page : 62 - Sartaj Sahni</p> <pre>#include <stdio.h> #include<conio.h> void main() { int m, n, p, q,i,j,k; int first[10][10], second[10][10], multiply[10][10]; printf("Enter the no of rows and columns of first matrix\n");</pre>

```
scanf("%d%d", &m, &n);

printf("Enter the elements of first matrix\n");

for ( i = 0 ; i < m ; i++ )
    for ( j = 0 ; j < n ; j++ )
        scanf("%d", &first[i][j]);

printf("Enter the no of rows and columns of second matrix\n");
scanf("%d%d", &p, &q);

if ( n != p )
    printf("Multiplication not possible\n");
else
{
    printf("Enter the elements of second matrix\n");
    for ( i = 0 ; i < p ; i++ )
        for ( j = 0 ; j < q ; j++ )
            scanf("%d", &second[i][j]);
    for ( i = 0 ; i < m ; i++ )
    {
        for ( j = 0 ; j < q ; j++ )
        {
            for ( k = 0 ; k < p ; k++ )
            {
                multiply[i][j] = multiply[i][j] + first[i][k]*second[k][j];
            }
        }
    }

    printf("Product of entered matrices:-\n");

    for ( i = 0 ; i < m ; i++ )
        for ( j = 0 ; j < q ; j++ )
            printf("%d\t", multiply[i][j]);
```

	<pre>printf("\n"); } getch(); }</pre> <p style="text-align: right;">(14M)</p> <div style="border: 1px solid black; padding: 5px;"> <p>Output:</p> <p>Enter the no of rows and columns of first matrix</p> <p>3 3</p> <p>Enter the elements of first matrix</p> <p>1 1 1 1 1 1 1 1 1</p> <p>Enter the no of rows and columns of second matrix</p> <p>3 3</p> <p>Enter the elements of second matrix</p> <p>1 1 1 1 1 1 1 1 1</p> <p>Product of entered matrices:</p> <p>3 3 3</p> <p>3 3 3</p> <p>3 3 3</p> </div>
2	<p>Write a program for String handling functions in C. (May 2016) (14M) BTL3</p> <p>Answer : Page : 80 - Sartaj Sahni</p> <p>(a)Program to concatenate two strings [strcat()]</p> <pre>#include<stdio.h> #include<conio.h> #include<string.h> void main() { char str1[10],str2[10];</pre>

```
printf("enter the str1");  
gets(str1);  
printf("enter the str2");  
gets(str2);  
strcat(str1,str2);  
printf("concatenated string is %s",str1);  
getch();  
}
```

Output:

```
Enter the str1  hai  
Enter the str2  hello  
Concatenated string is  haihello
```

(b)program to compare two strings [strcmp()]

```
#include<stdio.h>  
#include<conio.h>  
#include<string.h>  
void main()  
{  
char str1[10],str2[10];  
printf("enter the str1");  
gets(str1);  
printf("enter the str2");  
gets(str2);  
if(strcmp(str1,str2)==0)  
printf("Strings are equal");  
else  
printf("strings are not equal");
```

```
getch();  
}
```

Output:

```
Enter the str1  good  
Enter the str2  good  
Strings are equal
```

(c) Program to copy two strings [strcpy()]

```
#include<stdio.h>  
#include<conio.h>  
#include<string.h>  
void main()  
{  
char str1[10],str2[10];  
clrscr();  
printf("enter the str1");  
gets(str1);  
printf("enter the str2");  
gets(str2);  
strcpy(str2,str1);  
printf("copied string str2 is %s",str2);  
getch();  
}
```

Output:

```
Enter the str1  hai  
Enter the str2  hello  
Copied string str2  hai
```

(d)Program to find the length of the string [strlen()]

```
#include<stdio.h>
#include<conio.h>
#include<string.h>
void main()
{
char str1[10];
int len=0;
clrscr();
printf("enter the str1");
gets(str1);
len=strlen(str1);
printf("Length of the string is %d",len);
getch();
}
```

Output:

Enter the str1hello

Length of the string is 5

(e)Program to reverse a given string. [strrev()]

```
#include<stdio.h>
#include<conio.h>
#include<string.h>
void main()
{
char a[10];
clrscr();
printf("enter the string");
scanf("%s",&a);
strrev(a);
printf("\nThe string is %s\n",a);
```

<pre>getch(); }</pre>	<p>Output:</p> <p>Enter the string : computer</p> <p>The reversed string is</p> <p>retupmoc</p> <p>(14M)</p>
---------------------------	--

UNIT III LINEAR DATA STRUCTURES	
Arrays and its representations – Stacks and Queues – Linked lists – Linked list-based implementation of Stacks and Queues – Evaluation of Expressions – Linked list based polynomial addition.	
PART A	
Q.NO	QUESTIONS
1.	Define data structure. (Nov/dec-2016) (BTL 1) The organization, representation and storage of data is called the data structure. Since all programs operate on data, a data structure plays an important role in deciding the final solution for the problem.
2.	Define ADT (Abstract Data Type). What are operations of ADT? What are all not concerned in an ADT? (Nov/Dec 2017)(BTL 1) ADT may be defined as a "class of objects whose logical behavior is defined by a set of values and a set of operations. Abstract data types or ADTs are a mathematical specification of a set of data and the set of operations that can be performed on the data. Union, Intersection, size, complement and find are the various operations of ADT. The definition of an ADT is not concerned with the implementation details at all. It may not even be possible to implement a particular ADT on a particular piece of hardware or using a particular software system.
3.	Write any two data structures used in Operating System (May/June 2013) (BTL 1) <ul style="list-style-type: none"> • Linear list • Tree data structure.
4.	Define linear data structure. (BTL 1) Linear data structures are data structures having a linear relationship between its adjacent elements. A linear data structure traverses the data elements sequentially, in which only one data element can directly be reached. Ex: Arrays, Linked Lists
5.	What is meant by list ADT? (BTL 1) List or sequence is an abstract data type that represents a sequence of values, where the same value may occur more than once. List ADT is a sequential storage structure. General list of the form $a_1, a_2, a_3 \dots a_n$ and the size of the list is 'n'. Any element in the list at the position i is defined to be a_i , a_{i+1} the successor of a_i and a_{i-1} is the predecessor of a_i
6.	Define non-linear data structure. (BTL1) Data structure which is capable of expressing more complex relationship than that of physical adjacency is called non-linear data structure. The elements of data structure do not form a sequence or a linear list Example: Trees, BST (Binary Search Trees) etc.
7.	Explain the usage of stack in recursive algorithm implementation.(BTL 1)

	In recursive algorithms, stack data structures is used to store the return address when a recursive call is encountered and also to store the values of all the parameters essential to the current state of the procedure.		
8.	What is the difference between array and linked list?(BTL 1)		
	Features	Array	Linked list
	Access	elements can be randomly accessed	Elements are accessed Sequentially
	Memory Structure	Elements are stored in contiguous Memory Locations	Element is stored at any available Location, but the Pointer to that memory location is stored in Previous Node.
	Memory Allocation	Memory Should be allocated at Compile-Time	Linked list memory can be allocated at Run-Time
9.	What is the use of header pointer and Null pointer in a linked list?(BTL 1)		
	A linked list contains a pointer, referred as the head pointer, which points to the first node in the list that stores the address of the first node of the list. The final node in the linked list does not point to a next node. If link does not point to a node, its value is set to NULL. NULL pointer is often written 0 it is present in the address field of last node in the list		
10.	What are the advantages and disadvantages of a singly linked list?(BTL 1)		
	<u>ADVANTAGE :-</u>		
	<ul style="list-style-type: none"> ✓ Insertions and Deletions can be done easily. ✓ It does not need movement of elements for insertion and deletion. ✓ Its space is not wasted as we can get space according to our requirements. ✓ Its size is not fixed. ✓ It can be extended or reduced according to requirements. ✓ Elements may or may not be stored in consecutive memory available, even then we can store the data in computer. ✓ It is less expensive. 		
	<u>DISADVANTAGE :-</u>		
	<ul style="list-style-type: none"> ✓ It requires more space as pointers are also stored with information. ✓ Different amount of time is required to access each element. ✓ If we have to go to a particular element then we have to go through all those elements that come before that element. ✓ We cannot traverse it from last & only from the beginning. 		
	It is not easy to sort the elements stored in the linear linked list.		
11.	Define Stack. (Nov/Dec 2012)(BTL 1)		
	Stack is a LIFO (Last In First Out) data structure. A stack is an ordered collection of		

	<p>elements in which insertions and deletions are restricted to one end. The end from which elements are added and/or removed is referred to as top of the stack. Two operations supported are:</p> <ul style="list-style-type: none"> ✓ Push () ✓ Pop()
12.	<p>What is a double linked list? (BTL 1)</p> <p>Doubly linked list is an advanced form of a singly linked list, in which traversal can be done both forward and backward direction. In this each node contains three fields namely,</p> <ul style="list-style-type: none"> ✓ Previous address field. ✓ Data field. ✓ Next address field. <p>The previous address field of a node contains address of its previous node. The data field stores the information part of the node. The next address field contains the address of the next node in the list.</p>
13	<p>Give some applications of stack. (Nov/Dec 2011)(BTL 1)</p> <ul style="list-style-type: none"> ✓ Conversion of infix to postfix ✓ Expression evaluation ✓ Backtracking problem ✓ Towers of Hanoi ✓ Function calls ✓ Evaluation of postfix expression ✓ Balancing symbols ✓ Recursion
14	<p>What is a DEQUEUE? (May/June 2013)(BTL 1)</p> <p>DeQueue or double ended Queue is a data structure in which elements may be added to or deleted from the front or the rear. Like an ordinary queue, a double-ended queue is a data structure it supports the following operations: enq_front, enq_back, deq_front, deq_back, and empty. Dequeue can behave like a queue by using only enq_front and deq_front, and behaves like a stack by using only enq_front and deq_rear.</p>
15	<p>What is the advantages and disadvantages of doubly linked list? (BTL 1)</p> <p><u>ADVANTAGE:-</u></p> <ul style="list-style-type: none"> ✓ We can traverse in both direction i.e from starting to end as well as from end to starting. ✓ It is easy to reverse the linked list. ✓ If we are at a node, then we can go at any node. But in linked list, it is not possible to reach the previous node. <p><u>DISADVANTAGE:-</u></p> <ul style="list-style-type: none"> ✓ It requires more space per node because extra field is required for pointer to

	previous node. ✓ Insertion and Deletion take more time than linear linked list because more pointer operations are required than linear linked list.	
16.	<p>What is a circular queue?(BTL 1)</p> <p>Circular queue is a linear data structure. It follows FIFO principle.</p> <ul style="list-style-type: none"> ✓ In circular queue the last node is connected back to the first node to make a circle. ✓ Circular linked list follows the First In First Out principle ✓ Elements are added at the rear end and the elements are deleted at front end of the queue ✓ <p style="text-align: right;">Both</p> <p>the front and the rear pointers points to the beginning of the array.</p>	
17.	<p>Evaluate the value of the expression $ab+c*d$- using stack. (Nov/Dec 2014)(BTL 5)</p> <ul style="list-style-type: none"> ✓ Stack: a Output: ✓ Stack: a b Output: ✓ Stack: Output: a+b ✓ Stack: (a+b) c Output: ✓ Stack: Output: (a+b)*c ✓ 6. Stack: ((a+b)*c) d Output: 7. Stack: Output: ((a+b)*c) - d 	
18.	Stack	Queue
	Stack is a LIFO (Last In First Out) data structure.	Queue is a FIFO (First In First Out) data structure
	A stack is an ordered collection of elements in which insertions and deletions are restricted to one end. The end from which elements are added and/or removed is referred to as top of the stack.	A Queue is an ordered collection of elements in which insertions are made at one end and deletions are made at the other end.
	Two operations:	Two operations:

	<ul style="list-style-type: none"> ✓ push() ✓ pop() 	<ul style="list-style-type: none"> ✓ enqueue() ✓ dequeue().
	<p>Applications:</p> <ul style="list-style-type: none"> ✓ Conversion of infix to postfix ✓ Expression evaluation ✓ Backtracking problem ✓ Towers of Hanoi. 	<p>When a resource is shared among multiple consumers. Examples include CPU scheduling, Disk Scheduling.</p> <p>When data is transferred asynchronously (data not necessarily received at same rate as sent) between two processes. Examples include IO Buffers, pipes, file IO, etc.</p>
	In stack only one pointer is used: top	In queue two pointers are used: front and rear
19.	<p>What are the postfix and prefix forms of the expression $A+B*(C-D)/(P-R)$?(Nov/Dec 2011)(BTL 1)</p> <p>Postfix form: ABCD-*PR-/+</p> <p>Prefix form: +A/*B-CD-PR</p>	
20.	<p>Give some applications of queue. (Nov/Dec 2011)(BTL 1)</p> <p>Queues have many applications in computer systems. Most computers have only a singly processor, so only one user may be served at a time. Entries from other users are placed in a queue. Each entry gradually advances to the front of the queue as users receive their service. Queues are also used to support print spooling.</p>	
21	<p>Define Queue. How the data are stored in queue. (Nov/Dec 2014)(BTL 1)</p> <p>Queue is a FIFO (First In First Out) data structure. A Queue is an ordered collection of elements in which insertions are made at one end and deletions are made at the other end.</p> <p>The end at which insertions are made is referred to as the rear end, and the end from which deletions are made is referred to as the front end.</p> <p>In queue, the data are inserted only at the front end of the queue and it is pointed using rear pointer. The data's can be accessed sequentially. The elements are to be deleted from the back end of the queue.</p>	
22	<p>List the applications of linked list. (Nov/dec-2016)(BTL 1)</p> <ul style="list-style-type: none"> ✓ Linked lists are used to implement stacks, queues, graphs, etc. ✓ Linked lists let you insert elements at the beginning and end of the list. <p>In Linked Lists we don't need to know the size in advance.</p>	
	<p>What are the advantages of using doubly linked list over singly linked list?(BTL 1)</p>	

23	The advantage of using doubly linked list is, it uses the double set of pointers. One pointing to the next item and other pointing to the preceding item. This allows us to traverse the list in either direction.
24	<p>Define a heap. How can it be used to represent a priority queue? (Nov/Dec 2017)(BTL 1)</p> <ul style="list-style-type: none"> ✓ Heap data structure is a specialized binary tree based data structure. Here, the nodes are arranged based on their value. A heap data structure, sometimes called as Binary Heap. ✓ Heap is generally preferred for priority queue implementation because heaps provide better performance compared to arrays or linked list. When a priority queue is implemented using a heap, the worst-case times for both insert and remove Max are logarithmic in the number of values in the priority queue.
25	<p>List the advantages in the linked list implementation of stack. (April / May 2017)(BTL 1)</p> <ul style="list-style-type: none"> ✓ Stack using linked list is a dynamic data structure so it can grow and shrink at runtime by allocating and de-allocating memory. ✓ Insertion and deletion of nodes in stack are really easier. ✓ Size of linked list can increase or decrease at run time so there is no memory wastage. ✓ Data structures such as stack and queues can be easily implemented using linked list. Implementing a stack using a linked list is particularly easy because all accesses to a stack are at the top.
PART B	
1	<p>What are circular queue? Write an ADT for a circular queue to perform insertion and deletion operations. (Nov/Dec 2012)(13M)(BTL 1)</p> <p>Answer: Page:3.14-Dr.S.Poonkuzhali &P.Revathy</p> <p>Definition: (1M)</p> <ul style="list-style-type: none"> ✓ In circular queue, once the Queue is full the "First" element of the Queue becomes the "Rear" most element, if and only if the "Front" has moved forward. otherwise it will again be a "Queue overflow" state. <div data-bbox="649 1575 1117 1906" style="text-align: center;"> </div>

Figure: Circular Queue having

Rear = 5 and Front = 0

ROUTINE TO INSERT AN ELEMENT IN CIRCULAR QUEUE(3M)

For Insert Operation

- ✓ Insert-Circular-Q(CQueue, Rear, Front, N, Item)
- ✓ Here, CQueue is a circular queue where to store data. Rear represents the location in which the data element is to be inserted and Front represents the location from which the data element is to be removed.
- ✓ Here N is the maximum size of CQueue and finally, Item is the new item to be added. Initially Rear = 0 and Front = 0.

ALGORITHM

- ✓ If Front = 0 and Rear = 0 then Set Front := 1 and go to step 4.
- ✓ If Front = 1 and Rear = N or Front = Rear + 1
- ✓ then Print: "Circular Queue Overflow" and Return.
- ✓ If Rear = N then Set Rear := 1 and go to step 5.
- ✓ Set Rear := Rear + 1
- ✓ Set CQueue [Rear] := Item.
- ✓ Return

ROUTINE:(3M)

```

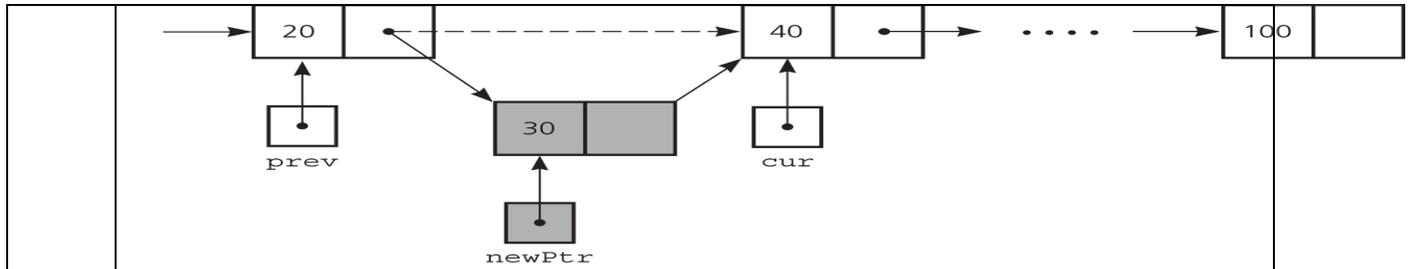
CEnqueue (int X)
{
if (Front == (rear + 1) % Maxsize)
printf("Queue is overflow");
else
{
if (front == -1)
front = rear = 0;
else
rear = (rear + 1) % Maxsize;
CQueue [rear] = X;
}
}

```

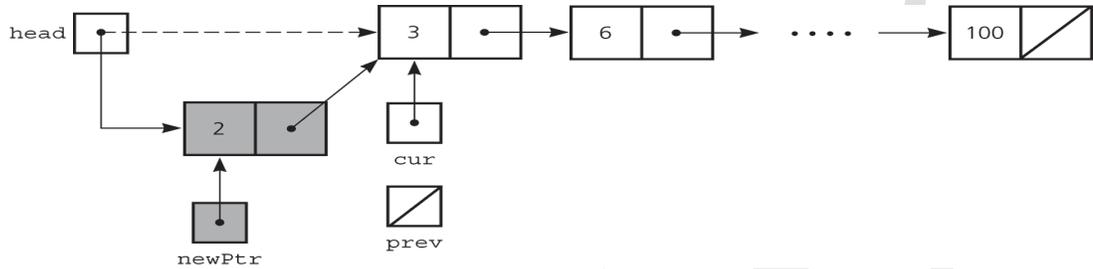
To perform the deletion, the position of the Front pointer is calculated by the relation

- ✓ Value = CQueue [Front]

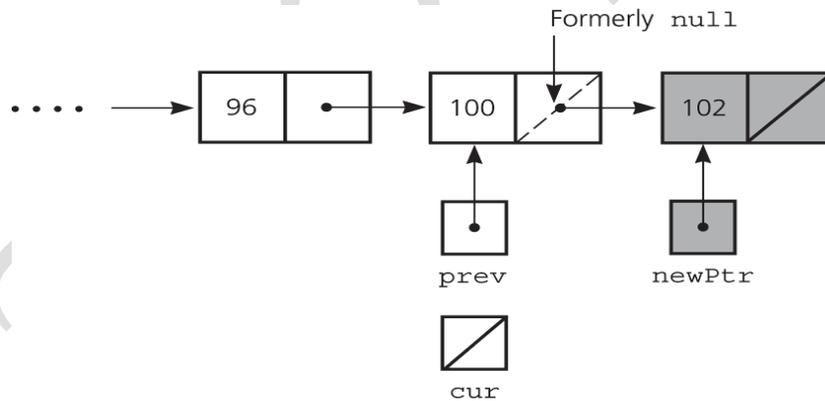
	<p>✓ Front = (Front + 1) % maxsize.</p> <p><u>ROUTINE TO DELETE AN ELEMENT FROM CIRCULAR QUEUE(3M)</u> <u>Delete-Circular-Q(CQueue, Front, Rear, Item)</u></p> <p>Here, CQueue is the place where data are stored. Rear represents the location in which the data element is to be inserted and Front represents the location from which the data element is to be removed. Front element is assigned to Item. Initially, Front = 1.</p> <ul style="list-style-type: none"> ✓ If Front = 0 then ✓ Print: "Circular Queue Underflow" and Return. /* ..Delete without Insertion ✓ Set Item := CQueue [Front] ✓ If Front = N then Set Front = 1 and Return. ✓ If Front = Rear then Set Front = 0 and Rear = 0 and Return. ✓ Set Front := Front + 1 ✓ Return. <p>ROUTINE:(3M) CDequeue () { if (front == -1) printf("Queue is underflow"); else { X = CQueue [Front]; if (Front == Rear) Front = Rear = -1; else Front = (Front + 1)% maxsize; } return (X); }</p>
2	<p>Implement insertion, deletion and search operations in singly linked list. (Nov/Dec 2016, (Nov/Dec 2015)(13M)(BTL 6) Answer: Page:3.4-Dr.S.Poonkuzhali &P.Revathy</p> <p>Definition:(1M)</p> <ul style="list-style-type: none"> ✓ Linked list consists of series of nodes. Each node contains the element and a pointer to its successor node. The pointer of the last node points to NULL. ✓ Insertion and deletion operations are easily performed using linked list. <p>Types of Linked List(2M)</p> <ul style="list-style-type: none"> ✓ Singly Linked List ✓ Doubly Linked List ✓ Circular Linked List. <p>Singly Linked List</p> <ul style="list-style-type: none"> ✓ A singly linked list is a linked list in which each node contains only one link field pointing to the next node in the list. <p>ROUTINE TO INSERT AN ELEMENT IN THE LIST(5M) <i>Insert at intermediate position</i></p>



Insert at the beginning



Insert at the end



Insert a node at the first position

```

void addfirst()
{
node *temp;
temp=(node *)malloc(sizeof(node));
printf("Enter the data...\t");
scanf("%d",&temp->item);
temp->next=head;
head=temp;
}
    
```

Insert a node at the middle position

```

void addmid()
{
int i=1,pos;
node *cur=head,*temp;
printf("\nEnter the position\t");
scanf("%d",&pos);
while(pos!=i+1&&cur!=NULL)
{
cur=cur->next;
i++;
}
if(pos==i+1)
{
temp=(node *)malloc(sizeof(node));
printf("Enter the data...");
scanf("%d",&temp->item);
temp->next=cur->next;
cur->next=temp;
}
}

```

Insert a node at the last position

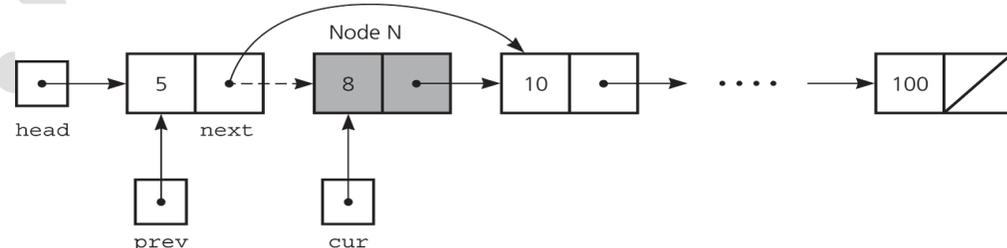
```

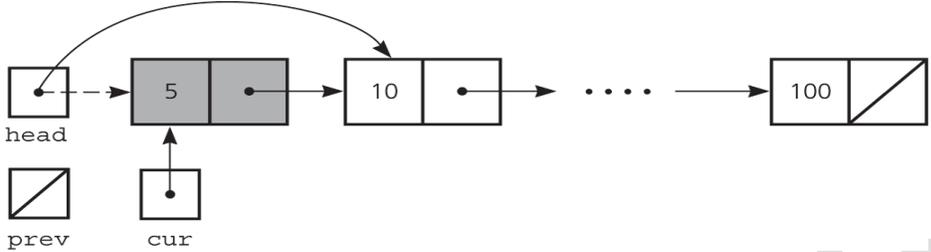
void addlast()
{
node *temp,*cur=head;
temp=(node *)malloc(sizeof(node));
printf("\nEnter the data...");
scanf("%d",&temp->item);
while(cur->next!=NULL)
{
cur=cur->next;
}
temp->next=cur->next;
cur->next=temp;
}

```

ROUTINE TO DELETE AN ELEMENT IN THE LIST (5M)

Deleting intermediate node



	<p>Deleting first node</p> 
3	<p>Explain the operation performed on QUEUE in detail. Write C program to implement these queue operation. (Nov/Dec 2016, May/June 2013)(13M)(BTL2)</p> <p>Answer: Page:3.46-Dr.S.Poonkuzhali &P.Revathy</p> <p>Queue Model(2M)</p> <ul style="list-style-type: none"> ✓ linear data structure which follows First In First Out (FIFO) principle, ✓ insertion performed at rear end and deletion performed at front end. ✓ Example : Waiting Line in Reservation Counter, <p>Operations on Queue(2M)</p> <p>The fundamental operations performed on queue are</p> <ul style="list-style-type: none"> ✓ Enqueue ✓ Dequeue <p>Enqueue : The process of inserting an element in the queue.</p> <p>Dequeue : The process of deleting an element from the queue.</p> <p>PROGRAM: (9M)</p> <pre>#include<stdio.h> #include<conio.h> #define MAXSIZE 20 int q[MAXSIZE]; int front,rear; void main() { void insert(int x); int delete(); void display();</pre>

```
intopt,x;

front=rear=-1;

clrscr();

do

{

printf("\n1.insert\n2.delete\n3.display\n4.exit");

printf("\nenter the option:");

scanf("%d",&opt);

switch(opt)

{

case 1:

{

printf("\ninsert the value in queue:");

scanf("%d",&x);

insert(x);

}

break;

case 2:

{

x=delet();

printf("\ndeleted element in queue=%d",x);

}

break;

case 3:

{

printf("\nthe element in queue are=");
```

```
display();
}
break;
case 4:
break;
default:
printf("\nenter the correct option=");
break;
}
}
while(opt!=4);
getch();
}
void insert(int x)
{
if(rear==MAXSIZE-1)
printf("\nqueue is full");
else
{
rear++;
q[rear]=x;
if(front== -1)
front=0;
}
}
intdelet(int x)
```

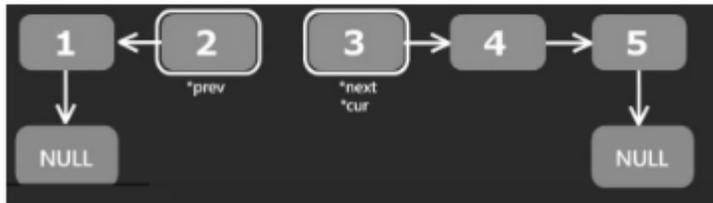
	<pre> { x=q[front]; if(front==rear) front=rear=-1; else front++; return(x); } void display() { int i; if(front==-1) printf("\nqueue is empty"); else { for(i=front;i<=rear;i++) { printf("%d\n",q[i]); } } } </pre>
4	<p>Design an algorithm to reverse the linked list. Trace it with an example. (Nov/Dec 2017)(7M)(BTL6)</p> <p>Answer: Page:3.3-Dr.S.Poonkuzhali &P.Revathy</p> <p>To Reverse The Linked List (1M)</p> <ul style="list-style-type: none"> ✓ Initialize three pointers prev as NULL, curr as head and next as NULL. ✓ Iterate through the linked list. In loop, do following. <p>ROUTINE:(2M)</p> <pre> // Before changing next of current, // store next node next = curr->next // This is where actual reversing happens </pre>

```
curr->next = prev
// Move prev and curr one step forward
prev = curr
curr = next
```

After first step of loop, i.e., after the statement next = curr->next



After one iteration of loop.



Iterative C program to reverse a linked list: (4M)

```
#include<stdio.h>
#include<stdlib.h>

/* Link list node */
struct Node
{
    int data;
    struct Node* next;
};

/* Function to reverse the linked list */
static void reverse(struct Node** head_ref)
{
```

```

struct Node* prev = NULL;

struct Node* current = *head_ref;

struct Node* next = NULL;

while (current != NULL)

{

    next = current->next;

    current->next = prev;

    prev = current;

    current = next;

}

*head_ref = prev;

}

```

ii. Define an efficient representation of two stacks in a given area of memory and explain. (Nov/Dec 2017)(6M)(BTL 2)

```

#include <stdio.h>

#define SIZE 10
int ar[SIZE];
int top1 = -1;
int top2 = SIZE;
//Functions to push data(1M)
void push_stack1 (int data)
{
    if (top1 < top2 - 1)
    {
        ar[++top1] = data;
    }
    else
    {
        printf ("Stack Full! Cannot Push\n");
    }
}
void push_stack2 (int data)
{
    if (top1 < top2 - 1)
    {
        ar[--top2] = data;
    }
    else

```

```
{
printf ("Stack Full! Cannot Push\n");
}
}

//Functions to pop data (3M)
void pop_stack1 ()
{
if (top1 >= 0)
{
intpopped_value = ar[top1--];
printf ("%d is being popped from Stack 1\n",popped_value);
}
else
{
printf ("Stack Empty! Cannot Pop\n");
}
}
void pop_stack2 ()
{
if (top2 < SIZE)
{
intpopped_value = ar[top2++];
printf ("%d is being popped from Stack 2\n",popped_value);
}
else
{
printf ("Stack Empty! Cannot Pop\n");
}
}

//Functions to Print Stack 1 and Stack 2(3M)
void print_stack1 ()
{
int i;
for (i = top1; i >= 0; --i)
{
printf ("%d ", ar[i]);
}
printf ("\n");
}
void print_stack2 ()
{
int i;
for (i = top2; i < SIZE; ++i)
{
printf ("%d ", ar[i]);
}
printf ("\n");
}
```

	<pre> } int main() { intar[SIZE]; int i; intnum_of_ele; printf ("We can push a total of 10 values\n"); //Number of elements pushed in stack 1 is 6 //Number of elements pushed in stack 2 is 4 for (i = 1; i <= 6; ++i) { push_stack1 (i); printf ("Value Pushed in Stack 1 is %d\n", i); } for (i = 1; i <= 4; ++i) { push_stack2 (i); printf ("Value Pushed in Stack 2 is %d\n", i); } //Print Both Stacks print_stack1 (); print_stack2 (); //Pushing on Stack Full printf ("Pushing Value in Stack 1 is %d\n", 11); push_stack1 (11); //Popping All Elements From Stack 1 num_of_ele = top1 + 1; while (num_of_ele) { pop_stack1 (); --num_of_ele; } //Trying to Pop From Empty Stack pop_stack1 (); return 0; } </pre>
5	<p>Explain linear linked implementation of stack and its applications. (Nov/Dec 2017, April/May 2015)(13M) (BTL 3)</p> <p>Answer: Page:3.10-Dr.S.Poonkuzhali &P.Revathy</p>

Stack Model (3M)

- ✓ A stack is a linear data structure which follows Last In First Out (LIFO) principle, in which both insertion and deletion occur at only one end of the list called the Top.
- ✓ Example : -Pile of coins., a stack of trays in cafeteria.

Operations On Stack

The fundamental operations performed on a stack are

- ✓ Push
- ✓ Pop

PUSH :

- ✓ The process of inserting a new element to the top of the stack. For every push operation the top is incremented by 1.

POP :

- ✓ The process of deleting an element from the top of stack is called pop operation. After every pop operation the top pointer is decremented by 1.

EXCEPTIONAL CONDITIONS

- ✓ OverFlow
Attempt to insert an element when the stack is full is said to be overflow.
- ✓ UnderFlow
Attempt to delete an element, when the stack is empty is said to be underflow.

Implementation of Stack

Stack can be implemented using arrays and pointers.

LINKED LIST IMPLEMENTATION OF STACK(5M)

- ✓ Push operation is performed by inserting an element at the front of the list.
- ✓ Pop operation is performed by deleting at the front of the list.
- ✓ Top operation returns the element at the front of the list.

```
#include<stdio.h>
#include<stdlib.h>
typedefstruct node
{
int data;
struct node*link;
}node;
node *top;
Void push(int x)
{
node*t;
t=(node*)malloc(sizeof(node));
t->data=x;
t->link=NULL;
if(top==NULL)
top=t;
else
{
t->link=top;
top=t;
}
printf("\n");
```

```
printf("\n the element is pushed \n");
}
int pop()
{
node*t;
int x;
if (top==NULL)
{
printf("\n");
printf("stack empty \n");
return(-1);
}
else
{
x=top->data;
t=top;
top=top->link;
free(t);
return(x);
}}
void display()
{
node*curr;
curr=top;
while(curr->link!=NULL)
{
printf("\n%d",curr->data);
curr=curr->link;
}
printf("\n %d",curr->data);
}
```

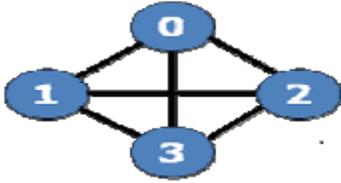
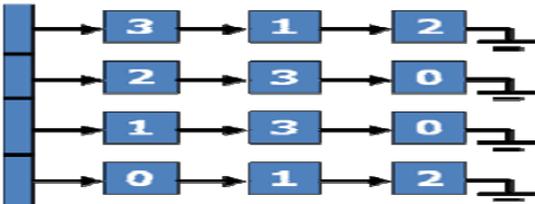
APPLICATIONS OF STACK(5M)

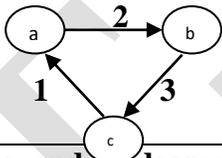
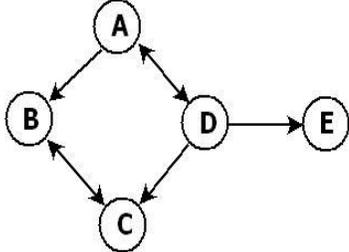
Some of the applications of stack are :

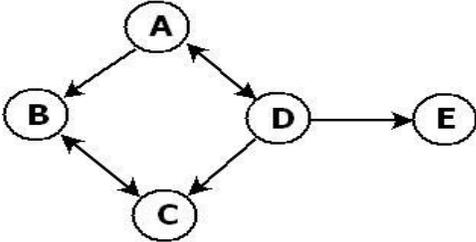
- ✓ Evaluating arithmetic expression
- ✓ Balancing the symbols
- ✓ Towers of Hanoi
- ✓ Function Calls.
- ✓ 8 Queen Problem.

UNIT IV NON- LINEAR DATA STRUCTURES	
Trees – Binary Trees – Binary tree representation and traversals –Binary Search Trees – Applications of trees. Set representations - Union-Find operations. Graph and its representations – Graph Traversals	
PART*A	
Q.NO	QUESTIONS
1.	<p>Define tree. BTL1</p> <p>A tree is an abstract data type (ADT) or data structure which represents hierarchical relationship between individual data items, with a root value and sub trees of children, represented as a set of linked nodes. Tree is a non-linear data structure.</p>
2.	<p>Define height or depth of a tree. BTL1</p> <p>The depth of a node is the number of edges from the node to the tree's root node. A root node will have a depth of 0. The height of a node is the number of edges on the <i>longest path</i> from the node to a leaf. A leaf node will have a height of 0.</p>
3.	<p>Define Binary tree. What are the two ways of representing binary tree?(Nov/Dec-2016) BTL1</p> <p>Binary tree is a tree data structure in which each node has at most two children, which are referred to as the left child and the right child. A binary tree is a finite set of nodes which is either empty or consists of a root and two disjoint binary trees called the left sub tree and the right sub tree. The two representations are,</p> <ul style="list-style-type: none"> ✓ Sequential representation ✓ Linked representation
4.	<p>Define a full binary tree. State some properties of a binary tree. BTL4(NOV/DEC 2018)</p> <p>A full binary tree is a binary tree in which all the leaves are on the same level and every non-leaf node has exactly two children. A full binary tree of a given height h has $2^{h+1} - 1$ nodes. The properties of a binary tree are as follows</p> <ul style="list-style-type: none"> ✓ A binary tree of n elements has $n-1$ edges ✓ Binary tree of height h has at least h and at most $2^h - 1$ elements. ✓ The maximum number of nodes on level n of a binary tree is 2^{n-1}, where $n \geq 1$.
5.	<p>Define Traversal. Give the types of traversal. BTL4</p> <p>One of the most important operations performed on a binary tree is its traversal. Traversing a binary tree means moving through all the nodes in the binary tree, visiting each node in the tree exactly once.</p> <p>There are three different traversal of binary tree.</p>

	<ul style="list-style-type: none"> ✓ In order traversal ✓ Post order traversal ✓ Pre order traversal
6.	<p>Give the code for pre order traversal.(Nov/Dec 2011) BTL5</p> <pre>void preorder(struct tree* t){ if (t==NULL) return; else{ cout<<"\t"<<t->data; preorder(t->left); preorder(t->right); } }</pre>
7.	<p>How to perform union operation? (Nov/Dec 2014) BTL1</p> <p>If a & b are in two different equivalence sets, then Union (a b) should merge those two sets into one Union (a,b) should merge those two sets into one Otherwise, no change.</p> <p>Union by height: Making the shallow tree a sub tree of the deeper tree.</p> <p>Union by size: Making the smaller tree a sub tree of the larger.</p>
8.	<p>What are the applications of binary tree? (Nov/Dec 2012) BTL2</p> <p>Binary tree is used in data processing.</p> <ul style="list-style-type: none"> ✓ File index schemes ✓ Hierarchical database management system
9.	<p>Define equivalence relation. (Nov/Dec 2012) BTL4</p> <p>Equivalence relation is the relation that holds between two elements if and only if they are members of the same cell within a set that has been partitioned into cells such that every element of the set is a member of one and only one cell of the partition. The intersection of any two different cells is empty; the union of all the cells equals the original set. These cells are formally called equivalence classes.</p> <p>Equivalence relation R is a relation that satisfies the following properties</p> <p>Reflexive- a R a for all a belongs to S</p> <p>Symmetric- a R b implies b R a</p>

	Transitive- a R b & b R c implies a R c							
10.	<p>What is a graph? List the two ways to represent a graph. What are the different ways to represent graph? (NOV/DEC 2014)(APRIL/MAY 2016) (APRIL/MAY 2017) BTL2</p> <p>Graph is a non-linear data structure that represents less relationship between its adjacent elements. There is no hierarchical relationship between the adjacent elements in case of graphs.</p> <p>A Graph $G=\{V, E\}$ consists of two sets V & E, where V is a set of vertices and E is a set of Edges. The set E is set of pair of vertices. So each is a pair (v,w) where v,w is an element of V.</p> <p>Two ways of representing a graph are:</p> <ul style="list-style-type: none"> ✓ Adjacency matrix ✓ Adjacency list <p>Consider the graph below:</p>  <p style="text-align: center;">G1</p> <p>Adjacency matrix representation is</p> $\begin{bmatrix} 0 & 1 & 1 & 1 \\ 1 & 0 & 1 & 1 \\ 1 & 1 & 0 & 1 \\ 1 & 1 & 1 & 0 \end{bmatrix}$ <p>Adjacency list representation is</p> 							
11.	<p>Find the maximum number of nodes in complete binary tree if d is the depth? How many trees are possible with 3 nodes? (Nov/Dec 2014) BTL4</p> <p>The maximum number of nodes in a binary tree of depth k is $2^k - 1$, $k \geq 1$.</p> <p>If there are n nodes, there exist 2^{n-1} different trees. $(2^3) - 3 = 3$ trees</p>							
12.	<p>Differentiate between trees and graphs? (Nov/Dec 2014) BTL3</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 25%;">Features</th> <th style="width: 33%;">Trees</th> <th style="width: 42%;">Graph</th> </tr> </thead> <tbody> <tr> <td style="height: 40px;"></td> <td></td> <td></td> </tr> </tbody> </table>		Features	Trees	Graph			
Features	Trees	Graph						

	Path	Tree is special form of graph i.e. minimally connected graph and having only one path between any two vertices.	In graph there can be more than one path i.e. graph can have uni-directional or bi-directional paths (edges) between nodes.
	Model	Tree is a hierarchical model .	Graph is a network model .
	Applications	Tree applications: sorting and searching like Tree Traversal & Binary Search.	Graph applications : Coloring of maps, in OR (PERT & CPM), algorithms, Graph coloring, job scheduling, etc.
13	<p>Write short notes on connected components? (Nov/Dec 2014) BTL1</p> <p>A connected component of an undirected graph is a maximal connected sub graph of the graph. Every vertex of the graph lies in a connected component that consists of all the vertices that can be reached from that vertex, together with all the edges that join those vertices. If an undirected graph is connected, there is only one connected component.</p>		
14	<p>Define a weighted graph. BTL4</p> <p>A graph is said to be weighted graph if every edge in the graph is assigned some weight or value. The weight of an edge is a positive value that may be representing the distance between the vertices or the weights of the edges along the path.</p> 		
15	<p>Define out degree and outdegree of a Graph.(Nov/Dec 2012) BTL4</p> <p>In a directed graph, for any node v, the number of outgoing edges from v, are called out degree of a node .</p>  <p>Out degree of A--→2</p> <p>Out degree of B-→1</p> <p>Out degree of C-→1</p>		

	<p>Out degree of D-→3</p> <p>Out degree of E-→0</p> <p>In a directed graph, for any node v, the number of incoming edges to v, are called in degree of a node v.</p>  <pre> graph TD A((A)) --> B((B)) A((A)) --> C((C)) B((B)) --> D((D)) C((C)) --> D((D)) D((D)) --> E((E)) </pre> <p>In degree of A--→1</p> <p>In degree of B-→2</p> <p>In degree of C-→2</p> <p>In degree of D-→1</p> <p>In degree of E-→1</p>
--	--

16.	<p>Give the code for post order traversal. BTL1</p> <pre> void postorder(struct tree* t) { if(t==NULL) return; else{ postorder(t->left); postorder(t->right); cout<<"\t"<<t->data;}} } } </pre>
17.	<p>Define path in a graph. BTL4</p>

	<p>The path in a graph is the route taken to reach terminal node from a starting node. A path in a graph is a sequence of vertices such that from each of its vertices there is an edge to the next vertex in the sequence. A path in a diagram in which the edges are distinct is called a simple path.</p>
18.	<p>What is an acyclic graph? BTL2</p> <p>A path which originates and ends in the same node is called a cycle or circuit. A simple diagram which does not have any cycles is called an acyclic graph. An acyclic graph does not contain any cycles. Trees are connected acyclic undirected graphs. Directed acyclic graphs are called DAGs.</p>
19.	<p>What is a strongly connected graph and weakly connected graph? BTL2</p> <p>A directed graph is said to be a strongly connected graph if for every pair of distinct vertices there exists a directed path from every vertex to every other vertex. It is also called so Complete Graph. A directed graph is said to be a weakly connected graph if any vertex doesn't have a directed path to any other vertices. The nodes in a weakly connected digraph therefore must all have either out degree or in degree of at least 1.</p>
20.	<p>List out the applications of depth first search. (APRIL/MAY 2016) (Nov/Dec 2017) BTL4</p> <ul style="list-style-type: none"> ✓ Detecting cycle in a graph ✓ Path Finding ✓ Topological Sorting ✓ To test if a graph is bipartite
21	<p>What is a spanning tree? Name two algorithms to find minimum spanning tree. BTL2</p> <p>A spanning tree of a graph is just a sub graph that contains all the vertices and is a tree. A graph may have many spanning trees. Spanning tree of the graph is a connected sub graph in which there are no cycles. The two algorithms are Kruskal's algorithm, Prim's algorithm</p>
22	<p>Define articulation point in a graph. (Nov/Dec 2012) BTL4</p> <p>The articulation point is the point at which the removal of the vertex will split the graph. Articulation points represent vulnerabilities in a network – single points whose failure would split the network into 2 or more disconnected components.</p> <div style="text-align: center;"> <p>Articulation points are 0 and 3</p> </div>
23	<p>Give the code for in order traversal. BTL1</p>

	<pre> void inorder(tree* t) { if(t!=NULL) { inorder(t->left); cout<<"\t"<<t->data; inorder(t->right); } } </pre>
24	<p>List the applications of Depth First Traversal. BTL1</p> <ul style="list-style-type: none"> ✓ Detecting cycle in a graph ✓ For an unweighted graph, DFS traversal of the graph produces the minimum spanning tree and all pair shortest path tree. ✓ For finding path in a graph ✓ For topological sorting ✓ For bi-partite graph ✓ For finding strongly connected component of graph
25	<p>Draw the binary search tree for the following inputs: 70,15,29,33,44,12,79 (Nov/Dec 2017) BTL1</p> <pre> graph TD 70((70)) --- 15((15)) 70 --- 79((79)) 15 --- 12((12)) 15 --- 29((29)) 29 --- 33((33)) 33 --- 44((44)) </pre>
PART B	
1	<p>Explain the various tree traversal methods with algorithm and predict a binary tree with Preorder: ABCDEFGHI and Inorder: BCAEDGHF.(13M)(April/May 2015)(BTL 2)</p> <p>Answer: Page:3.10-Dr.S.Poonkuzhali &P.Revathy</p> <p>Routine and Algorithm :</p> <p>pre order traversal:(3M)</p> <p>Pretrav (p)</p>

```
NODEPTR P;
{
    if (P!=NULL)
    {
        Printf ("%d\n",P->info);
        Pretrav (P->left);
        Pretrav (P->right);
    }
}
```

post order traversal:(3M)

```
posttrav(p)
NODEPTR P;
{
    if(P!=NULL)
    {
        posttrav(P->left);
        posttrav(P->right);
        printf("%d\n",P->info);
    }
}
```

In order traversal:(3M)

```
intrav(p)
NODEPTR P;
{
    if(P!=NULL)
    {
```

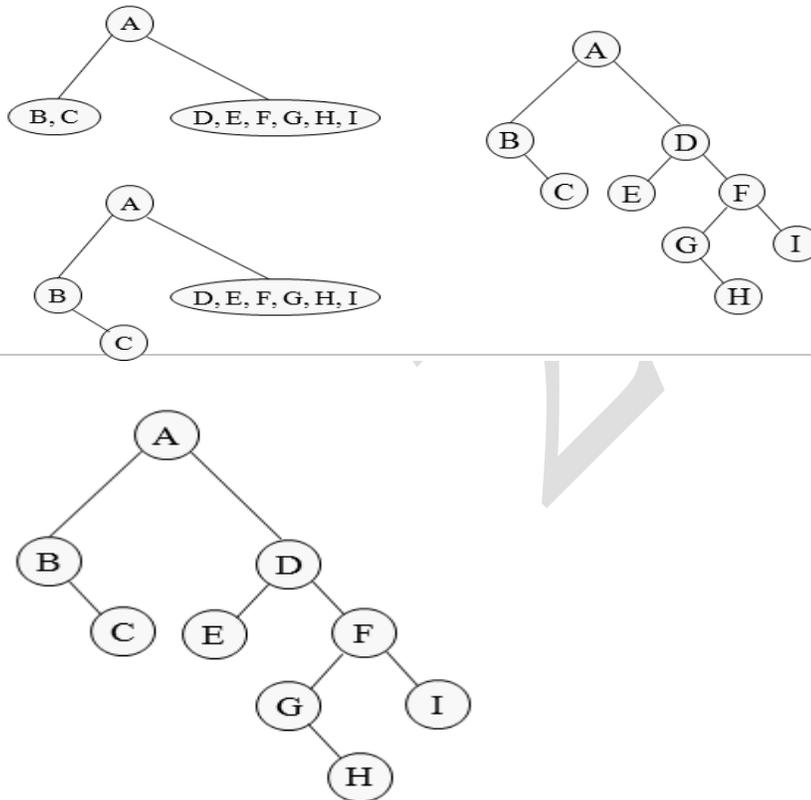
```

posttrav(P->left);

printf(“%d\n”,P->info);

        posttrav(P->right);    }}
    
```

Diagram: (4M)



2 With necessary algorithms, explain the two graph traversal methods. Demonstrate with examples. (April/May 2017, April/May 2015)(13M)(BTL 6)

Answer: Page:3.10-Dr.S.Poonkuzhali &P.Revathy

Graph Traversal(2M)

It is a procedure by which each vertex in the graph is processed exactly once in a systematic manner.

Types of graph traversal(1M)

- ✓ Depth first search
- ✓ Breadth first search

Depth first search(5M)

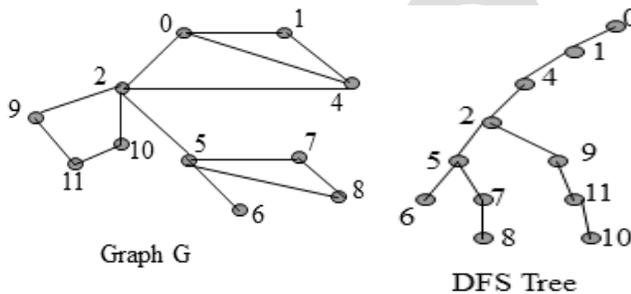
To implement the Depth first Search perform the following Steps :

- ✓ **Step 1:** Choose any node in the graph. Designate it as the search node and mark it as visited.
- ✓ **Step 2:** Using the adjacency matrix of the graph, find a node adjacent to the search node that has not been visited yet. Designate this as the new search node and mark it as visited.
- ✓ **Step 3:** Repeat step 2 using the new search node. If no nodes satisfying (2) can be found, return to the previous search node and continue from there.
- ✓ **Step 4:** When a return to the previous search node in (3) is impossible, the search from the originally chosen search node is complete.
- ✓ **Step 5:** If the graph still contains unvisited nodes, choose any node that has not been visited and repeat step (1) through (4).

ROUTINE FOR DEPTH FIRST SEARCH

```
void DFS (Vertex V)
{
visited [V] = True;
for each W adjacent to V
if (! visited [W])
DFS (W);
}
```

Example :



DFS → 0 → 1 → 4 → 2 → 5 → 6 → 7 → 8 → 9 → 11 → 10

Adjacency Matrix

	0	1	2	4	5	6	7	8	9	1	1
0	0	1	1	1	0	0	0	0	0	0	0
1	1	0	0	1	0	0	0	0	0	0	0
2	1	0	0	1	1	0	0	0	1	1	0
4	1	1	1	0	0	0	0	0	0	0	0
5	0	0	1	0	0	1	1	1	0	0	0
6	0	0	0	0	1	0	0	0	0	0	0
7	0	0	0	0	1	0	0	1	0	0	0
8	0	0	0	0	1	0	1	0	0	0	0
9	0	0	1	0	0	0	0	0	0	0	1
10	0	0	1	0	0	0	0	0	0	0	1
11	0	0	0	0	0	0	0	0	1	1	0

Applications of Depth First Search

- ✓ To check whether the undirected graph is connected or not.
- ✓ To check whether the connected undirected graph is Biconnected or not.
- ✓ To check the a Acyclicity of the directed graph.

Breadth First Traversal(5M)

Breadth first search of a Graph G starts from an unvisited vertex v. Then all unvisited vertices w adjacent to v are visited and so on. The traversal terminates when there are no more nodes to visit. Breadth first search uses a queue data structure to keep track of the order of nodes.

- ✓ **Step 1:** Choose any node in the graph, designate it as the search node and mark it as visited.
- ✓ **Step 2:** Find all the unvisited adjacent nodes to the search node and enqueue them in to the queue Q.
- ✓ **Step 3:** Then the node is dequeued from the queue. Mark that node as visited and designate it as the new search node.
- ✓ **Step 4:** Repeat 2 and 3 using the new search node.
- ✓ **Step 5:** Repeat until the queue becomes empty.

Routine for Breadth first Search

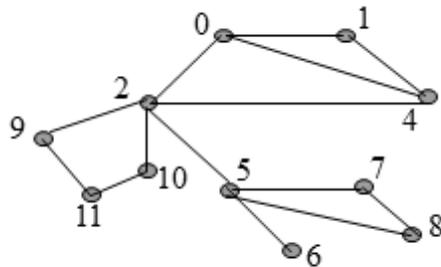
```
void BFS(vertex v)
{
  InitializeQueue(Q);
  visited[v]=1;
  Enqueue(v,Q);
  while(!I  sEmpty(Q))
  {
    v=Dequeue(Q);
    for all w adjacent to v
    {
      Enqueue(w,Q);
      visited[w]=1;
    }
  }
}
```

Example:

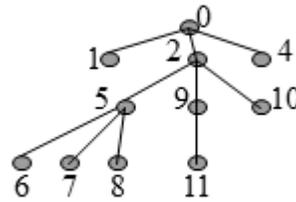
Adjacency Matrix

	0	1	2	4	5	6	7	8	9	10	11
0	0	1	1	1	0	0	0	0	0	0	0
1	1	0	0	1	0	0	0	0	0	0	0
2	1	0	0	1	1	0	0	0	1	1	0
4	1	1	1	0	0	0	0	0	0	0	0
5	0	0	1	0	0	1	1	1	0	0	0
6	0	0	0	0	1	0	0	0	0	0	0
7	0	0	0	0	1	0	0	1	0	0	0

8	0	0	0	0	1	0	1	0	0	0	0
9	0	0	1	0	0	0	0	0	0	0	1
10	0	0	1	0	0	0	0	0	0	0	1
11	0	0	0	0	0	0	0	0	1	1	0



Graph G



BFS Tree

BFS→0->1->2->4->5->9->10->6->7->8->11

3

Explain in detail about the smart union algorithm. (Nov/Dec 2012) (13M)(BTL 2)

Answer: Page:3.10-Dr.S.Poonkuzhali &P.Revathy

Introduction:(2M)

The *unions* were performed rather arbitrarily, by making the second tree a subtree of the first. A simple improvement is always to make the smaller tree a subtree of the larger, breaking ties by any method; we call this approach *union-by-size*.

SMART UNION ALGORITHM(2M)

- ✓ Arbitrary Union
- ✓ Union by size
- ✓ Union by height

Arbitrary Union(3M)

The *unions* were performed rather arbitrarily, by making the second tree a subtree of the first.

```
void initialize(Disjointset S)
```

```
{
```

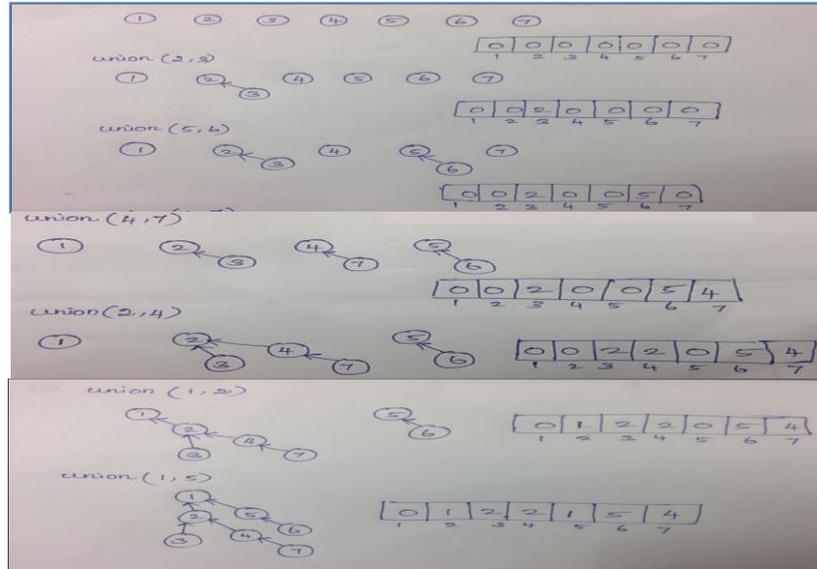
```
    int i;
```

```
    for(i=NumSets;i>0;i--)
```

```
        S[i]=0;
```

```
}
```

```
void SetUnion(DisjSetS,SetType Root1, SetType Root2)
{
S[Root2]=Root1;
}
```

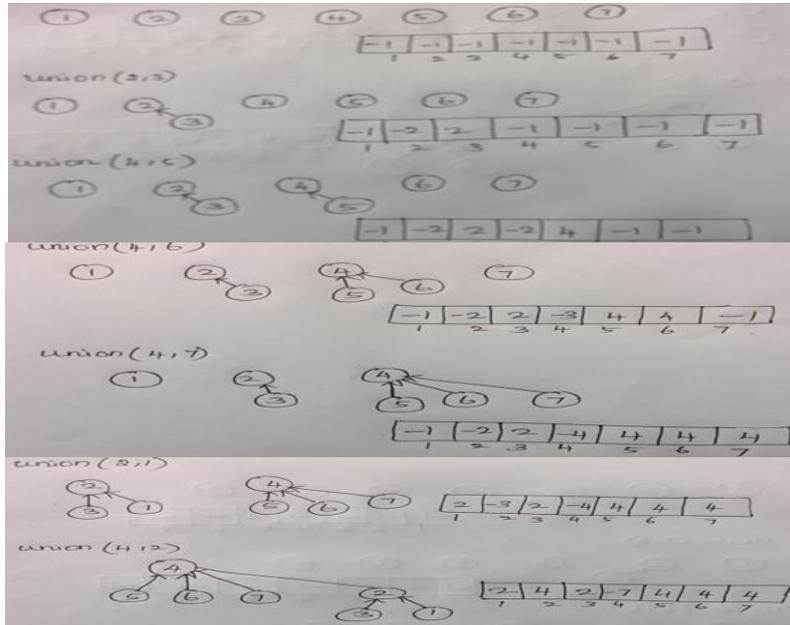


Union by Size(3M)

This can be performed by making the smaller tree a sub tree of the larger tree.

```
void initialize(Disjointset S)
{
int i;
for(i=NumSets;i>0;i--)
    S[i]=-1;
}

void SetUnion(DisjSetS,SetType Root1,
SetType Root2)
{
S[Root1]=S[Root1]+S[Root2];
S[Root1]=Root2;
}
```



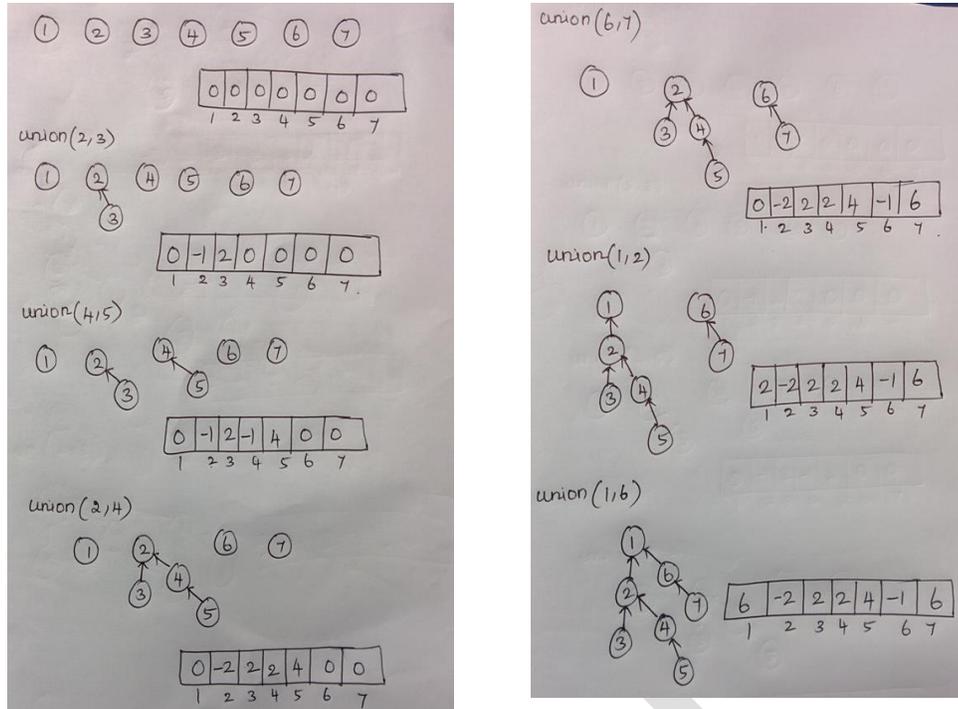
Union by height(3M)

This can be performed by making the shallow tree a sub tree of the deeper tree.

```

void initialize(Disjointset S)
{
    int i;
    for(i=NumSets;i>0;i--)
        S[i]=0;
}

void SetUnion(DisjSetS,SetType Root1, SetType Root2)
{
    if(S[Root2]<S[Root1])
        S[Root1]=Root2;
    else
    {
        if(S[Root2]==S[Root1])
            S[Root1]=S[Root1]-1;
        S[Root2]=Root1;
    }
}
    
```



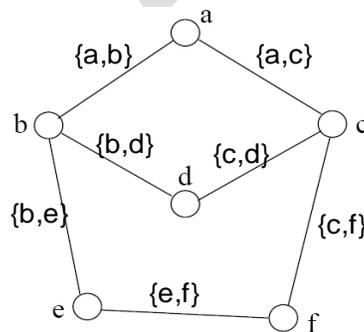
4

What is graph? What are the different ways for representing the graph?(13M) (BTL 1)

Answer: Page:3.10-Dr.S.Poonkuzhali &P.Revathy
Introduction: (2M)

- ✓ A graph $G=(V, E)$ consists a set of vertices, V , and a set of edges, Each edge is a pair of (v, w) , where v, w belongs to V .If the pair is unordered, the graph is undirected; otherwise it is directed

Example(2M)



$$V = \{a, b, c, d, e, f\}$$

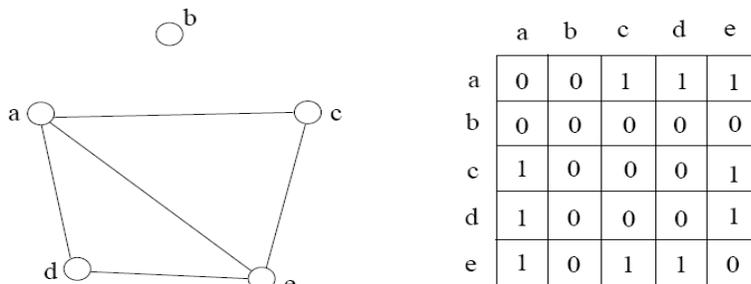
$$E = \{\{a, b\}, \{a, c\}, \{b, d\}, \{c, d\}, \{b, e\}, \{c, f\}, \{e, f\}\}$$

Graph Representation(3M)

Two popular computer representations of a graph. Both represent the vertex set and the edge set, but in different ways.

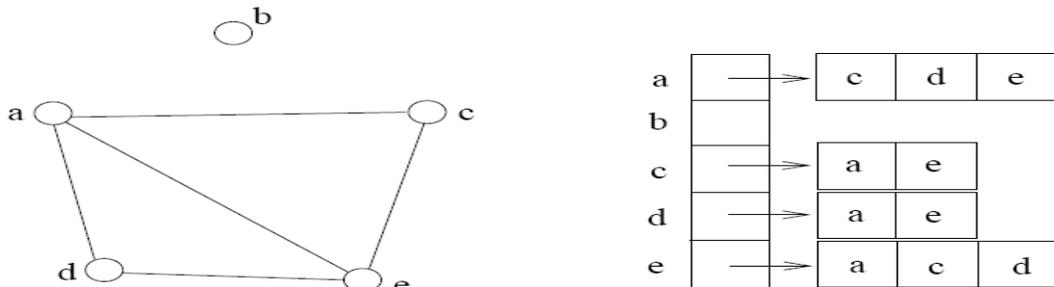
- ✓ Adjacency Matrix
Use a 2D matrix to represent the graph
- ✓ Adjacency List
Use a 1D array of linked lists

Adjacency Matrix



- ✓ 2D array A[0..n-1, 0..n-1], n - the number of vertices in the graph
- ✓ Each row and column is indexed by the vertex
- ✓ A[i][j]=1 if there is an edge connecting vertices i and j; otherwise, A[i][j]=0
- ✓ storage requirement - $\Theta(n^2)$.

Adjacency List(3M)



- ✓ The adjacency list - an array A[0..n-1] of lists, n - the number of vertices in the graph.
- ✓ Each array entry - indexed by the vertex id.
- ✓ Each list A[i] stores the ids of the vertices adjacent to vertex i

Storage of Adjacency List

- ✓ The array takes up $\Theta(n)$ space
- ✓ Define degree of v, deg(v), to be the number of edges incident to v. Then, the total space to store the graph is proportional to:

$$\sum_{\text{vertex } v} \text{deg}(v)$$

	<p>✓ In all, the adjacency list takes up $\Theta(n+m)$ space</p> <p>Adjacency List vs. Matrix(3M)</p> <p>✓ Adjacency List More compact than adjacency matrices if graph has few edges Requires more time to find if an edge exists</p> <p>✓ Adjacency Matrix Always require n^2 space Can quickly find if an edge exist</p>
5	<p>(i)How can you construct an expression tree? Describe your answer with an example.(7M) (Nov/Dec 2015)(BTL 3)</p> <p>Answer: Page:3.10-Dr.S.Poonkuzhali &P.Revathy Introduction:(2M)</p> <p>An expression tree is a tree whose leaves contain the operands of the expression, and the other nodes contain the operators.</p> <p>Example:</p> <p>Consider the expression:</p> <p>$(a + b*c) * (d + e)$</p> <p>It can be represented as a binary tree:</p> <p>In-order traversal - (left subtree_root right) reconstructs the expression: $(a + b*c) * (d + e)$</p> <p>Post-order traversal - results in the corresponding postfix expression: $a b c * + d e + *$</p> <p>Algorithm: (3M)</p> <p>Read a symbol sym.</p> <p>If (sym = operand) print it</p> <p>If (sym = '(') push(S, sym)</p> <p>If (sym = operation)</p> <p>If (stack is empty) push(S, sym)</p>

Else temp_sym = pop(S)

If temp_sym higher or equal priority

print temp_sym

push(sym)

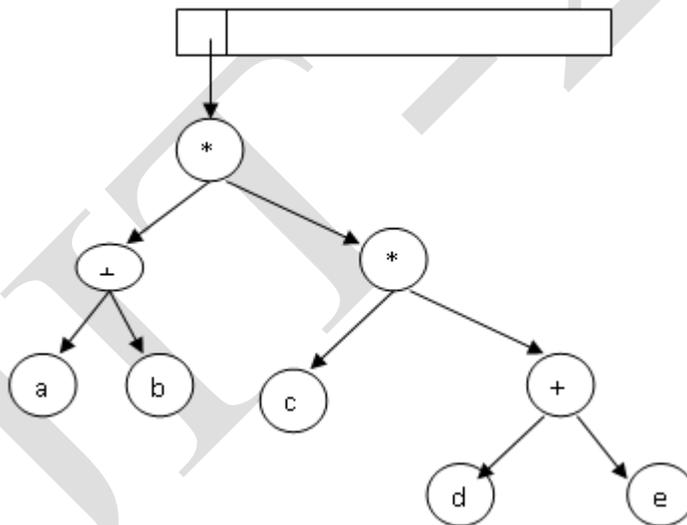
Else push(temp_sym)

push(sym)

If (sym = ')') pop and print until '(' is encountered, do not print '('.

Pop and print the remaining symbols from the stack.

Diagram;(2M)



(ii) Explain how sets are represented? Explain union find operations. (Nov/Dec 2015)(BTL 2)(6M)

Answer: Page:3.10-Dr.S.Poonkuzhali &P.Revathy

Introduction:(2M)

A relation R is defined on a set S for every pair of elements (a,b), $a,b \in S$,the relation aRb is either true or false.

If aRb is true, then a is related to b.

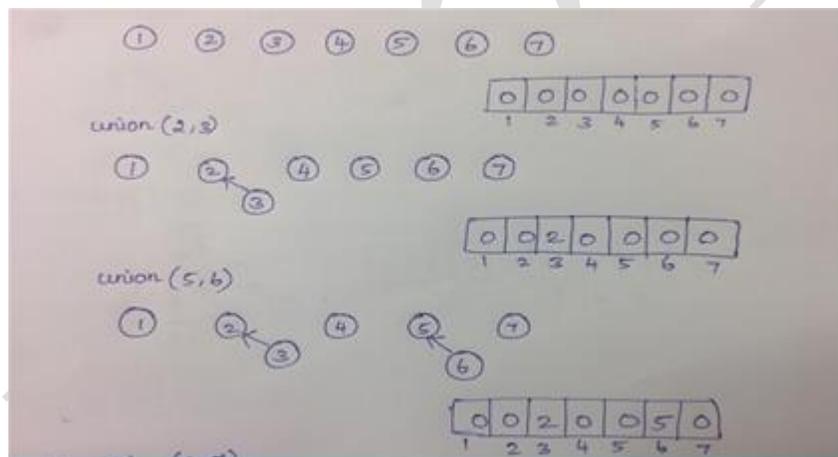
An equivalence relation is a relation R that satisfies three properties:

- ✓ (Reflexive) $a R a$, for all a belongs to S.
- ✓ (Symmetric) $a R b$ if and only if $b R a$.
- ✓ (Transitive) $a R b$ and $b R c$ implies that $a R c$.

Basic data structure:(2M)

Tree data structure is used to implement the set. The name of a set is given by the node at the root.The array implementation of tree represents that $P[i]$ is the parent of i^{th} element. If i is a root, then $P[i] = 0$.

Representation of sets:

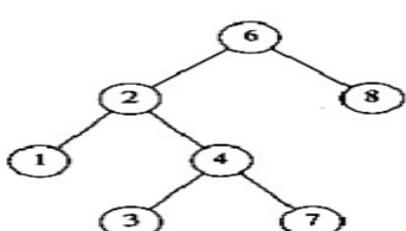


Union Find Operations(2M)

- ✓ **Find(X)** – Returns the root of the tree containing X.
- ✓ **Union(X,Y)** – Merges the two trees by making the root pointer of one node point to the root node of the other tree.

Disjoint set initialization routine

```
void initialize(Disjset S)
{
```

	<pre> int i; for(i = numsets;i>0;i--) S[i] = 0; } </pre> <p>Routine for Find</p> <p>SetType Find(Element Type X, DisjSet S)</p>
<p>.No</p>	<p style="text-align: center;">PART* C</p>
<p>1</p>	<p>Explain in detail the implementation of Binary Search Tree and perform its operations. (May/June 2012)(13M)(BTL 2) Answer: Page:3.10-Dr.S.Poonkuzhali &P.Revathy</p> <p>Introduction: (2M) Binary search tree is a binary tree in which for every node X in the tree, the values of all the keys in its left sub tree are smaller than the key value in X, and the values of all the keys in its right sub tree are larger than the key value in X.</p> <p>Example: (3M)</p> <p>Void SetUnion(DisjSet S, SetType R₁,SetType R₂)</p>  <pre> graph TD 6((6)) --- 2((2)) 6 --- 8((8)) 2 --- 1((1)) 2 --- 4((4)) 4 --- 3((3)) 4 --- 7((7)) </pre>
	<p>Implementation of Binary Search Tree: (8M)</p> <p>Binary Search Tree can be implemented as a linked data structure in which each node with three fields.</p> <ul style="list-style-type: none"> ✓ Element ✓ pointer to the left child ✓ pointer to the right child. <p>Binary Search Tree Declaration</p> <pre> typedef struct TreeNode * SearchTree; StructTreeNode </pre>

```

{
int Element ;

SearchTree Left;

SearchTree Right;

};

```

ROUTINE TO INSERT

SearchTree Insert (int X, searchTree T)

```

{
if (T == NULL)
{
T = malloc (size of (StructTreeNode));
if (T != NULL) // First element is placed in the root.
{
T->Element = X;
T-> left = NULL;
T ->Right = NULL;
}
}
else if (X < T ->Element)
T ->left = Insert (X, T->left);
else if (X > T->Element)
T ->Right = Insert (X, T->right);
return T;
}

```

ROUTINE FOR FIND OPERATION

int Find (int X, SearchTree T)

```
{  
if (T == NULL)  
Return NULL ;  
if (X < T ->Element)  
return Find (X, T ->left);  
else if (X > T ->Element)  
return Find (X, T ->Right);  
else  
return T; // returns the position of the search element.  
}
```

NON - RECURSIVE ROUTINE FOR FINDMIN

```
intFindMin (SearchTree T)  
{  
if (T! = NULL)  
while (T->Left != NULL)  
T = T->Left ;  
return T;  
}
```

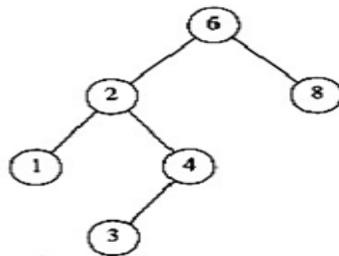
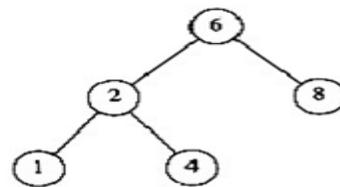
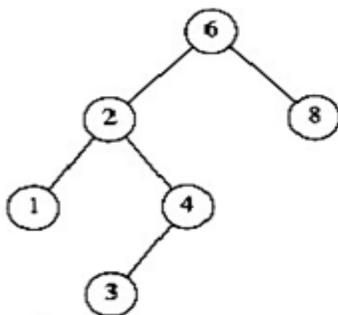
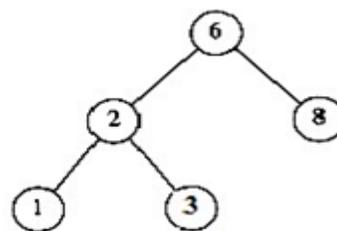
NON - RECURSIVE ROUTINE FOR FINDMAX

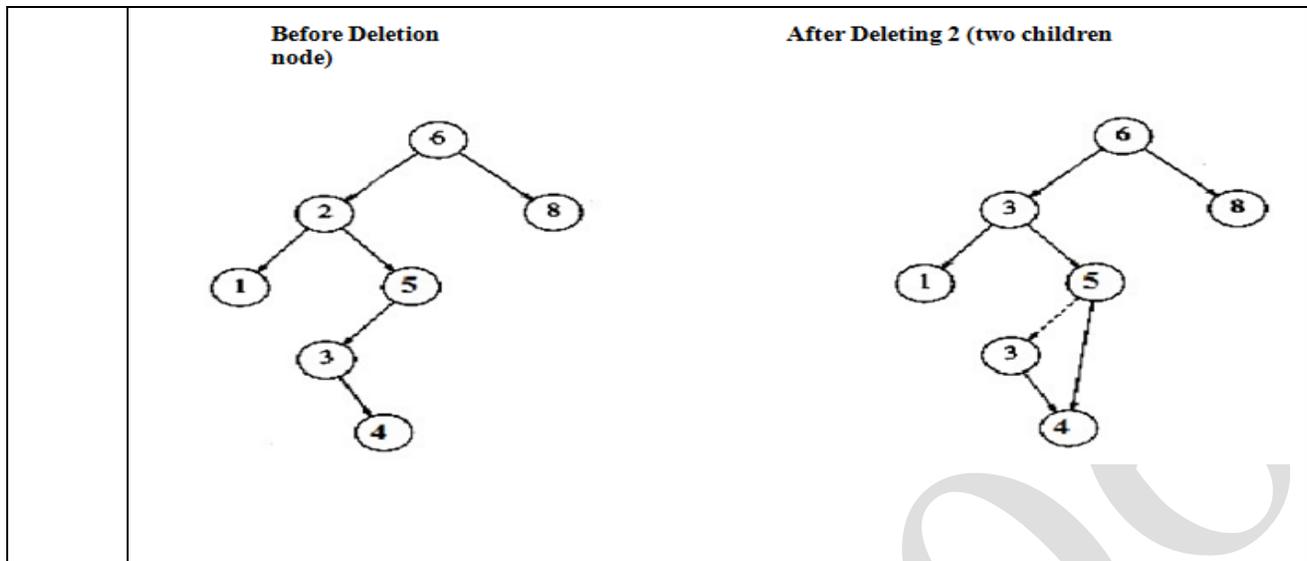
```
intFindMax (SearchTree T)  
{  
if (T! = NULL)  
while (T->Right != NULL)  
T = T->Right ;  
return T ;  
}
```

DELETE :

Deletion operation is the complex operation in the Binary search tree. To delete an element, consider the following three possibilities.

- ✓ CASE 1: Node to be deleted is a leaf node (ie) No children.
- ✓ CASE 2: Node with one child.
- ✓ CASE 3: Node with two children.

CASE 1: Node with no children (Leaf node)**To Delete 3****Before Deletion****After Deleting 3****CASE 2: - Node with one child****Before Deletion****After Deleting 4****CASE 3 : Node with two children**



2 **Formulate an algorithm to insert an element in a binary tree. (Nov/Dec 2011)(BTL 5)(13M)**

Answer: Page:3.10-Dr.S.Poonkuzhali &P.Revathy

Definition :- (2M)

Binary Tree is a tree in which no node can have more than two children. Maximum number of nodes at level i of a binary tree is 2^{i-1} .

A **binary tree** is a tree which is either empty, or one in which every node:

- ✓ has no children; or
- ✓ has just a left child; or
- ✓ has just a right child; or
- ✓ has both a left and a right child.

BINARY TREE NODE DECLARATIONS (4M)

```
StructTreeNode
{
int Element;
StructTreeNode *Left ;
StructTreeNode *Right;
};
```

FULL BINARY TREE :-

A full binary tree of height h has $2^{h+1} - 1$ nodes.

COMPLETE BINARY TREE :

A complete binary tree of height h has between 2^h and $2^{h+1} - 1$ nodes. In the bottom level the elements should be filled from left to right.

REPRESENTATION OF A BINARY TREE (5M)

There are two ways for representing binary tree, they are

- ✓ Linear Representation
- ✓ Linked Representation

Linear Representation

For any element in position i, the left child is in position 2i, the right child is in position (2i + 1), and the parent is in position (i/2).

Linked Representation

The elements are represented using pointers. Each node in linked representation has three fields, namely,

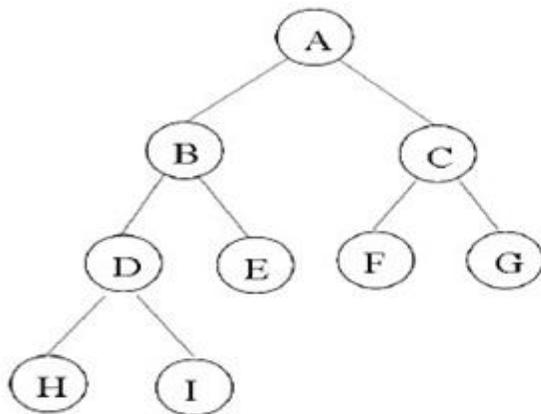
- ✓ Pointer to the left subtree
- ✓ Data field
- ✓ Pointer to the right subtree

In leaf nodes, both the pointer fields are assigned as NULL.

Array Representation (Sequential Representation) (2M)

The elements in the tree are represented using arrays. For any element in position i , the left child is in position $2i$, the right child is in position $(2i + 1)$, and the parent is in position $(i/2)$.

Binary Tree



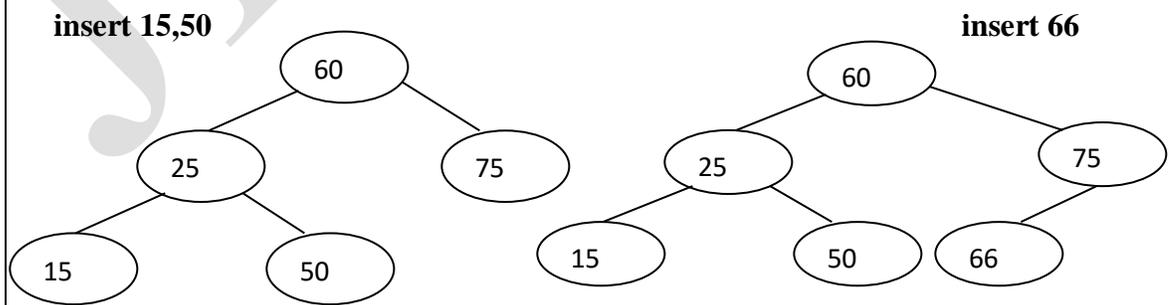
Array Representation

[1]	A
[2]	B
[3]	C
[4]	D
[5]	E
[6]	F
[7]	G
[8]	H
[9]	I

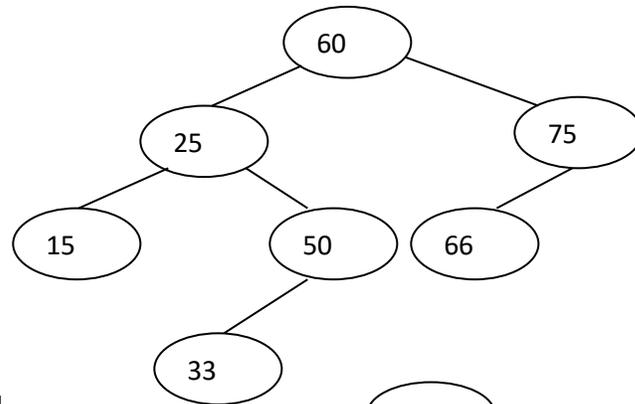
3 Draw a binary search tree for the input 60,25,75,15,50,66,33,44. Trace the algorithm to delete nodes 25,75,44 from the tree.(13M) (May/June 2012)BTL 5

Answer: Page: 98 – Notes

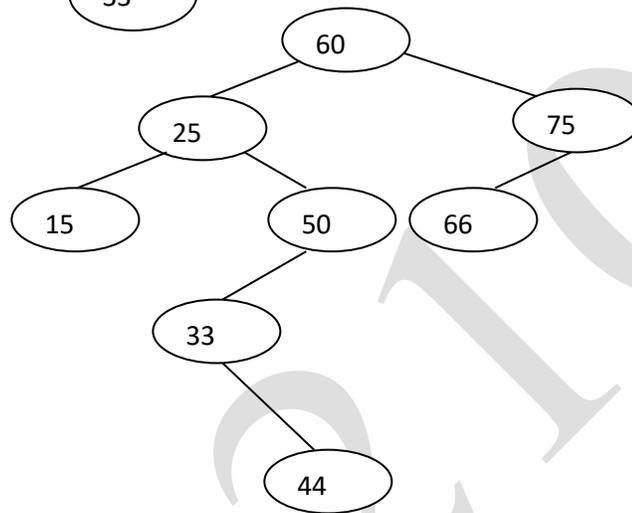
Operations:(13M)



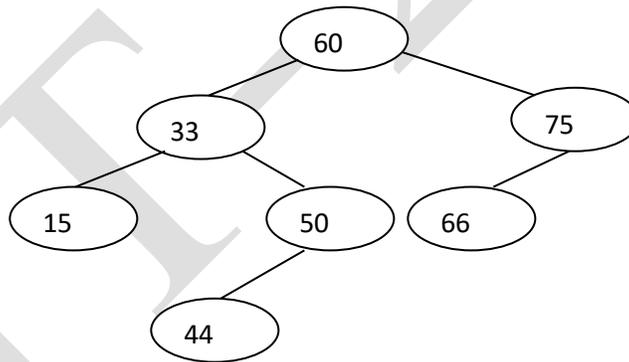
Insert 33



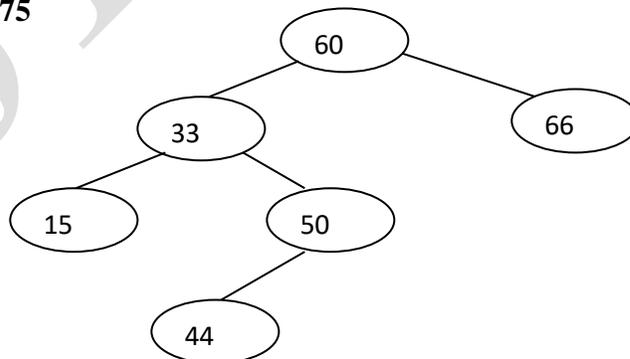
insert 44

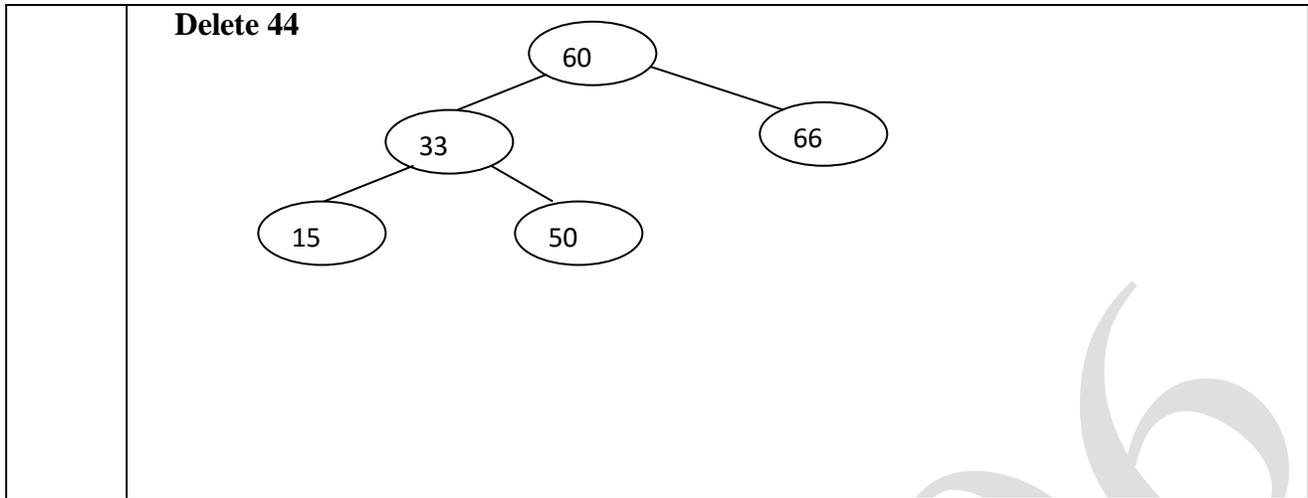


Delete 25



Delete 75





JIT-2106

UNIT V SEARCHING AND SORTING ALGORITHMS	
Linear Search – Binary Search. Bubble Sort, Insertion sort – Merge sort – Quick sort - Hash tables – Overflow handling.	
PART*A	
Q.NO	QUESTIONS
1.	<p>What is meant by sorting and what are its classifications?(April/May 2015) BTL 1</p> <p>Ordering the data in an increasing or decreasing order according to some relationship among the data item is called sorting.</p> <ul style="list-style-type: none"> ✓ Internal sorting ✓ External sorting
2.	<p>What is meant by external sorting?BTL 1 (NOV/DEC 2018)</p> <p>External sorting is a process of sorting in which large blocks of data stored devices are moved to the main memory and then sorted. Example: Merge sort.</p>
3.	<p>What is meant by internal sorting?BTL 1(NOV/DEC 2018)</p> <p>This method uses only primary memory during sorting process if all data to be sorted can be accommodated at the time in memory is called as internal sorting. Example: Heap sort, shell sort, quick sort.</p>
4.	<p>What are the various factors to be considered in deciding a sorting algorithm? BTL 1</p> <ul style="list-style-type: none"> ✓ Programming time ✓ Execution time of the program ✓ Memory needed for program environment
5.	<p>What is the main idea in Bubble sort? BTL 1</p> <p>The basic idea underlying the bubble sort is to pass through the file sequentially several times. Each pass consists of comparing each element in the file with its successor ($x[i]$ and $x [i+1]$) and interchanging the two elements if they are not in proper order.</p>
6.	<p>What is the basic idea of quick sort? BTL 1</p> <p>Pick one element in the array, which will be the pivot. Make one pass through the array, called a partition step, re-arranging the entries so that: The pivot is in its proper place. Entries smaller than the pivot are to the left of the pivot. Entries larger than the pivot are to its right. Recursively apply quick sort to the part of the array that is to the left of the pivot, and to the right part of the array.</p>
7.	<p>What is the advantage of quick sort? BTL 1</p> <p>Quick sort reduces unnecessary swaps and moves an item to a greater distance, in one</p>

	move. One of the fastest algorithms on average. Does not need additional memory
8.	<p>What is complexity analysis? BTL1</p> <p>It is the analysis of the amount of memory and time an algorithm requires to completion. There are two types of Complexity</p> <ul style="list-style-type: none"> ✓ Space Complexity: Space complexity of an algorithm is the amount of memory it needs to run to completion. ✓ Time Complexity: Time complexity is the amount of computer time an algorithm requires to run to completion.
9.	<p>What does asymptotic notation mean? BTL 1</p> <p>Asymptotic notations are terminology that is introduced to enable us to make meaningful statements about the time and. The different notations are</p> <ul style="list-style-type: none"> ✓ Big – Oh notation ✓ Omega notation ✓ Theta notation.
10.	<p>What are the techniques used to choose the pivot element for quick sort? BTL 1</p> <p>The various techniques are</p> <ul style="list-style-type: none"> ✓ First element ✓ Random pick ✓ Median of three portioning
11.	<p>What is binary search? BTL 1</p> <p>Binary search is also a method used to locate a specified item in a sorted list. This method starts by comparing the searched element to the elements in the middle of the list. If the comparison determines that the two elements are equal the method stops and returns the position of the element. If the searched element is greater than the middle element, it starts the method again using only the bottom half of the sorted list. If the searched element is less than the middle element, it starts the method again using only the top half of the sorted list.</p>
12.	<p>What is linear search? BTL 1</p> <p>Linear search is the simplest searching method, which checks each element in a list sequentially until it finds a specified element. The input to the linear search method is a sequence and the item that needs to be searched. The output is true if the specified item is within the provided sequence or false if it is not in the sequence. The complexity of linear search is $O(n)$.</p>
13	<p>What is divide and conquer technique?BTL 1</p> <p>Divide and Conquer algorithm is based on dividing the problem to be solved into several, smaller sub instances, solving them independently and then combining the sub instances</p>

	solutions so as to yield a solution for the original instance.												
14	<p>What is dynamic programming?BTL 1</p> <p>Dynamic programming algorithm is a general class of algorithms which solve problems by solving smaller versions of the problem, saving the solutions to the small problems and then combining them to solve the larger problems.</p>												
15	<p>What is the time complexity of Quick sort and Binary search?(Nov/Dec 2014)BTL 1</p> <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>Time complexity</th> <th>Quick sort</th> <th>Binary Search</th> </tr> </thead> <tbody> <tr> <td>Best case</td> <td>$O(n \log n)$</td> <td>$O(\log n)$</td> </tr> <tr> <td>Average case</td> <td>$O(n \log n)$</td> <td>$O(\log n)$</td> </tr> <tr> <td>Worst case</td> <td>$O(n^2)$</td> <td>$O(\log n)$</td> </tr> </tbody> </table>	Time complexity	Quick sort	Binary Search	Best case	$O(n \log n)$	$O(\log n)$	Average case	$O(n \log n)$	$O(\log n)$	Worst case	$O(n^2)$	$O(\log n)$
Time complexity	Quick sort	Binary Search											
Best case	$O(n \log n)$	$O(\log n)$											
Average case	$O(n \log n)$	$O(\log n)$											
Worst case	$O(n^2)$	$O(\log n)$											
16.	<p>Define merge sort. How an array elements are sorted using merge sort?(Nov/Dec 2015)BTL 1</p> <p>Merge sort is a divide and conquer algorithm. Merge sort is the technique which has sorted sub arrays which are merged to form a single sorted array.</p> <p>A merge sort works as follows:</p> <ul style="list-style-type: none"> ✓ Divide the unsorted list into n sub lists, each containing 1 element ✓ Repeatedly merge sub lists to produce new sorted sub lists until there is only 1 sub list remaining. This will be the sorted list. 												
17.	<p>What are the advantages of merge sort? BTL 1</p> <ul style="list-style-type: none"> ✓ It can be applied to files of any size. ✓ Reading of the input during the run-creation step is sequential ==>Not much seeking. ✓ Reading through each run during merging and writing the sorted record is also sequential. 												
18.	<p>What are the advantages and disadvantages of shell sort? BTL 1</p> <ul style="list-style-type: none"> ✓ Efficient for medium size list. ✓ The number of comparisons is less. ✓ The running time of shell sort depends on the incrementing sequence. <p>Disadvantages:</p>												

	<ul style="list-style-type: none"> ✓ Elements at odd and even places are compared only in the last step. 						
19.	<p>Set the drawbacks of insertion sort. (April / May 2017)BTL 1</p> <ul style="list-style-type: none"> ✓ It is less efficient on list containing more number of elements. ✓ As the number of elements increases the performance of the program would be slow. ✓ Insertion sort needs a large number of element shifts. 						
20.	<p>Differentiate linear search and binary search.BTL 1</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 50%; text-align: center;">Linear search</th> <th style="width: 50%; text-align: center;">Binary search</th> </tr> </thead> <tbody> <tr> <td>Linear search is easy but takes more time to search an element as it compare all element sequentially</td> <td>Binary search it start searching from middle, if the searching element is not found in middle then it goes to left or right and vice versa. and hence take less time than linear search</td> </tr> <tr> <td>Linear search requires $O(n)$times</td> <td>Binary search is very best in time and efficiency. It requires $O(\log n)$times</td> </tr> </tbody> </table>	Linear search	Binary search	Linear search is easy but takes more time to search an element as it compare all element sequentially	Binary search it start searching from middle, if the searching element is not found in middle then it goes to left or right and vice versa. and hence take less time than linear search	Linear search requires $O(n)$ times	Binary search is very best in time and efficiency. It requires $O(\log n)$ times
Linear search	Binary search						
Linear search is easy but takes more time to search an element as it compare all element sequentially	Binary search it start searching from middle, if the searching element is not found in middle then it goes to left or right and vice versa. and hence take less time than linear search						
Linear search requires $O(n)$ times	Binary search is very best in time and efficiency. It requires $O(\log n)$ times						
21	<p>What is insertion sort?BTL 1</p> <p>Insertion sort iterates, consuming one input element each repetition, and growing a sorted output list. Each iteration, insertion sort removes one element from the input data, finds the location it belongs within the sorted list, and inserts it there. It repeats until no input elements remain.</p>						
22	<p>Define best case of an algorithm. (April/May 2010)BTL 1</p> <p>It is the shortest time that an algorithm will use over all instances of size n for a given problem to produce the result.</p>						
23	<p>State why quick sort is more efficient than merge sort. (Nov/Dec 2013)BTL 1</p> <p>Theoretically, both quick sort and merger sort take $O(n \log n)$ time and hence time taken to sort the elements remains same. However, quick sort is superior to merge sort in terms of space. Quick sort is in-place sorting algorithm whereas merge sort is not in-place. In-place sorting means, it does not use additional storage space to perform sorting. In merge sort, to merge the sorted arrays it requires a temporary array and hence it is not in-place. However time efficiency of the quick sort depends on the choice of the pivot element.</p>						
24	<p>What is performance analysis of an algorithm?BTL 1</p>						

	<p>The analysis of the performance of an algorithm based on specification is called performance analysis. It is loosely divided into</p> <ul style="list-style-type: none"> ✓ Priori estimates ✓ Posterior Testing
25	<p>What is time complexity?(April/May 2015)BTL 1</p> <p>Time complexity of an algorithm computes the amount of time taken by an algorithm to run to its completion. Commonly it is represented using big O notation. Generally it is categorized as best case time complexity, worst case time complexity and average case time complexity. It is commonly estimated by counting the number of elementary operations performed by the algorithm.</p>
	PART * B
1	<p>Define Heap Sort. Write the algorithm for heap sort procedures.(13M) BTL 2</p> <p>Answer: Page:5.11-Dr.S.Poonkuzhali &P.Revathy</p> <p>Introduction: (3M)</p> <ul style="list-style-type: none"> ✓ Heap sort operates by first converting the list in to a heap tree. ✓ Heap tree -binary tree in which each node has a value greater than both its children. <p>Program:(10M)</p> <pre>#include <stdio.h> void main() { int heap[10], no, i, j, c, root, temp; printf("\n Enter no of elements :"); scanf("%d", &no); printf("\n Enter the nos : "); for (i = 0; i < no; i++) scanf("%d", &heap[i]); for (i = 1; i < no; i++) { c = i;</pre>

```
do
{
root = (c - 1) / 2;
if (heap[root] < heap[c]) /* to create MAX heap array */
{
temp = heap[root];
heap[root] = heap[c];
heap[c] = temp;
}
c = root;
} while (c != 0);
}

printf("Heap array : ");
for (i = 0; i < no; i++)
printf("%d\t ", heap[i]);
for (j = no - 1; j >= 0; j--)
{
temp = heap[0];
heap[0] = heap[j] /* swap max element with rightmost leaf element */
heap[j] = temp;
root = 0;
do
{
c = 2 * root + 1; /* left node of root element */
if ((heap[c] < heap[c + 1]) && c < j-1)
c++;
```

	<pre> if (heap[root]<heap[c] && c<j) /* again rearrange to max heap array */ { temp = heap[root]; heap[root] = heap[c]; heap[c] = temp; } root = c; } while (c < j); } printf("\n The sorted array is : "); for (i = 0; i < no; i++) printf("\t %d", heap[i]); printf("\n Complexity : \n Best case = Avg case = Worst case = O(n logn) \n"); } </pre>
2	<p>Write a C program to implement binary search and explain it with an example. Compute its complexity. (13M) (Nov/Dec2017, April / May 2017)BTL 2</p> <p>Answer: Page:5.3-Dr.S.Poonkuzhali &P.Revathy</p> <p>Introduction:(3M)</p> <ul style="list-style-type: none"> ✓ Binary search - method used to locate a specified item in a sorted list. ✓ This method starts by comparing the searched element to the elements in the middle of the list. ✓ If the searched element is greater than the middle element, it starts the method again using only the bottom half of the sorted list. ✓ If the searched element is less than the middle element, it starts the method again using only the top half of the sorted list. ✓ If the searched element is not within the list, the method will return a unique value indicating that. <p>Problem: (5M)</p>

Fig: Illustration to find 22 from the list
 → Element 22 is in the position 10.

Program: (5M)

```

#include<stdio.h>
#include<conio.h>
void bsearch(int x[], int low, int high, int ele);
int x[100];
void main()
{
    int i,n,ele;
    clrscr();
    printf("\nENTER THE NUMBER OF ELEMENTS:");
    scanf("%d",&n);
    printf("ENTER THE VALUES:");
    for(i=1;i<=n;i++)
    {
    
```

<pre>scanf("%d",&x[i]); } printf("ENTER THE ELEMENT TO BE SEARCHED:"); scanf("%d",&ele); bsearch(x,1,n,ele); getch(); } void bsearch(int x[],int low, int high, intele) { int mid; mid=(low+high)/2; if(ele==x[mid]) { printf("ELEMENT FOUND\n"); printf("POSITION:%d",mid); } else if(ele<x[mid]) { bsearch(x,1,mid-1,ele); } else if(ele>x[mid]) { bsearch(x,mid+1,high,ele); } else {</pre>
--

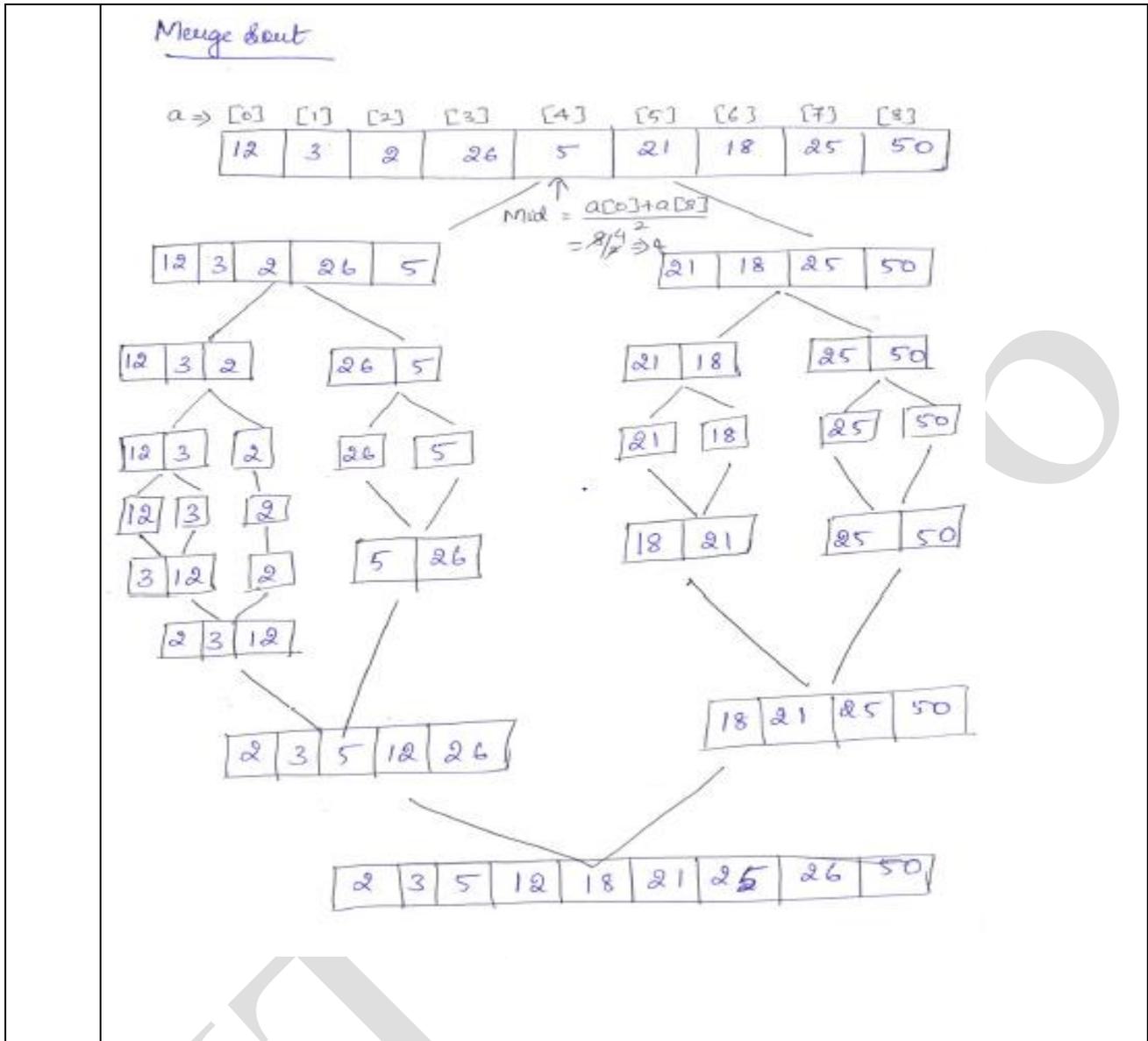
	<pre>printf("ELEMENT NOT FOUND"); } }</pre> <p>The average case efficiency is $O(\log n)$</p>
3	<p>Describe the merge sort using divide and conquer technique with suitable example. Sort the elements 12,3,2,26,5,21,18,25 and 50 using merge sort and trace the output. (13M) (Nov/Dec 2017, April / May 2017)BTL 2</p> <p>Answer: Page:5.16 -Dr.S.Poonkuzhali&P.Revathy</p> <p>Introduction: (3M) Top down merge sort algorithm that recursively splits the list into sublists until sublist size is 1, then merges those sublists to produce a sorted list. The copy back step is avoided with alternating the direction of the merge with each level of recursion.</p> <p>Program:(5M)</p> <pre>//Program for implementing merge sort #include<stdio.h> void mergesort(int ilist[],int,int); void merge(intilist[],int,int,int); void main() { int a[20]; inti,n; clrscr(); printf("\tMERGE SORT"); printf("\n\nEnter the number of elements:"); scanf("%d",&n); printf("Enter the array elements:"); for(i=0;i<n;i++) scanf("%d",&a[i]);</pre>

```
printf("\nThe elements of the array are:");
    for(i=0;i<n;i++)
printf(" %d",a[i]);
mergesort(a,0,n-1);
printf("\nThe sorted array is:");
    for(i=0;i<n;i++)
printf(" %d",a[i]);
}
//mergesort function
void mergesort(intilist[20],intlow,int high)
{
int mid;
if(low<high)
{
mid=(low+high)/2;
mergesort(ilist,low,mid);
mergesort(ilist,mid+1,high);
merge(ilist,low,mid,high);
}
}
//merge function
void merge(intilist[20],intlow,intmid,int high)
{
int i1,i2,iresult,i;
intmlist[20];
i1=low;
```

```
i2=mid+1;
iresult=low;
while((i1<=mid)&&(i2<=high))
{
    if(ilst[i1]<=ilst[i2])
    {
mlist[iresult]=ilst[i1];
        i1++;
    }
    else
    {
mlist[iresult]=ilst[i2];
        i2++;
    }
iresult++;
}
if(i1<=mid)
{
    while(i1<=mid)
    {
mlist[iresult]=ilst[i1];
        i1++;
iresult++;
    }
}
else
```

```
{  
    while(i2<=high)  
    {  
mlist[iresult]=ilist[i2];  
        i2++;  
iresult++;  
    }  
}  
for (i=low;i<=high;i++)  
ilist[i] =mlist[i];  
}
```

Problem:(5M)



4 Write a recursive algorithm for quick sort and apply the same to sort the elements 12,3,2,26,5,21,18,25 and 50 and trace the output.(13M)(April / May 2017, Nov/Dec 2017) BTL 2

Answer: Page:5.12-Dr.S.Poonkuzhali &P.Revathy

Introduction:

(3M)

Quicksort is a fast sorting algorithm, which is used not only for educational purposes, but widely applied in practice. On the average, it has $O(n \log n)$ complexity, making quicksort suitable for sorting big data volumes.

The divide-and-conquer strategy is used in quicksort. Below the recursion step is described:

- ✓ Choose a pivot value.
- ✓ Partition.

✓ Sort both parts.

On the average quicksort has $O(n \log n)$ complexity

Program:(10 M)

```
#include<stdio.h>

#include<conio.h>

void quicksort(int x[], int left, int right);

void swap(int x[], int ele1, int ele2);

int x[100];

void main()
{
    inti,n;

    printf("\nENTER THE NUMBER OF ELEMENTS:");
    scanf("%d",&n);
    printf("ENTER THE VALUES:");
    for(i=1;i<=n;i++)
    {
        scanf("%d",&x[i]);
    }
    printf("\nELEMENTS BEFORE SORTING:");
    for(i=1;i<=n;i++)
    {
        printf("%d\t",x[i]);
    }
    quicksort(x,1,n);

    printf("\nELEMENTS AFTER SORTING:");

    for(i=1;i<=n;i++)
```

```
{
    printf("%d\t",x[i]);
}
}
void quicksort(int x[],int left, int right)
{
    inti,j,pivot;
    if(left<right)
    {
        i=left;
        j=right+1;
        pivot=x[left];
        do
        {
            do
                i++;
            while(x[i]<pivot);
            do
                j--;
            while(x[j]>pivot);
            if(i<j)
                swap(x,i,j);
        } while(i<j);
        swap(x,left,j);
        quicksort(x,left,j-1);
        quicksort(x,j+1,right);
    }
}
```

```

    }
}
void swap(int x[], int ele1, int ele2)
{
    int temp;
    temp=x[ele1];
    x[ele1]=x[ele2];

    x[ele2]=temp;
}

```

5 **List the various sorting techniques and explain the worst and best case time complexity of various sorting techniques (13M)(Nov/Dec 2017)BTL 1**

Answer: Page:5.6-Dr.S.Poonkuzhali &P.Revathy

Algorithm	Time Complexity	
	Best	Worst
Selection Sort	$\Omega(n^2)$	$O(n^2)$
Bubble Sort	$\Omega(n)$	$O(n^2)$
Insertion Sort	$\Omega(n)$	$O(n^2)$
Heap Sort	$\Omega(n \log(n))$	$O(n \log(n))$
Quick Sort	$\Omega(n \log(n))$	$O(n^2)$
Merge Sort	$\Omega(n \log(n))$	$O(n \log(n))$
Bucket Sort	$\Omega(n+k)$	$O(n^2)$
<u>Radix Sort</u>	$\Omega(nk)$	$O(nk)$

Q.No	PART* C
1	<p>Explain in detail about the implementation of Linear Search and perform its operations (13M)(May/June 2012) BTL 2 Answer: Page:5.15-Dr.S.Poonkuzhali &P.Revathy</p> <p>Linear search – Introduction:(2M)</p> <ul style="list-style-type: none"> ✓ linear search (Searching algorithm) which is used to find whether a given number is present in an array and if it is present then at what location it occurs. ✓ Also known as sequential search. ✓ Very simple and works as follows: We keep on comparing each element with the next element to search until the desired element is found or list ends. Linear search is suitable for multiple occurrences and using function. <p>Program:(7M)</p> <pre>#include <stdio.h> int main() { int array[100], search, c, n; printf("Enter the number of elements \n"); scanf("%d",&n); printf("\nEnter the elements"); for (c = 0; c < n; c++) scanf("%d", &array[c]); printf("Enter the number to search\n"); scanf("%d", &search); for (c = 0; c < n; c++) { if (array[c] == search) { printf("%d is present at location %d.\n", search, c+1); break; } } if (c == n) printf("%d is not present in array.\n", search); return 0; }</pre> <p>Operations:(4M)</p>

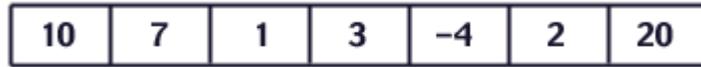


Figure %: The array we're searching

Lets search for the number 3. We start at the beginning and check the first element in t array. Is it 3?

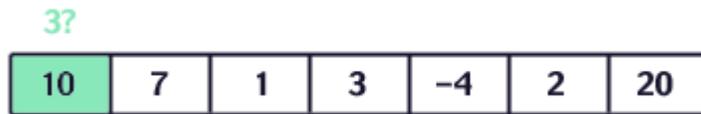


Figure %: Is the first value 3?

No, not it. Is it the next element?

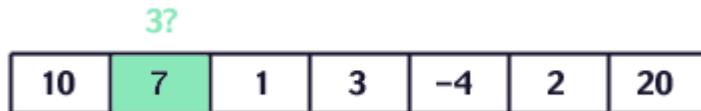


Figure %: Is the second value 3?

Not there either. The next element?

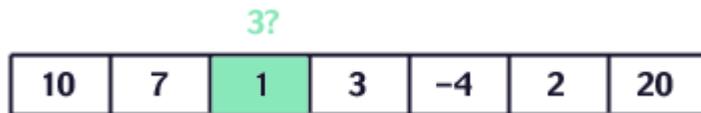


Figure %: Is the third value 3?

Not there either. Next?

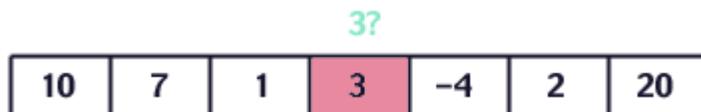


Figure %: Is the fourth value 3?

Hence the value 3 is found

2 **Explain the hash function techniques in detail. (13M)(May/June 2013) BTL 2**
Answer: Page:5.15-Dr.S.Poonkuzhali &P.Revathy

Introduction: (2M)

The implementation of hash tables is frequently called hashing. Hashing is a technique used for performing insertions, deletions and finds in constant average time.

- ✓ data structure is merely an array of some fixed size, containing the keys.
- ✓ key is a string with an associated value .We will refer to the table size as H_SIZE with the understanding that this is part of a hash data structure .
- ✓ The common convention is to have the table run from 0 to H_SIZE-1;
- ✓ Each key is mapped into some number in the range 0 to H_SIZE - 1 and placed appropriate cell. The mapping is called a hash function, which ideally should be simple to compute and should ensure that any two distinct keys get different cell

Example:(1M)

In this example, john hashes to 3, phil hashes to 4, dave hashes to 6, and mary hashes to 7.

0	
1	
2	
3	john 25000
4	phil 31250
5	
6	dave 27500
7	mary 28200
8	
9	

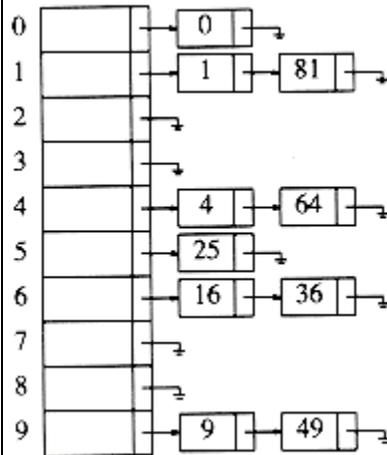
Open Hashing (Separate Chaining)(4M)

- ✓ The first strategy, commonly known as either open hashing, or separate chaining, keep a list of all elements that hash to the same value.
- ✓ If space is tight, it might be preferable to avoid their use. We assume for this se

that the keys are the first 10 perfect squares and that the hashing function is $\text{hash}(x) = x \bmod 10$.

Operations

- ✓ Insert
- ✓ Delete
- ✓ Traverse



An open hash table

Program:

(6M)

Type declaration for open hash table

```
typedef struct list_node *node_ptr;

struct list_node
{
    element_type element;
    node_ptr next;
};

typedef node_ptr LIST;

typedef node_ptr position;

/* LIST *the_list will be an array of lists, allocated later */

/* The lists will use headers, allocated later */
```

```
structhash_tbl
{
unsigned inttable_size;
LIST *the_lists;
};

Initialization routine for open hash table

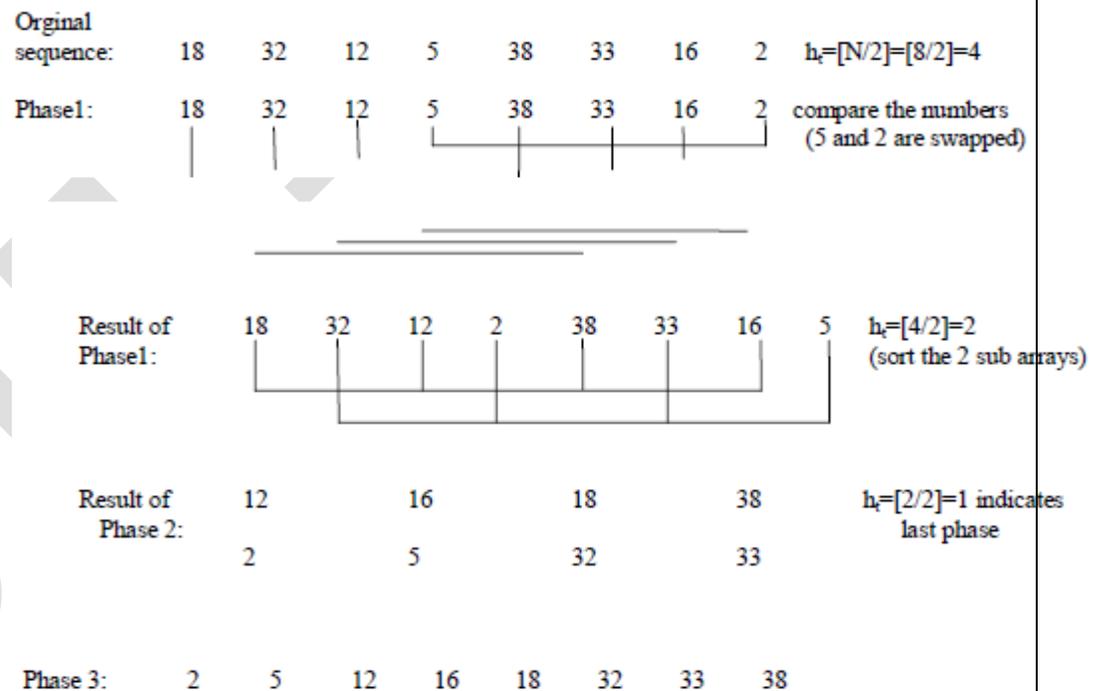
HASH_TABLE
initialize_table( unsigned inttable_size )
{
HASH_TABLE H;
int i;
if( table_size < MIN_TABLE_SIZE )
{
error("Table size too small");
return NULL;
}
/* Allocate table */
H = (HASH_TABLE) malloc ( sizeof (structhash_tbl) );
if( H == NULL )
fatal_error("Out of space!!!");
H->table_size = next_prime( table_size );
/* Allocate list pointers */
H->the_lists = (position *)
malloc( sizeof (LIST) * H->table_size );
if( H->the_lists == NULL )
```

	<pre>fatal_error("Out of space!!!"); /* Allocate list headers */ for(i=0; i<H->table_size; i++) { H->the_lists[i] = (LIST) malloc (sizeof (structlist_node)); if(H->the_lists[i] == NULL) fatal_error("Out of space!!!"); else H->the_lists[i]->next = NULL; } return H;</pre>
3	<p>Explain about shell sort techniques in detail with example. (13M)BTL 2 Answer: Page:5.15-Dr.S.Poonkuzhali &P.Revathy</p> <p>Shell Sort: (2M)</p> <ul style="list-style-type: none"> ✓ Founded by Donald Shell and named the sorting algorithm after himself in 1959 ✓ Shell sort works by comparing elements that are distant rather than adjacent elements in an array or list where adjacent elements are compared. ✓ Shell sort makes multiple passes through a list and sorts a number of equally sized sublists using the insertion sort. ✓ It is 5 times faster than the bubble sort and a little over twice as fast as the insertion sort, its closest competitor. ✓ Shellsort is sometimes referred as Diminishing increment sort. ✓ Shellsort uses a sequence h_1, h_2, \dots, h_t called the increment sequence. The increment sequence is given by $h_t = \lfloor N/2 \rfloor$. The incrementing sequence is calculated until $h_t = 1$. <p>Steps: (1M)</p> <ul style="list-style-type: none"> ✓ Calculate the incrementing sequence or gap by using the formula $h_t = \lfloor N/2 \rfloor$. ✓ Sort the elements present in the spacing of the incrementing sequence. ✓ Until $h_t = 1$ repeat the phases. ✓ The last phase will be basically a Insertion sort. <p>Algorithm for Shell sort(2M)</p> <pre>void Shellsort(Elementtype A[],int N)</pre>

```

{
int i , j , increment ;
elementtype tmp ;
for(elementtype=N / 2;increment > 0;increment /= 2)
{
for( i= increment ; i=increment; j -=increment)
if(tmp< A[ j]=A[j - increment]);
A[ j]=A[ j - increment];
Else Break;
A[ j]=tmp;
}
}
    
```

Problem Example:(5M)



Efficiency of Shell Sort: (3M)

- ✓ The worst case running time of shell sort is $O(N^2)$.
- ✓ The average case running time for shell sort using Hibbard's increments is $O(N \log N)$.

	<p>Advantages:</p> <ul style="list-style-type: none">✓ Efficient for medium size list.✓ The number of comparisons is less.✓ The running time of shell sort depends on the incrementing sequence. <p>Disadvantages:</p> <ul style="list-style-type: none">✓ Elements at odd and even places are compared only in the last step.
--	--

EC8351

ELECTRONIC CIRCUITS I

L T P C
3 0 3**OBJECTIVES:**

- To understand the methods of biasing transistors
- To design and analyze single stage and multistage amplifier circuits
 - To analyze the frequency response of small signal amplifiers
- To design and analyze the regulated DC power supplies.
- To troubleshoot and fault analysis of power supplies.

UNIT I BIASING OF DISCRETE BJT, JFET AND MOSFET

9

BJT– Need for biasing - DC Load Line and Bias Point – DC analysis of Transistor circuits - Various biasing methods of BJT – Bias Circuit Design - Thermal stability - Stability factors - Bias compensation techniques using Diode, thermistor and Sensistor – Biasing BJT Switching Circuits. JFET - DC Load Line and Bias Point - Various biasing methods of JFET - JFET Bias Circuit Design - MOSFET Biasing - Biasing FET Switching Circuits.

UNIT II BJT AMPLIFIERS

9

Small Signal Hybrid π equivalent circuit of BJT – Early effect - Analysis of CE, CC and CB amplifiers using Hybrid π equivalent circuits - AC Load Line Analysis- Darlington Amplifier - Bootstrap technique - Cascade, Cascode configurations - Differential amplifier, Basic BJT differential pair – Small signal analysis and CMRR.

UNIT III SINGLE STAGE FET, MOSFET AMPLIFIERS

9

Small Signal Hybrid π equivalent circuit of FET and MOSFET - Analysis of CS, CD and CG amplifiers using Hybrid π equivalent circuits - Basic FET differential pair- BiCMOS circuits.

UNIT IV FREQUENCY RESPONSE OF AMPLIFIERS

9

Amplifier frequency response – Frequency response of transistor amplifiers with circuit capacitors – BJT frequency response – short circuit current gain - cut off frequency – f_{α} , f_{β} and unity gain bandwidth – Miller effect - frequency response of FET - High frequency analysis of CE and MOSFET CS amplifier - Transistor Switching Times.

UNIT V POWER SUPPLIES AND ELECTRONIC DEVICE TESTING

9

Linear mode power supply - Rectifiers - Filters - Half-Wave Rectifier Power Supply - Full-Wave Rectifier Power Supply - Voltage regulators: Voltage regulation - Linear series, shunt and switching Voltage Regulators - Over voltage protection - BJT and MOSFET – Switched mode power supply (SMPS) - Power Supply Performance and Testing - Troubleshooting and Fault Analysis, Design of Regulated DC Power Supply.

TOTAL: 45 PERIODS**OUTCOMES:**

After studying this course, the student should be able to:

- Acquire knowledge of Working principles, characteristics and applications of BJT and FET Frequency response characteristics of BJT and FET amplifiers
- Analyze the performance of small signal BJT and FET amplifiers - single stage and multi stage amplifiers
- Apply the knowledge gained in the design of Electronic circuits

TEXT BOOKS:

1. Donald. A. Neamen, Electronic Circuits Analysis and Design, 3rd Edition, Mc Graw Hill Education (India) Private Ltd., 2010. (Unit I-IV)
2. Robert L. Boylestad and Louis Nasheresky, —Electronic Devices and Circuit Theory, 11th Edition, Pearson Education, 2013. (Unit V)

REFERENCES

1. Millman J, Halkias.C and Sathyabrada, Electronic Devices and Circuits, 4th Edition, Mc Graw Hill Education (India) Private Ltd., 2015.
2. Salivahanan and N. Suresh Kumar, Electronic Devices and Circuits, 4th Edition, Mc Graw Hill Education (India) Private Ltd., 2017.
3. Floyd, Electronic Devices, Ninth Edition, Pearson Education, 2012.
4. David A. Bell, Electronic Devices & Circuits, 5th Edition, Oxford University Press, 2008.
5. Anwar A. Khan and Kanchan K. Dey, A First Course on Electronics, PHI, 2006.
6. Rashid M, Microelectronics Circuits, Thomson Learning, 2007.

Subject Code: EC8351

Year/Semester: II /03

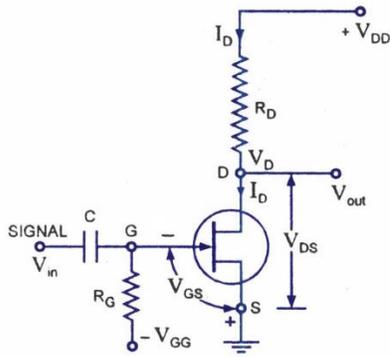
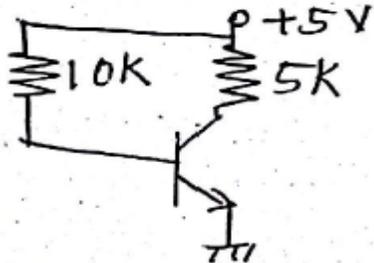
Subject Name: ELECTRONIC CIRCUITS I

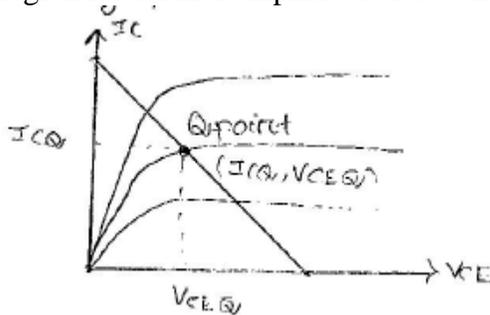
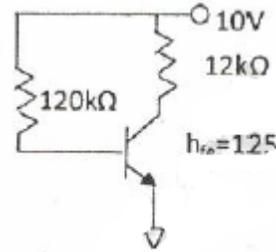
Subject Handler: Mr.R.Thandaiah Prabu

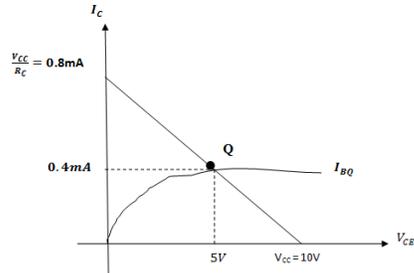
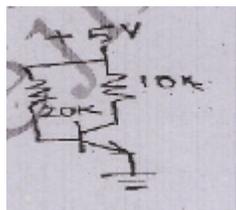
UNIT I -BIASING OF DISCRETE BJT, JFET AND MOSFET

BJT– Need for biasing - DC Load Line and Bias Point – DC analysis of Transistor circuits - Various biasing methods of BJT – Bias Circuit Design - Thermal stability - Stability factors - Bias compensation techniques using Diode, thermistor and Sensistor – Biasing BJT Switching Circuits- JFET - DC Load Line and Bias Point - Various biasing methods of JFET - JFET Bias Circuit Design - MOSFET Biasing - Biasing FET Switching Circuits.

PART * A

Q.No.	Questions
1.	<p>What is Diode Compensation? (April 2018) BTL1 In diode compensation, a temperature sensitive device called diode is used to compensate the variation in V_{BE} or I_{CO}.</p>
2	<p>Sketch the fixed biasing circuit of JFET. (April 2018) BTL1</p> 
3	<p>List out the three-stability factor. (April 2017) Define stability factor. (Nov - 2015) BTL1 Stability factor is defined as the rate of change of collector current I_C, with respect to collector base leakage current I_{CO}, base current I_B and current gain β respectively, when other 2 values are constant. $S = \frac{\partial I_C}{\partial I_{CO}} = \frac{dI_C}{dI_{CO}} = \frac{\Delta I_C}{\Delta I_{CO}}$ $S' = \frac{\partial I_C}{\partial V_{BE}} = \frac{\Delta I_C}{\Delta V_{BE}}$ $S'' = \frac{\partial I_C}{\partial \beta} = \frac{\Delta I_C}{\Delta \beta}$</p>
4	<p>Find out the collector current and base current of the circuit given in the following figure $h_{fe} = 80$, $V_{be(on)} = 0.7$ V. (April 2017) BTL3</p>  <p>Apply KVL to input loop</p>

	$V_{cc} = I_b R_b + V_{be}$ $5 = I_b * 10k + 0.7$ $I_b = (5 - 0.7) / 10k = 0.43mA$ $I_c = h_{fe} * I_b = 34.4mA$
5	<p>What is operating point? (Nov-2017) (Nov 2016) (May-2016) (Dec 2011) What is the function of Q point? (Dec -2013) BTL1 The set of DC voltage V_{CEQ} and current I_{CQ} suitably selected to operate the transistor in active region for faithful amplification is called Q- point or operating point.</p> 
6	<p>What is thermal runaway? (Nov-2017) BTL1 Due to the self-heating at the collector junction, the collector current rises. This causes damage to the device. This phenomenon is called thermal runaway.</p>
7	<p>Give the methods of biasing JFET. (May-2016) BTL1 There are 3 methods for biasing a JFET,</p> <ol style="list-style-type: none"> 1. Fixed bias 2. Self-bias 3. Voltage divider bias
8	<p>What is impact of temperature on drain current of MOSFET? (Nov-2016) BTL1 The impact of temperature on drain current of MOSFET is the drain current varies with temperature. The change in I_D in temperature range for N-channel is over 20% being slightly lower than P-channel device. Drain current decreases as temperature increases because MOSFET is a negative temperature co-efficient device.</p>
9	<p>List out the importance of selecting the proper operating point. (April-2015) BTL1 In order to produce distortion-free output in amplifier circuits, the supply voltages and resistances in the circuit must be suitably chosen. These voltages and resistances establish a set of DC voltage V_{CEQ} and current I_{CQ} to operate the transistor in the active region are called quiescent values which determine the Q-point of the transistor.</p>
10	<p>Draw a DC load line of the circuit shown in Figure. (April-2015) BTL 3</p>  <p>For drawing DC load line, the two end points viz maximum VCE point (at $I_C = 0$) and maximum</p>

	<p>IC point (at $V_{CE} = 0$) are required. Maximum $V_{CE} = V_{CC} = 10\text{ V}$ Apply KVL to base emitter loop find I_B and I_C The optimum operating point lies at the mid-point of the DC load line</p> 
11	<p>Why is the operating point selected at the middle of the active region? (Nov - 2015) BTL2 In order to get the faithful amplification of the signals, operating point has to be fixed at the middle of the DC load line. i.e. in the active region.</p>
12	<p>Find out the collector current and base current of circuit given in the fig $h_{fe} = 100$, $V_{be(ON)} = 0.7\text{V}$ (Nov-2014) BTL3</p>  <p>Apply KVL to collector to emitter loop $V_{CC} = I_C R_C + V_{CE}$</p> <p>Apply KVL to input loop $V_{CC} = I_B R_B + V_{BE}$</p> $I_B = \frac{V_{CC} - V_{BE}}{R_B}$ $= \frac{5 - 0.7}{20 \times 10^3}$ $I_B = 215 \mu\text{A}$ $I_C = h_{fe} I_B$ $= 100 \times 215 \times 10^{-6}$ $I_C = 21.5 \text{ mA}$
13	<p>What is the operating region of N-channel MOSFET and how do you identify the operating region? (Nov-2014). BTL1 The operating regions of N- channel MOSFET are</p> <ol style="list-style-type: none"> Cut-off region

	<ol style="list-style-type: none"> 2. Ohmic region 3. Active region 4. Saturation region
14	<p>What is thermal stability? (Dec -2013) BTL1</p> <p>The steady state temperature rise in the collector junction is proportional to the power dissipated at the junction. Condition for thermal stability is the rate at which heat is released at the collector should not exceed the rate at which the heat can be dissipated under steady state conditions.</p> $\frac{\partial P_c}{\partial T_j} = 1/\phi$
15	<p>Determine the value of R_s and R_c for a collector to base bias circuit for the specified condition $V_{CC} = 15\text{ V}$, $V = 5\text{ V}$, $I_c = 5\text{ mA}$ and $\beta = 100$ (Dec- 2014) BTL3</p> <p>Apply KVL to input loop $V_{CC} = I_b R_b + V_{be}$ $I_c = h_{fe} I_b$ Apply KVL to output loop $V_{CC} = I_c R_c + V_{ce}$</p>
16	<p>What are the factors against which an amplifier needs to be stabilized? (Dec- 2014) BTL1</p> <p>The q point must be stabilized at the Centre of the active region of the output Characteristics.</p> <ol style="list-style-type: none"> 1. Stabilize the collector current against the temperature variations. 2. Make the q point independent of the transistor parameters. 3. When the transistor is replaced, it must be of same type. 4. Stabilize the Collector current against the variation in V_{BE}
17	<p>What is the need for biasing in transistor amplifier. (May 2011) BTL1</p> <p>To use the transistor in any application it is necessary to provide sufficient Voltage and current to operate the transistor. This is called biasing.</p>
18	<p>Give the stability factor S for the fixed bias circuit. (May 2007) BTL1</p> <p>The stability factor for the fixed bias circuit is, $S = 1 + \beta$</p>
19	<p>How does the thermistor compensation work? BTL1</p> <p>The thermistor has a negative temperature coefficient i.e., its resistance decreases with the increase in temperature. So, any excess collector current is decreased because of the reduction in the active current through the device.</p>
20	<p>Write a major difference between JFET and E-MOSFET biasing. BTL1</p> <p>Biasing circuits for E-MOSFET are similar to the circuit used for JFET biasing. The primary difference between the two is the fact that E-MOSFET only permits operating points with positive value of V_{GS} for n channel and negative value of V_{GS} for p channel.</p>
21	<p>What do you understand by DC & AC load line? (Dec 2016) BTL2</p> <p>DC Load Line: It is the line on the output characteristics of a transistor circuit which gives the values of I_c & V_{ce} corresponding to zero signal (or) DC Conditions.</p> <p>AC Load Line: This is the line on the output characteristics of a transistor circuit which gives the values of I_c & V_{ce} when signal is applied.</p>
22	<p>When does a transistor act as a switch? BTL1</p> <p>The transistor acts as a switch when it is operated at either cut off region or Saturation region.</p>
23	<p>What do you mean by punch through? (June 2014) BTL1</p> <p>On increasing the Reverse bias voltage then at a time instant the width of the base becomes zero and this effect is called punch through effect and that reverse bias voltage is called punch</p>

	through voltage.
24	<p>State the two techniques used in the stability of the Q point. BTL 1</p> <p>Stabilization technique: This refers to the use of resistive biasing circuit which allows I_B to vary so as to keep I_C relatively constant with variations in I_{CO} and V_{BE}.</p> <p>Compensation techniques: This refers to the use of temperature sensitive devices such as thermistors diodes. They provide compensating voltages and currents to maintain operating point constant.</p>
25	<p>Why transistor is called as current controlled device? BTL1</p> <p>The output characteristics of the transistor depend on the input current. So, the transistor is called a current controlled device.</p>
PART * B	
1	<p>Explain voltage Divider bias method of BJT and derive an expression for Stability Factors. (13M) (April 2018) BTL1</p> <p>Answer: Page 200 - S. Salivahanan & 1.25- Bakshi</p> <p>Voltage Divider Bias: voltage divided - two parallel resistors – Self Biased –Biased by itself- Best biasing method (2M)</p> <p>Circuit diagram: DC voltage source – Biasing Resistors – CE Configuration – Emitter ground (2M)</p> <p>Dc equivalent circuit: Set AC voltage Zero – Open Circuit Capacitors – Draw DC Equivalent Circuit (2M)</p> <p>Stability factor definition: Rate of Change of I_c with respect to I_b - Rate of Change of I_c with respect to V_{be} - Rate of Change of I_c with respect to β. (1M)</p> <p>Stability Factor S: $S=1+\beta$ (2M)</p> <p>Stability Factor S': $S'=-\beta/(R_b+(1+\beta)R_e)$ (2M)</p> <p>Stability Factor S'': $S''=S I_c/\beta(1+\beta)$ (2M)</p>
2	<p>With neat diagram explain the working of self-bias and voltage divider bias for common source amplifier. (13M) (April 2018) BTL1</p> <p>Answer: Page 239 - S. Salivahanan & 2.6- Bakshi</p> <p>Self-Bias: Voltage divided - two parallel resistors – Self Biased –Biased by itself- Best biasing method–good stability factor (4M)</p> <p>Circuit diagram: DC voltage source – Biasing Resistors – CS Configuration – Source ground (3M)</p> <p>Dc equivalent circuit Set AC voltage Zero – Open Circuit Capacitors – Draw DC Equivalent Circuit (3M)</p> <p>Derivation and Explanation : KVL to Input loop – Output Loop – Find $V_{gs} - I_D$ (3M)</p>
3	<p>With neat diagram explain the source and drain resistance biasing of MOSFET. (13M) (Nov- 2017) BTL1</p> <p>Answer: Page 239 - S. Salivahanan & 2.25- Bakshi</p>

	<p>Source and drain resistance Bias: Bias- Source and drain resistance – good stability than fixed bias (4M)</p> <p>Circuit diagram: DC voltage source – Biasing Resistors –drain to source resistance- CS Configuration – Source ground (3M)</p> <p>Dc equivalent circuit: Set AC voltage Zero – Open Circuit Capacitors – Draw DC Equivalent Circuit (3M)</p> <p>Derivation and Explanation: KVL to Input loop – Output Loop – Find $V_{gs} - I_D$ (3M)</p>
4	<p>Derive the stability factors for voltage divider bias circuit and give reason why it is advantageous then fixed bias circuit. (13M) (April-2017) BTL3 Answer: Page 200 - S. Salivahanan & 1.25- Bakshi</p> <p>Voltage Divider Bias: voltage divided - two parallel resistors – Self Biased –Biased by itself- Best biasing method (2M)</p> <p>Circuit diagram: DC voltage source – Biasing Resistors – CE Configuration – Emitter ground (2M)</p> <p>Dc equivalent circuit: Set AC voltage Zero – Open Circuit Capacitors – Draw DC Equivalent Circuit (2M)</p> <p>Stability factor definition: Rate of Change of I_c with respect to I_b - Rate of Change of I_c with respect to V_{be} - Rate of Change of I_c with respect to β. (2M)</p> <p>Stability Factor S: $S=1$ (1M)</p> <p>Stability Factor S': $S' = -\beta / (R_b + (1 + \beta)R_e)$ (1M)</p> <p>Stability Factor S'': $S'' = S I_c / \beta (1 + \beta)$ (1M)</p> <p>Advantages: Better stability - Simple circuit. (2M)</p>
5	<p>Draw a circuit which uses a diode to compensate for changes in I_{c0}. Explain how stabilization is achieved in the circuit. (6M) (April-2017) BTL3 Answer: Page 217 - S. Salivahanan & 1.49- Bakshi</p> <p>Bias Compensation: Compensating - change in Q point - temperature effects - using temperature sensitive devices - diodes, thermistor, Sensistor. (1M)</p> <p>Circuit Diagram: Diode compensation – Diode – emitter – compensate I_{C0} – Base – Compensate I_b (1M)</p> <p>Base Current Compensation: $I_b = I - I_0$ (2M)</p> <p>Explanation: Temperature Increases- V_{BE} decreases- I_b increases- I_c Increases- diode current increases – Base current decreases – collector current decreases – compensation done (2M)</p>
6	<p>Briefly explain the reason for keeping the operating point of a transistor as fixed. (4M) (April-2017) BTL1 Answer: Page 184 - S. Salivahanan & 1.6- Bakshi</p> <p>Need for Biasing: Faithful amplification – Transistor as Amplifier – Distortion less amplification (1M)</p>

	<p>Compensation: Compensating - change in Q point - temperature effects - temperature sensitive devices - diodes, thermistor, sensistors. (1M)</p> <p>Stabilization: stabilizing - Q point - proper supply voltage - resistors (1M)</p> <p>Optimum Q point: Middle of DC load line. (1M)</p>
7	<p>Compare the methods of biasing using BJT in terms of their stability factors. (13M) (May-2016) BTL2 Answer: Page 1.106 – T.Joel</p> <p>Need for Biasing: Faithful amplification – Transistor as Amplifier – Distortion less amplification (1M)</p> <p>Types of Biasing: Stabilizing - Q point - active region - faithful amplification (2M)</p> <p>Fixed bias: Fixed Voltage – Base Bias – Poor Stability (1M)</p> <p>Collector to base bias – Collector to base Resistance – better stability than fixed bias (1M)</p> <p>Collector to emitter feedback bias – Collector to emitter Resistance – better stability than fixed bias (2M)</p> <p>Collector to base bias with Re- Collector to base Resistance –Emitter Resistance- better stability than fixed bias (2M)</p> <p>Collector to emitter feedback bias with Re- Collector to emitter Resistance –Emitter Resistance - better stability than fixed bias (2M)</p> <p>Voltage divider bias- voltage divided - two parallel resistors – Self Biased –Biased by itself- Best biasing method – Good stability Factor (2M)</p>
8	<p>With neat diagrams, explain the bias compensation techniques and state is advantages and disadvantages. (10M) (May-2016) BTL1 Answer: Page 214 - S. Salivahanan & 1.49- Bakshi</p> <p>Compensation: Compensating - change in Q point - temperature effects - temperature sensitive devices - diodes, thermistor, sensistors. (1M)</p> <p>Stabilization: stabilizing - Q point - proper supply voltage - resistors (1M)</p> <p>Bias compensation methods:</p> <p>Diode compensation: Diode compensation – Diode – emitter – compensate I_{C0} – Base – Compensate I_b (2M)</p> <p>Thermistor compensation: Thermistor at base- Negative temperature Coefficient – Resistance decreases as Temperature Increases- compensate I_c (2M)</p> <p>Sensistor compensation: Sensistor at base- Positive temperature Coefficient - Resistance increases as Temperature decreases-Compensate I_c (2M)</p> <p>Advantages: Compensate Variation in I_c – bias stabilization (1M)</p> <p>Disadvantage: Complex Circuit (1M)</p>
9	<p>Analyze a BJT with a voltage divider bias circuit and determine the change in the Q-point with a variation in β when the circuit contains an emitter resister. Let the biasing resistors be $R_{B1} = 56 \text{ K}\Omega$, $R_{B2} = 12.2 \text{ K}\Omega$, $R_c = 2 \text{ K}\Omega$, $R_E = 0.4 \text{ K}\Omega$, $V_{cc} = 10 \text{ V}$, $V_{be} (\text{on}) = 0.7\text{V}$ and</p>

$\beta = 100$. (13M) (Nov-2016) BTL4
Answer: Page 338 - Donald.

Voltage Divider Bias: voltage divided - two parallel resistors – Self Biased –Biased by itself- Best biasing method
 (1M)

Circuit diagram: DC voltage source – Biasing Resistors – CE Configuration – Emitter ground
 (1M)

Dc equivalent circuit: Set AC voltage Zero – Open Circuit Capacitors – Draw DC Equivalent Circuit
 (1M)

Thevenin's Resistance: $R_{th} = R_1 R_2 / (R_1 + R_2) = 10k$ (1M)

KVL: Input loop and solve, $I_{BQ} = 21.6\mu A$ (1M)

Collector Current: $I_c = \beta I_b$ will give, $I_{CQ} = 2.16mA$ (2M)

Emitter Current: $I_{EQ} = I_{CQ} + I_{BQ} = 2.18mA$ (2M)

KVL: Output Loop – Collector to emitter voltage- $V_{CEQ} = 4.81V$ (2M)

Circuit Diagram: Voltage Divider Bias Circuit – With calculated Values (2M)

10 Consider the circuit shown below with transistor parameters $I_{DSS} = 12mA$, $V_p = -4V$, and $\lambda = 0.008 V^{-1}$. Determine the small- signal voltage gain $A_v = V_o/V_i$. (13M) (Nov-2016) BTL3

Answer: Page 265 - Donald.

Self-Bias: Voltage divided - two parallel resistors – Self Biased –Biased by itself- Best biasing method–good stability factor (2M)

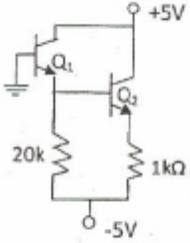
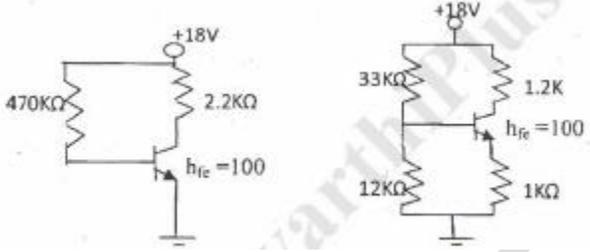
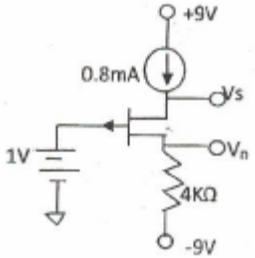
Circuit diagram: DC voltage source – Biasing Resistors – CS Configuration – Source ground (2M)

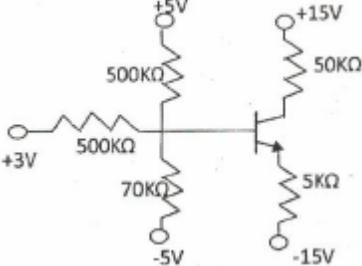
Dc equivalent circuit Set AC voltage Zero – Open Circuit Capacitors – Draw DC Equivalent Circuit (1M)

Derivation and Explanation : KVL to Input loop – Output Loop – Find $V_{gs} - I_D$ (1M)

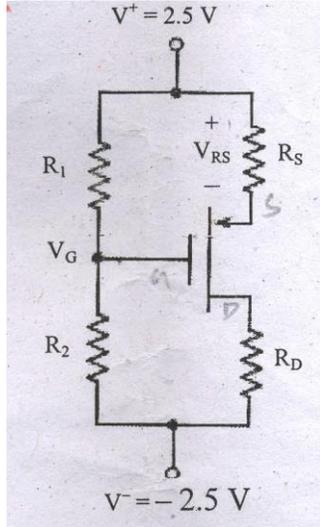
Calculation: $V_{gsQ} = -2V - I_{DQ} = 3mA - g_m = 3mA/V - r_o = 41.7k, A_v = -4.66$ (7M)

11 The parameters for each transistor in the circuit in Figure. Are $h_{fe} = 100$ and $V_{be} = 0.7 V$. determine the Q- point values of base, collector and emitter currents in Q1 and Q2. (10M) (April - 2015) BTL3

	 <p>Answer: Page 366 - Donald.</p> <p>Dc equivalent circuit Set AC voltage Zero – Open Circuit Capacitors – Draw DC Equivalent Circuit (2M)</p> <p>KVL to input and output loop: Collector Current – Base Current – Emitter Current (2M)</p> <p>Optimum Q point Calculation: Find V_{CEmax}, I_{Cmax} – Plot – Join two points – DC load Line – Optimum Q point – Middle of DC Load line. (3M)</p> <p>Practical Q point: Find Base Current – Collector current $I_{cQ} = \beta * I_b$ – Substitute Output loop equation – Find V_{CEQ}- Plot (3M)</p>
<p>12</p>	<p>Determine the change in collector current produced in each bias referred to in figures. when the circuit temperature raised from 25⁰ C to 105⁰C and $I_{cbo} = 15 \text{ nA}$ at 25 ⁰C. (13M) (April - 2015) BTL3</p>  <p>Answer: Page 239 - S. Salivahanan.</p> <p>Effect of Temperature in Collector Current: I_{co} doubles - every 10⁰ rises - temperature. (2M)</p> <p>Dc equivalent circuit Set AC voltage Zero – Open Circuit Capacitors – Draw DC Equivalent Circuit (2M+2M)</p> <p>KVL to input and output loop: Collector Current – Base Current – Emitter Current (2M)</p> <p>Change in collector current: Changes with respect to temperature change – compare (3M)</p>
<p>13</p>	<p>Determine the quiescent current and voltage values in a p-channel JFET circuit. (10M) (April - 2015) BTL3</p>  <p>Answer: Page 189 - Donald</p> <p>Dc equivalent circuit Set AC voltage Zero – Open Circuit Capacitors – Draw DC Equivalent Circuit (2M)</p>

	<p>KVL to input and output loop: Collector Current – Base Current – Emitter Current (1M) Calculation: Gate source Voltage-$V_{gs}=1.086V$ – Drain Source voltage - $V_{sd}=5.71V$ (4M+4M)</p>
14	<p>The circuit in Figure let $h_{fe} = 100$. Find V_{th} and R_{th} for the base circuit. Determine I_{cQ} and V_{ceQ}. Draw the DC load line. (13M) (April - 2015) BTL3</p>  <p>Answer: Page 187- S. Salivahanan.</p> <p>Dc equivalent circuit Set AC voltage Zero – Open Circuit Capacitors – Draw DC Equivalent Circuit (2M) KVL to input and output loop: KVL – Input - output loop (2M) DC Load Line: $I_c=0$ - find V_{ce} - $V_{ce}=0$ - Find I_c - Plot two points - join - line - DC load line. (6M) Optimum Q point Calculation: DC load Line – Optimum Q point – Middle of DC Load line. (1M) Practical Q point: Find Base Current – Collector current $I_{cQ} = \beta * I_b$ – Substitute Output loop equation – Find V_{CEQ}- Plot (2M)</p>
15	<p>Why the biasing is necessary in BJT amplifier? Explain the concept of DC & AC load line with neat diagram. How will you select the operating point, explain it using CE amplifier characteristics? (13M) (Nov – 2015) BTL2 Answer: Page 184 - S. Salivahanan & 1.9- Bakshi</p> <p>Need for Biasing: Faithful amplification – Transistor as Amplifier – Distortion less amplification (1M) Dc equivalent circuit Set AC voltage Zero – Open Circuit Capacitors – Draw DC Equivalent Circuit (2M) KVL to input and output loop: KVL – Input - output loop (2M) DC Load Line: $I_c=0$ - find V_{ce} - $V_{ce}=0$ - Find I_c - Plot two points - join - line - DC load line. (6M) Optimum Q point Calculation: DC load Line – Optimum Q point – Middle of DC Load line. (1M) Practical Q point: Find Base Current – Collector current $I_{cQ} = \beta * I_b$ – Substitute Output loop equation – Find V_{CEQ}- Plot (2M) AC Load Line: AC equivalent Resistance – Update V_{CE}, I_c- Plot – Join two points – AC load line (2M)</p>
	PART * C
1	<p>Design the circuit given below such that $I_{DQ} = 100\mu A$, $V_{SDQ} = 3V$, and $V_{RS} = 0.8V$. Note that V_{RS} is the voltage across the source resistor R_s. The value of the larger bias resistor R_1, R_2 is to be $200K\Omega$. Transistor parameters are $K_p = 100\mu A/V^2$, and $V_{TP} = -0.4V$, the conduction</p>

parameter varies by ± 5 percent. (15M) (Nov 2016) BTL3



Answer: Page 147 - Donald.

Dc equivalent circuit Set AC voltage Zero – Open Circuit Capacitors – Draw DC Equivalent Circuit (2M)

KVL to input and output loop: KVL – Input - output loop (2M)

Calculation: Gate source voltage - $V_{sg}=1.4V$, Gate voltage - $V_g=0.3V$, Bias current - $I_{bias}=0.014mA$, (6M)

Resistance values: $R_1=157K$ - $R_s=8k$ - $R_d=12K$ - $V_g=0.278V$ (5M)

Derive the stability factor of self-biasing circuit of BJT. (15M) (Nov- 2014) BTL1

Answer: Page 239 - S. Salivahanan & 1.25- Bakshi

Voltage Divider Bias: voltage divided - two parallel resistors – Self Biased –Biased by itself- Best biasing method (2M)

Circuit diagram: DC voltage source – Biasing Resistors – CE Configuration – Emitter ground (2M)

2 Dc equivalent circuit: Set AC voltage Zero – Open Circuit Capacitors – Draw DC Equivalent Circuit (2M)

Stability factor definition: Rate of Change of I_c with respect to I_b - Rate of Change of I_c with respect to V_{be} - Rate of Change of I_c with respect to β . (2M)

Stability Factor S: $S=1$ (1M)

Stability Factor S': $S'=-\beta / (R_b+(1+\beta)R_e)$ (1M)

Stability Factor S'': $S'' = S I_c / \beta (1+\beta)$ (1M)

Advantages: Better stability - Simple circuit. (2M)

Design the emitter bias of BJT with $I_e = 2mA$, $V_{dc} = 18V$, $V_{ce} = 10V$ and $\beta = 150$ (15M) (Nov 2014) BTL1

Answer: Page 1.71 -T.Joel.

3 Dc equivalent circuit Set AC voltage Zero – Open Circuit Capacitors – Draw DC Equivalent Circuit (3M)

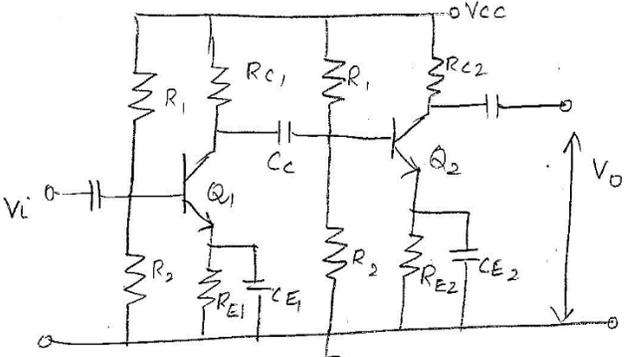
KVL to input and output loop: KVL – Input - output loop (3M)

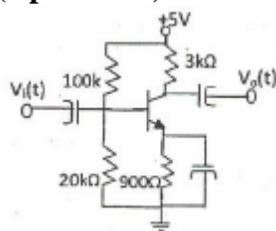
Calculation: All resistor values. (9M)

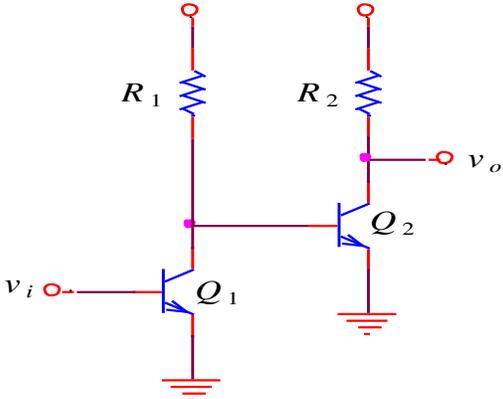
UNIT II –BJT AMPLIFIERS

Small Signal Hybrid π equivalent circuit of BJT – Early effect - Analysis of CE, CC and CB amplifiers using Hybrid π equivalent circuits - AC Load Line Analysis- Darlington Amplifier - Bootstrap technique - Cascade, Cascode configurations - Differential amplifier, Basic BJT differential pair – Small signal analysis and CMRR.

PART * A

Q.No.	Questions
1.	<p>Draw the circuit of cascade amplifier. (April 2018) BTL1 The RC Coupled cascade amplifier is</p> 
2.	<p>Why CE configuration is preferred for amplification? (April 2018) BTL1 CE configuration offers,</p> <ol style="list-style-type: none"> 1. High input impedance 2. Low output impedance 3. High voltage gain and 4. Moderate current gain. Hence it is preferred.
3.	<p>What is bypass and coupling capacitor? (Nov-2017) BTL1</p> <ol style="list-style-type: none"> 1. An emitter bypass capacitor CE is connected in parallel with the emitter resistance RE to provide a low reactance path to the amplified ac signal. 2. Input and output coupling capacitors are connected after the source and before the load to couple only the ac components and to block dc components.
4.	<p>What is the need for boost strapping? (Nov-2017) BTL1 In Darlington transistor pair circuits, the input impedance is reduced because of the biasing resistors in the circuit. To overcome this, decrease in the input resistance due to the biasing network, a small capacitor and resistance R3 are added in the circuit. This improves the input impedance of the Darlington pair circuit. Thus, the effect of increasing input impedance when voltage gain Av approaches unity is called Bootstrapping.</p>
5.	<p>State Millers' theorem. (April 2017) BTL1 Millers theorem states that, any impedance(z) connected between two nodes can be resolved into two components from each node to ground. The two impedances are $Z1 = Z/1-K$, $Z2 = ZK/K-1$; where K = voltage gain.</p>
6.	<p>List the values of input and output impedance of BJT small signal model. BTL 1 Input Impedance:</p> $r_{\pi} = \frac{\beta V_T}{I_{CQ}}$

	<p>Output Impedance:</p> $r_o = \frac{V_A}{I_{CQ}}$
7.	<p>Define CMRR of BJT differential amplifier. How will you improve it? (April-2015) BTL1</p> <p>The ability of differential amplifier to reject a common mode signal is expressed by a ratio called as common mode rejection ratio [CMRR]. It is defined as the ratio of differential voltage gain A_d to common mode voltage gain A_c. BTL1</p> $CMRR = \rho = \left \frac{A_d}{A_c} \right $ <p>Methods of improving CMRR:</p> <ol style="list-style-type: none"> 1. Constant current bias method. 2. Use of current mirror circuit. 3. Use of active load.
8.	<p>A small signal source $V_i(t) = 20\cos 20t + 30\sin 10^6t$ is applied to a transistor amplifier as shown in figure. The transistor has $h_{fe} = 150$, $r_o = \infty$ and $r_{\pi} = 3 \text{ K}\Omega$. Determine $V_o(t)$. (April-2015) BTL3</p>  <p> $A_v = -h_{fe} \cdot R_c / h_{ie}$ $h_{ie} = r_{\pi}$ $A_v = -150$ $V_o(t) = A_v \cdot V_i(t)$ $V_o(t) = -\{3000\cos 20t + 4500 \sin 10^6t\}$ </p>
9.	<p>How the amplifiers are classified according to the transistor configuration? (Nov 2015) BTL1</p> <p>BJT AMPLIFIERS:</p> <ol style="list-style-type: none"> 1. Common Emitter (CE) 2. Common Base (CB) 3. Common Collector (CC) <p>FET AMPLIFIERS:</p> <ol style="list-style-type: none"> 1. Common Source (CS) 2. Common Drain (CD) 3. Common Gate (CG)
10.	<p>Draw Darlington amplifier. BTL1</p>

	
11.	<p>Find out CMRR of differential amplifier with differential gain of 300 and common mode gain of 0.2. (Nov-2014) BTL1</p> $CMRR = \rho = \left \frac{A_d}{A_c} \right $ <p>Ans: CMRR = 63.52dB.</p>
12.	<p>What are the advantages of Darlington circuit? (Nov 2011) BTL1</p> <ol style="list-style-type: none"> 1. Very high current gain 2. Very high input impedance 3. Convenient and easy circuit configuration to use 4. Darlington pairs are widely available in a single package or they can be made from two separate transistors
13.	<p>What is common mode signal? BTL1</p> <p>The average of two input signals or voltages is called a common-mode signal. The gain with which it amplifies the common mode signal to produce the output is called common mode gain of the differential amplifier denoted as A_c.</p> $\text{Common mode voltage } V_c = \frac{V_1 - V_2}{2}$ $V_o \propto V_c$ $V_o = A_c \cdot V_c$ $\text{Gain } A_c = \frac{V_o}{V_c}$ <p>The common mode gain is expressed in decibel (dB) value as $A_c = 20 \log_{10}(A_c)$ in dB.</p>
14.	<p>What are the coupling schemes used in multistage amplifiers (April-2010) BTL1</p> <p>When amplifiers are cascaded it is necessary to use a coupling network between the output of one amplifier and the input of the following amplifier. This type of coupling is called as inter stage coupling. They serve the following purposes,</p> <p>It transfers the A.C output of one stage to the input of next stage It isolates the D.C conditions of one stage to next.</p> <p>The commonly used coupling schemes are,</p> <ol style="list-style-type: none"> 1. Resistance, capacitance (RC) coupling 2. Transformer coupling 3. Direct coupling
15.	<p>What is differential mode signal? BTL1</p> <p>The difference between the two input signals is generally called as differential signal or difference signal.</p>

	<p>Differential voltage $V_d = V_1 - V_2$ $V_o \propto V_d$ $V_o = A_d \cdot V_d$ Gain $A_d = \frac{V_o}{V_1 - V_2}$</p> <p>The differential gain is expressed in decibel (dB) value as $A_d = 20 \log_{10} (A_d)$ in dB.</p>
16.	<p>Define transconductance. (Nov 2008] BTL1 Transconductance, also known as mutual conductance is the ratio of the current change at the output port to the voltage change at the input port. It is written as g_m. For direct current, transconductance is defined as follows: $g_m = \frac{\Delta I_{out}}{\Delta V_{in}}$ For small signal alternating current, the definition is simpler $g_m = \frac{I_{CQ}}{V_T}$</p>
17.	<p>State Miller effect in terms of capacitance. (Dec-2006) BTL1 For any inverting amplifier, the input capacitance will be increased by a miller effect capacitance, sensitive to the gain of the amplifier and the inter electrode capacitance connected between the input and output terminals of the active device. $CM_i = (1 - AV) C_f$; $CM_o = C_f$</p>
18.	<p>What is meant by bootstrapping? (Dec-2003) BTL1 The effect of increasing input impedance when voltage gain A_v approaches unity is called Bootstrapping. R_{eff} - Effective input resistance. And $R_{eff} = R / (1 - A_v)$</p>
19.	<p>What is the need of differential amplifier? (April-2011) BTL1 The need for differential amplifier arises in many physical measurements, in medical electronics and in direct coupled amplifier applications. In this amplifier, there will be no output voltage resulting from thermal drifts or any other changes provided, change in both halves of the circuits are equal.</p>
20.	<p>Why emitter bypass capacitor CE is used in CE amplifier circuit. (April 2004) BTL1 An emitter bypass capacitor CE is connected in parallel with the emitter resistance RE to provide a low reactance path to the amplified ac signal. If it is not inserted, the amplified ac signal passing through RE will cause a voltage drop across it. This will reduce the output voltage, reducing the gain of the amplifier.</p>
21.	<p>State early effect in BJT. BTL1 The Early effect is the variation in the width of the base in a BJT due to a variation in the applied base-to-collector voltage. A greater reverse bias across the collector-base junction, for example, increases the collector-base depletion width, decreasing the width of the charge neutral portion of the base.</p>
22.	<p>What are the applications of a differential amplifier? BTL1</p> <ol style="list-style-type: none"> 1. To measure many physical quantities. 2. Can be used as a direct coupled amplifier. 3. Used in operational amplifier.
23.	<p>What are the advantages of differential amplifier? BTL1</p> <ol style="list-style-type: none"> 1. Very stable. 2. Low noise, low drift.

- 3. Variations in supply voltage, temperature etc. will not change the gain of the amplitude.
- 4. Does not require any coupling capacitor.
- 5. Frequency response is better.

24. **Draw the small signal equivalent circuit of CE amplifier. (April 2015) BTL1**

25. **Mention the important characteristics of CC circuit.(Dec 2013) BTL1**
- 1. Offers high input impedance upto 500K.
 - 2. It can be further improved by direct coupling schemes called Darlington and Bootstrapping.
 - 3. It offers output equal to input.
 - 4. Voltage gain is unity.

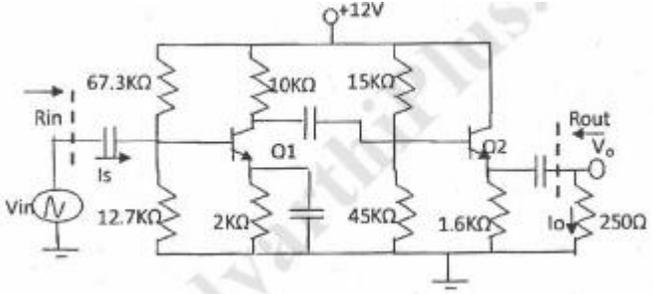
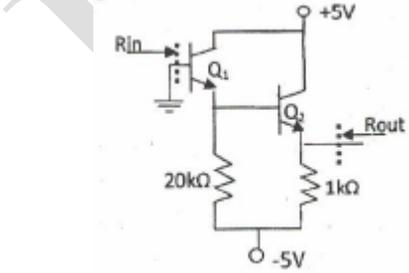
PART*B

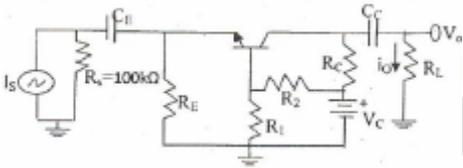
1. **Write the short notes on multi stage amplifier. Draw a two stage RC coupled amplifier and explain. Also compare cascade and Cascode amplifier. (13M) (April-2018) BTL1**
Answer: Page 440 – Donald & 3.25- Bakshi

Multistage amplifier: More than one transistor amplifier – Cascaded – Cascoded (2M)
Need: Improve input impedance - Improve voltage gain (2M)
Circuit Diagram: 2 stage RC coupled multistage amplifier (4M)
Comparison: Cascade – More than 2 CE amplifiers – Connected - series
 Cascode – One CE amplifier – One CB amplifier- Connected- parallel (2M)
Explanation: Transfers - one stage A.C output - Input of next stage
 Isolates - D.C conditions - One stage to next. (3M)

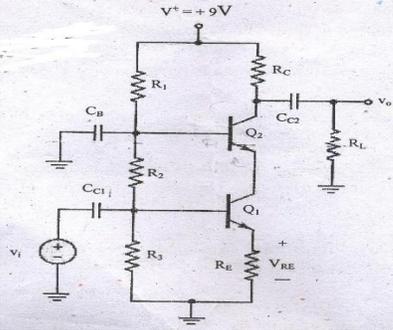
2. **Derive the expression for the voltage gain, current gain, input and output impedance of emitter follower amplifier. (13M) (April-2018) BTL1**

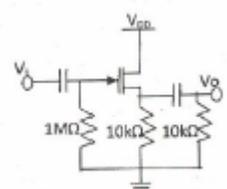
	<p>Answer: Page 424 – Donald & 3.14- Bakshi</p> <p>AC equivalent circuit: Short circuit - input and output, bypass coupling capacitors - Set DC voltage to zero. (2M)</p> <p>Small signal equivalent circuit: Replace transistor - equivalent small signal model. (2M)</p> <p>Small signal parameters: (1M)</p> <p>Input Impedance: Total Input resistances- $R_i = R_1 // R_2 // R_{ib}$ (2M)</p> <p>Output Impedance: Total Output Resistances - $R_o = r_{\pi} / (1 + \beta) // R_e // r_o$. (2M)</p> <p>Voltage Gain: Ratio - Output to input voltage. $A_v = \frac{(1 + \beta)(r_o // R_e)}{r_{\pi} + (1 + \beta)(r_o // R_e)} \left(\frac{R_i}{R_i + R_s} \right)$ (2M)</p> <p>Current Gain: Ratio - Output to input Current. $A_i = (1 + \beta)$ (2M)</p>
3.	<p>Draw the AC equivalent circuit of a CE amplifier with voltage divider bias and derive the expression for current gain, voltage gain, input impedance, output admittance and overall current gain. (13M) (April-2017) BTL1</p> <p>Answer: Page 400 – Donald & 3.4- Bakshi</p> <p>AC equivalent circuit: Short circuit - input and output, bypass coupling capacitors - Set DC voltage to zero. (2M)</p> <p>Small signal equivalent circuit: Replace transistor - equivalent small signal model. (2M)</p> <p>Small signal parameters: (1M)</p> <p>Input Impedance: Total Input resistances: $R_i = R_1 // R_2 // R_{\pi}$ (2M)</p> <p>Current Gain: Ratio - Output to input Current: $A_i = -h_{fe} = -g_m * r_{\pi}$ (2M)</p> <p>Output Impedance: Total Output Resistances: $R_o = R_c // r_o$. (2M)</p> <p>Voltage Gain: Ratio - Output to input voltage: $A_v = -g_m \left(\frac{R_1 // R_2 // r_{\pi}}{R_1 // R_2 // r_{\pi} + R_s} \right) (R_c // r_o)$ (2M)</p>
4.	<p>Explain the operation of cascade amplifier and derive and derive voltage gain, overall gain, Resistance overall current gain and output impedance. (13M) (April-2017) BTL1</p> <p>Answer: Page 440 – Donald & 3.25- Bakshi</p> <p>AC equivalent circuit: Short circuit - input and output, bypass coupling capacitors - Set DC voltage to zero. (2M)</p> <p>Small signal equivalent circuit: Replace transistor - equivalent small signal model. (2M)</p> <p>Small signal parameters: (1M)</p> <p>Input Impedance: Total Input resistances: $R_i = R_1 // R_2 // r_{\pi 1}$ (2M)</p> <p>Output Impedance: Total Output Resistances: $R_o = R_c 2$ (2M)</p> <p>Voltage Gain: Ratio - Output to input voltage: $A_v = g_{m1} * g_{m2} (R_c 1 // r_{\pi 2}) (R_c 2 // R_L) (R_i / (R_i + R_s))$ (2M)</p> <p>Current Gain: Ratio - Output to input Current: $A_i = A_{i1} * A_{i2}$ (2M)</p>
5.	<p>With a neat diagram explain the operation of differential amplifier and derive the necessary equations to calculate the CMRR. (13M) (Nov 2017) BTL1</p> <p>Answer: Page 789 – Donald & 3.35- Bakshi</p> <p>AC equivalent circuit: Short circuit - input and output, bypass coupling capacitors - Set DC</p>

	<p>voltage to zero. (2M)</p> <p>Small signal equivalent circuit: Replace transistor - equivalent small signal model. (2M)</p> <p>Small signal parameters:</p> <p>Common mode analysis: Common input – both transistors- $A_{cm} = (V_1 + V_2) / 2$ (3M)</p> <p>Differential Mode Analysis: Difference Mode – Different Input – A_{dm} (3M)</p> <p>Small signal Gain: Common Mode Gain A_C- Difference mode Gain A. (1M)</p> <p>Common Mode Rejection Ratio: $CMRR = A_d / A_c = \frac{1}{2}(1 + (1 + \beta)I_q R_o / V_{T\beta})$ (2M)</p>
<p>6.</p>	<p>Consider the circuit shown in figure with the parameters are $h_{fe} = 120$ and $V_A = \infty$.</p> <p>(1) determine the current gain, voltage gain, input impedance and output impedance</p> <p>(2) Find the maximum undistorted output voltage swing. (13M) (April-2015) BTL3</p>  <p>Answer: Page 440 - Donald.</p> <p>AC equivalent circuit: Short circuit - input and output, bypass coupling capacitors - Set DC voltage to zero. (2M)</p> <p>Small signal equivalent circuit: Replace transistor - equivalent small signal model. (2M)</p> <p>Small signal parameters: (1M)</p> <p>Input Impedance: Total Input resistances: $R_i = R_1 // R_2 // r_{\pi 1} = 10.23K$ (2M)</p> <p>Output Impedance: Total Output Resistances: $R_o = (R_{C1} + r_{\pi 2}) / (1 + \beta) // R_{E2} = 83.35k$ (2M)</p> <p>Voltage Gain: Ratio - Output to input voltage: $A_v = g_{m1} * g_{m2} (R_{C1} // r_{\pi 2}) (R_{C2} // R_L) (R_i / (R_i + R_s)) = -3.41$ (2M)</p> <p>Maximum Voltage swing: Maximum variation – Acceptable $\Delta I_c = 9.72mA, \Delta V_{ce} = 2.10V_c$ (2M)</p>
<p>7.</p>	<p>The parameter for each transistor in the circuit are $h_{fe} = 100$, $V_A = \infty$ and $V_{BE} (on) = 0.7 V$. Determine the input and output impedance. (8M) (April-2015) BTL3</p>  <p>Answer: Page 444 - Donald.</p> <p>AC equivalent circuit: Short circuit - input and output, bypass coupling capacitors - Set DC voltage to zero. (2M)</p>

	<p>Small signal equivalent circuit: Replace transistor - equivalent small signal model. (2M)</p> <p>Small signal parameters:</p> <p>Input Impedance: Total Input resistances $R_i = r_{\pi 1} + (1 + \beta) r_{\pi 2} = 2 \beta r_{\pi 2} = 122.2 \text{ k}$ (2M)</p> <p>Output Impedance: Total Output Resistances: $R_o = R_{e2} = 1 \text{ k}$ (2M)</p>
8.	<p>Draw the circuit diagram of bootstrapped emitter follower with its equivalent circuit, derive for its input and output impedance. (10M) (April-2015) BTL1</p> <p>Answer: Page 411 – S.Salivahanan & 3.24- Bakshi</p> <p>Circuit Diagram for Bootstrapped amplifier. (4M)</p> <p>Concept of Bootstrapping: Input impedance - infinite - voltage gain approaches unity. (2M)</p> <p>Condition for Bootstrapping: To achieve high input impedance $R_{eff} = R_3 / (1 - A_v)$ (4M)</p>
9.	<p>For the circuit shown in figure the transistor parameters are $h_{fe} = 125$, $V_A = \infty$, $V_{CC} = 18 \text{ V}$, $R_L = 4 \text{ k}\Omega$, $R_E = 3 \text{ k}\Omega$, $R_C = 4 \text{ k}\Omega$, $R_1 = 25.6 \text{ k}\Omega$ and $R_2 = 10.4 \text{ k}\Omega$. The input signal is a current source. Determine its small signal voltage gain, current gain, maximum voltage gain and input impedance. (13M) (April-2015) BTL3</p>  <p>Answer: Page 400 - Donald.</p> <p>AC equivalent circuit: Short circuit - input and output, bypass coupling capacitors - Set DC voltage to zero. (2M)</p> <p>Small signal equivalent circuit: Replace transistor - equivalent small signal model. (2M)</p> <p>Small signal parameters: (1M)</p> <p>Input Impedance: Total Input resistances $R_{ie} = r_{\pi} / (1 + \beta)$ (2M)</p> <p>Output Impedance: Total Output Resistances: $R_o = R_c = 4 \Omega$ (2M)</p> <p>Current Gain: Ratio - Output to input Current: $A_i = \beta / (1 + \beta) = 987$ (2M)</p> <p>Voltage Gain: Ratio - Output to input voltage: $A_v = g_m (R_c // R_L) = 39$ (2M)</p>
10.	<p>Calculate the small signal voltage gain of an emitter follower circuit. Given $\beta = 100$, $V_{BE(on)} = 0.7 \text{ V}$, $V_A = 80 \text{ V}$, $I_{CQ} = 0.793 \text{ mA}$, $V_{CEQ} = 3.4 \text{ V}$. (8M) (May16) BTL1</p> <p>Answer: Page 424 – Donald.</p> <p>AC equivalent circuit: Short circuit - input and output, bypass coupling capacitors - Set DC voltage to zero. (2M)</p> <p>Small signal equivalent circuit: Replace transistor - equivalent small signal model. (2M)</p> <p>Small signal parameters: (1M)</p> <p>Voltage Gain: Ratio - Output to input voltage:</p> $A_v = \frac{(1 + \beta)(r_o // R_e)}{r_{\pi} + (1 + \beta)(r_o // R_e)} \left(\frac{R_i}{R_i + R_s} \right)$ (2M) <p>Ans=0.96 (2M)</p>

11.	<p>With neat diagrams, explain the operation and advantages of Darlington pair circuit. (13M) (Nov-2016) BTL1 Answer: Page 444 – Donald & 3.22- Bakshi</p> <p>AC equivalent circuit: Short circuit - input and output, bypass coupling capacitors - Set DC voltage to zero. (2M)</p> <p>Small signal equivalent circuit: Replace transistor - equivalent small signal model. (2M)</p> <p>Small signal parameters: (1M)</p> <p>Input Impedance: Total Input resistances - $R_i = r_{\pi 1} + (1 + \beta_1) r_{\pi 2} = 2 \beta_1 * r_{\pi 2}$ (2M)</p> <p>Output Impedance: Total Output Resistances: $R_o = R_{e2}$ (2M)</p> <p>Current Gain: Ratio - Output to input Current: $A_1, A_2 \dots$</p> <p>Overall Current Gain: $A_i = \beta_1 * \beta_2$ (2M)</p> <p>Advantages: (1M)</p> <ol style="list-style-type: none"> 1. Large overall gain. 2. Higher input impedance <p>Disadvantages: (1M)</p> <ol style="list-style-type: none"> 1. The input resistance of the amplifier -decreased - shunting effect - biasing resistors. 2. High leakage current.
PART * C	
1.	<p>Draw the circuit of cascade amplifier (15M) (April 2018) BTL1 Answer: Page 440 – Donald & 3.25- Bakshi</p> <p>Circuit diagram of cascade amplifier (2M)</p> <p>AC equivalent circuit: Short circuit - input and output, bypass coupling capacitors - Set DC voltage to zero. (2M)</p> <p>Small signal equivalent circuit: Replace transistor - equivalent small signal model. (2M)</p> <p>Small signal parameters: (2M)</p> <p>Input Impedance: Total Input resistances - $R_i = R_1 // R_2 // r_{\pi 1}$ (2M)</p> <p>Output Impedance: Total Output Resistances: $R_o = R_{c2}$ (2M)</p> <p>Voltage Gain: Ratio - Output to input voltage: $A_v = g_{m1} * g_{m2} (R_{c1} // r_{\pi 2}) (R_{c2} // R_L) (R_i / (R_i + R_s))$ (3M)</p>
2.	<p>Analyze a basic common-base amplifier circuit and derive the expressions for its small-signal voltage gain, current gain, input impedance and output impedance. (15M) (Nov-2016) BTL1 Answer: Page 435 – Donald & 3.18- Bakshi</p> <p>Circuit diagram- CB Amplifier (2M)</p> <p>AC equivalent circuit: Short circuit - input and output, bypass coupling capacitors - Set DC voltage to zero. (2M)</p> <p>Small signal equivalent circuit: Replace transistor - equivalent small signal model. (2M)</p>

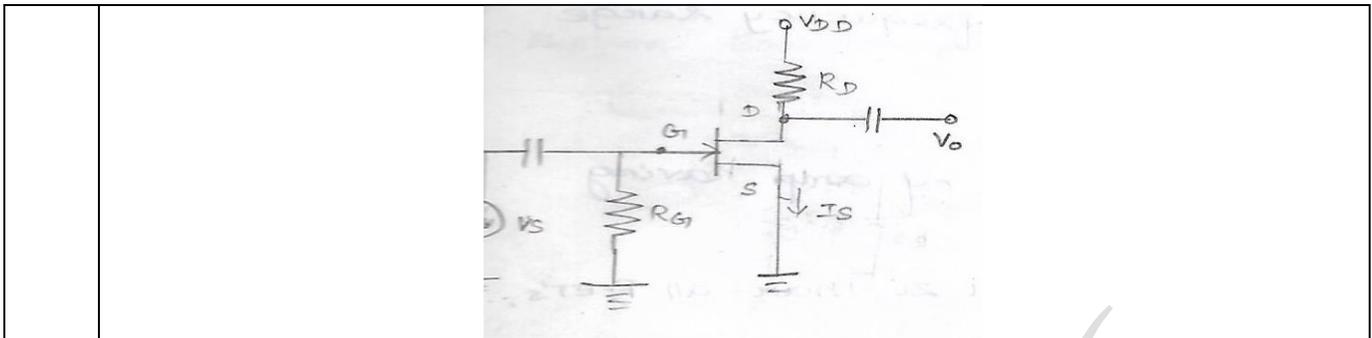
	<p>Small signal parameters: (1M)</p> <p>Input Impedance: Total Input resistances - $R_{ie} = r_{\pi} / (1 + \beta)$ (2M)</p> <p>Output Impedance: Total Output Resistances: $R_o = R_c$ (2M)</p> <p>Current Gain: Ratio - Output to input Current: $A_i = \beta / (1 + \beta)$ (2M)</p> <p>Voltage Gain: Ratio - Output to input voltage: $A_v = g_m (R_c // R_L)$ (2M)</p>
3.	<p>What are the changes in the AC characteristics of a common emitter amplifier when an emitter resistor and an emitter bypass capacitor are incorporated in the design? Explain with necessary equations. (15M) (May-2016) BTL1</p> <p>Answer: Page 400 – Donald & 3.14- Bakshi</p> <p>Circuit diagram: CE Amplifier with emitter resistor R_e (2M)</p> <p>AC equivalent circuit: Short circuit - input and output, bypass coupling capacitors - Set DC voltage to zero. (2M)</p> <p>Small signal equivalent circuit: Replace transistor - equivalent small signal model. (2M)</p> <p>Small signal parameters: (1M)</p> <p>Input Impedance: Total Input resistances - $R_i = R_1 // R_2 // R_{ib}$ (2M)</p> <p>Current Gain: Ratio - Output to input Current: $A_i = -h_{fe} = -g_m * r_{\pi}$ (2M)</p> <p>Output Impedance: Total Output Resistances: $R_o = R_c // r_o$. (2M)</p> <p>Voltage Gain: Ratio - Output to input voltage: $A_v = \left(-\frac{R_c}{R_e} \right)$ (2M)</p>
4.	<p>Design the cascode circuit shown below to meet the following specifications. $V_{ce1} = V_{ce2} = 2.5V$, $V_{re} = 0.7$, $I_{c1} = I_{c2} = 1mA$, and $I_{r1} = I_{r2} = I_{r3} = 0.10mA$. (15M) (Nov 2016) BTL3</p>  <p>Answer: Page 351 - Donald.</p> <p>Circuit diagram (1M)</p> <p>AC equivalent circuit: Short circuit - input and output, bypass coupling capacitors - Set DC voltage to zero. (2M)</p> <p>Small signal equivalent circuit: Replace transistor - equivalent small signal model. (2M)</p> <p>Determination of Unknown parameters: Apply KVL to input loop- Output loop (2M)</p> <p>Input Resistances: $R_3 = 14K$, $R_2 = 25K$, $R_1 = 51K$ ((4M)</p> <p>Emitter Resistance: $R_e = 0.7K$ (2M)</p> <p>Collector Resistance: $R_c = 3.3K$ (2M)</p>

UNIT III – SINGLE STAGE FET, MOSFET AMPLIFIERS	
Small Signal Hybrid π equivalent circuit of FET and MOSFET - Analysis of CS, CD and CG amplifiers using Hybrid π equivalent circuits - Basic FET differential pair- BiCMOS circuits.	
PART * A	
Q.No.	Questions
1.	<p>What is I_{DSS} in JFET? (April 2018) BTL1</p> <p>I_{DSS} is the reverse saturation current when $V_{gs}=0$. It is used for fixing Q point of JFET. It is related with Drain current by the formula, $I_D = I_{DSS}(1 - V_{gs}/V_p)^2$</p>
2	<p>Why MOSFET are used? (April 2018) BTL1</p> <p>MOSFET are used because,</p> <ol style="list-style-type: none"> 1. MOSFETs offers greater input impedance. MOSFETs typically offers about $10^{14} \Omega$ of impedance, sometimes greater. 2. Low transconductance (gain) 3. Voltage controlled. 4. MOSFETs can be operated in depletion type or enhancement type.
3	<p>What is BIMOS? (Nov-2017) BTL1</p> <p>Bipolar Transistors are having larger trans conductance. MOS transistors are having larger input impedance. Both this advantage can be exploited together to get high trans conductance and input impedance and is called BIMOS technology and the circuit is called BIMOS.</p>
4	<p>A self-biased P-Channel JFET has a pinch off voltage of 5V and $I_{DSS} = 12\text{mA}$. The supply voltage is 12 V. Determine the values of resistors R_D and R_S, so that $I_D = 5 \text{ mA}$ and $V_{DS} = 6\text{V}$. (Nov-2017) BTL1</p> <ol style="list-style-type: none"> 1. Finding V_{gs} using $I_D = I_{DSS}(1 - V_{gs}/V_p)^2$ 2. Apply KVL to input loop and find R_S 3. Apply KVL to output loop and find R_D
5	<p>List the features of BIMOS cascade amplifier. (April 2017) (Nov-2014) BTL1</p> <ol style="list-style-type: none"> 1. Bipolar transistors have larger trans conductance 2. MOSFET have Infinite input impedance 3. These advantages are exploited together as BIMOS amplifier technology with high trans conductance, high input, output impedance and wider frequency band width.
6	<p>What is the use of source bypass capacitor in CS amplifier? (April 2017) BTL1</p> <p>The signal from the source is coupled to the gate through coupling capacitor C_c, which provide dc isolation between the amplifier and signal source.</p>
7	<p>Determine the output impedance of a JFET amplifier shown in fig. Let $g_m = 2\text{mA/V}$ and $\lambda = 0$. (April-2015) BTL3</p>  <p>$Z_0 = r_d // R_S // R_I // (1/g_m)$ $= R_S // R_I // (1/g_m)$</p>

	$= 457.4\Omega$																		
8	<p>Compare between JEFT and MOSFET amplifiers. (April-2015) BTL1</p> <table border="1"> <thead> <tr> <th></th> <th>JFETs</th> <th>MOSFETs</th> </tr> </thead> <tbody> <tr> <td>How it operates</td> <td>Voltage controlled</td> <td>Voltage controlled.</td> </tr> <tr> <td>Gain (Transconductance)</td> <td>Low transconductance (gain)</td> <td>Low transconductance (gain)</td> </tr> <tr> <td>Input Impedance</td> <td>JFETs are depletion type transistors only.</td> <td>MOSFETs can be depletion type or enhancement type.</td> </tr> <tr> <td>Input Impedance</td> <td>JFETs offer less input impedance than MOSFETs. JFETs typically offer about $10^9 \Omega$ of impedance.</td> <td>MOSFETs offers greater input impedance. MOSFETs typically offers about $10^{14} \Omega$ of impedance, sometimes greater.</td> </tr> <tr> <td>Cost</td> <td>JFETs are somewhat cheaper to manufacture than MOSFETs. They have a less sophisticated manufacturing process.</td> <td>MOSFETs is slightly more expensive to manufacture than JFETs.</td> </tr> </tbody> </table>		JFETs	MOSFETs	How it operates	Voltage controlled	Voltage controlled.	Gain (Transconductance)	Low transconductance (gain)	Low transconductance (gain)	Input Impedance	JFETs are depletion type transistors only.	MOSFETs can be depletion type or enhancement type.	Input Impedance	JFETs offer less input impedance than MOSFETs. JFETs typically offer about $10^9 \Omega$ of impedance.	MOSFETs offers greater input impedance. MOSFETs typically offers about $10^{14} \Omega$ of impedance, sometimes greater.	Cost	JFETs are somewhat cheaper to manufacture than MOSFETs. They have a less sophisticated manufacturing process.	MOSFETs is slightly more expensive to manufacture than JFETs.
		JFETs	MOSFETs																
	How it operates	Voltage controlled	Voltage controlled.																
	Gain (Transconductance)	Low transconductance (gain)	Low transconductance (gain)																
	Input Impedance	JFETs are depletion type transistors only.	MOSFETs can be depletion type or enhancement type.																
Input Impedance	JFETs offer less input impedance than MOSFETs. JFETs typically offer about $10^9 \Omega$ of impedance.	MOSFETs offers greater input impedance. MOSFETs typically offers about $10^{14} \Omega$ of impedance, sometimes greater.																	
Cost	JFETs are somewhat cheaper to manufacture than MOSFETs. They have a less sophisticated manufacturing process.	MOSFETs is slightly more expensive to manufacture than JFETs.																	
9	<p>Draw small signal model of JFET. (Nov-2014) BTL1</p>																		
10	<p>Give the general conditions under which CS amplifier would be used. (MAY 16) BTL1</p> <p>CS amplifier is used with the following conditions,</p> <ol style="list-style-type: none"> 1. Medium input, output impedance 2. Medium current and voltage gain 3. Output is 180° out of phase with input 																		
11	<p>What is body effect in MOSFET? How does it change the small signal equivalent circuit of MOSFET? (MAY 16) BTL1</p> <p>It refers to the change in transistor threshold voltage resulting from the voltage difference between transistor source and body(substrate). In small signal equivalent circuit this effect can be seen by adding a current source in parallel with r_o, and its value is $g_{mb} * V_{bs}$.</p>																		

<p>12</p>	<p>What are FET amplifiers? Where it is used? BTL1 FET is a voltage-controlled device which provides high voltage gain and high input impedance. It can be used as linear amplifier or a digital device in logic circuits it's also used in high frequency applications and interfacing applications.</p>																		
<p>13</p>	<p>Two amplifiers having gain 20 dB and 40 dB are cascaded. Find overall gain in dB. (NOV 2009) BTL1 $A_{v1} = 20 \text{ dB}$ $A_{v2} = 40 \text{ dB}$ $A_v = A_{v1} + A_{v2}$ So, $A_v = 60 \text{ dB}$</p>																		
<p>14</p>	<p>Compare BJT and JFET. BTL1</p> <table border="1" data-bbox="235 829 1209 1060"> <thead> <tr> <th>Parameter</th> <th>BJT</th> <th>JFET</th> </tr> </thead> <tbody> <tr> <td>Device</td> <td>Bipolar</td> <td>unipolar</td> </tr> <tr> <td>Characteristics</td> <td>Current Controlled</td> <td>Voltage Controlled</td> </tr> <tr> <td>A_v</td> <td>Very Large</td> <td>Limited</td> </tr> <tr> <td>A_i</td> <td>Very Large</td> <td>$A_i = \text{Infinite since } I_g = 0$</td> </tr> <tr> <td>Region of operation</td> <td>Active region</td> <td>Saturation region</td> </tr> </tbody> </table>	Parameter	BJT	JFET	Device	Bipolar	unipolar	Characteristics	Current Controlled	Voltage Controlled	A_v	Very Large	Limited	A_i	Very Large	$A_i = \text{Infinite since } I_g = 0$	Region of operation	Active region	Saturation region
Parameter	BJT	JFET																	
Device	Bipolar	unipolar																	
Characteristics	Current Controlled	Voltage Controlled																	
A_v	Very Large	Limited																	
A_i	Very Large	$A_i = \text{Infinite since } I_g = 0$																	
Region of operation	Active region	Saturation region																	
<p>15</p>	<p>State the general advantage of using JFET rather than BJT. BTL1</p> <ol style="list-style-type: none"> 1. FETs require less space than that for BJTs, hence they are preferred in integrated circuits. 2. FETs have higher input impedance than BJT they are preferred in amplifiers where high input impedance is required. 																		
<p>16</p>	<p>List out the applications of MOSFET. BTL1</p> <ol style="list-style-type: none"> 1. Heat sink and cooling within a computer most MOSFETs are located on the microprocessor chip, mounted on the motherboard and conspicuously cooled by its own heat sink and cooling fan. 2. Microprocessor chip itself is mounted in an electronic package with hundreds of interconnecting pins and connected to the chip by hundreds of tiny bond wires. 3. Chip cross-section A cross-section of the chip reveals multiple layers of tiny wires above the MOSFETs which are embedded in the silicon substrate. 																		
<p>17</p>	<p>Sketch the simple common gate amplifier circuit of JFET. BTL1 In Common Gate Amplifier Gate Terminal is grounded, Input is given in Source terminal and output is taken from Drain terminal.</p>																		

18	What is the impact of including a source resistor in the FET amplifier? (Nov 2016) BTL1 The impact of including a R_S in the FET amplifier is the voltage drop across the internal resistance would decrease.																					
19	Why multi-stage amplifiers are required? (Nov 2016) BTL1 In many applications, a single stage transistor amplifier cannot meet the desired specification of a given amplification factor. i.e. input resistance and output resistance. Hence to increase Input impedance and Gain more than one transistor amplifiers are connected and is called multistage amplifiers.																					
20	Compare the features of three MOSFET amplifier configurations. (Nov 2015) BTL1	<table border="1"> <thead> <tr> <th>Si.No</th> <th>Parameters</th> <th>Common Source (CS)</th> <th>Common Gate (CG)</th> <th>Common Drain (CD)</th> </tr> </thead> <tbody> <tr> <td>1</td> <td>Input resistance</td> <td>$R_i = R_1 \parallel R_2$</td> <td>$R_i = \frac{1}{g_m}$</td> <td>$R_i = R_1 \parallel R_2$</td> </tr> <tr> <td>2.</td> <td>Output resistance</td> <td>$R_o = r_o \parallel R_D$</td> <td>$R_o = R_D$</td> <td>$R_o = r_o \parallel R_S \parallel \frac{1}{g_m}$</td> </tr> <tr> <td>3.</td> <td>Voltage gain</td> <td>$A_V = -g_m(r_o \parallel R_D) \times \frac{R_i}{R_i + R_S}$</td> <td>$A_V = \frac{g_m}{1 + g_m R_S} \times (R_D \parallel R_L)$</td> <td>$A_V = \frac{g_m(r_o \parallel R_S)}{1 + g_m R_S(r_o \parallel R_D)} \times \frac{R_i}{R_i + R_S}$</td> </tr> </tbody> </table>	Si.No	Parameters	Common Source (CS)	Common Gate (CG)	Common Drain (CD)	1	Input resistance	$R_i = R_1 \parallel R_2$	$R_i = \frac{1}{g_m}$	$R_i = R_1 \parallel R_2$	2.	Output resistance	$R_o = r_o \parallel R_D$	$R_o = R_D$	$R_o = r_o \parallel R_S \parallel \frac{1}{g_m}$	3.	Voltage gain	$A_V = -g_m(r_o \parallel R_D) \times \frac{R_i}{R_i + R_S}$	$A_V = \frac{g_m}{1 + g_m R_S} \times (R_D \parallel R_L)$	$A_V = \frac{g_m(r_o \parallel R_S)}{1 + g_m R_S(r_o \parallel R_D)} \times \frac{R_i}{R_i + R_S}$
Si.No	Parameters	Common Source (CS)	Common Gate (CG)	Common Drain (CD)																		
1	Input resistance	$R_i = R_1 \parallel R_2$	$R_i = \frac{1}{g_m}$	$R_i = R_1 \parallel R_2$																		
2.	Output resistance	$R_o = r_o \parallel R_D$	$R_o = R_D$	$R_o = r_o \parallel R_S \parallel \frac{1}{g_m}$																		
3.	Voltage gain	$A_V = -g_m(r_o \parallel R_D) \times \frac{R_i}{R_i + R_S}$	$A_V = \frac{g_m}{1 + g_m R_S} \times (R_D \parallel R_L)$	$A_V = \frac{g_m(r_o \parallel R_S)}{1 + g_m R_S(r_o \parallel R_D)} \times \frac{R_i}{R_i + R_S}$																		
21	How does a transistor width-to-length ratio affect the small signal voltage gain of a common source amplifier? (Nov 2015) BTL1 $V_o/V_{gs} = -g_m \cdot R_L$, where $g_m = \sqrt{2K_n'} \sqrt{W/L} \sqrt{I_d}$ The square root of width to length ratio is directly proportional to voltage gain, width to length ratio changes voltages gain changes and also g_m depends on internal capacitance, due to changes in g_m , C_{gs} , the voltage gain gets affected.																					
22	Sketch the simple common source amplifier circuit of MOSFET. BTL3																					



23 **Draw the simple common source voltage divider bias amplifier circuit of MOSFET. BTL1**

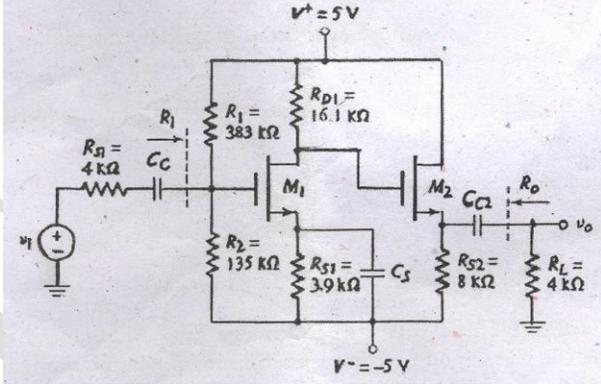
24 **Sketch the hybrid pi equivalent of simple common source voltage divider bias amplifier circuit of MOSFET. BTL1**

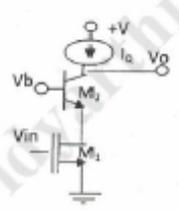
25 **Give the hybrid pi equivalent of source follower amplifier circuit of MOSFET. BTL1**

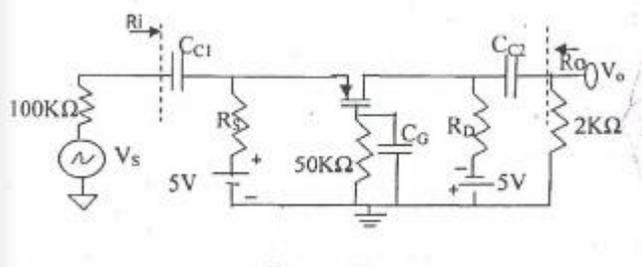
PART*B

1. **Describe the small signal equivalent circuit of the MOSFET and determine the values of small signal parameters. (13M) (April-2018)**
Derive gain, input and output impedance of common source JFET amplifier with neat

	<p>diagram and equivalent circuit. (13M) (April-2017) (Nov 2016) BTL1 Answer: Page 219- Donald & Godse :4.4 Circuit diagram: Common source JFET - Depletion MOSFET (2M) AC equivalent circuit: Short circuiting - input – output - bypass -coupling capacitors -Set DC voltage - zero. (2M) Small signal equivalent circuit: Replace transistor – Small signal hybrid pi equivalent model. (2M) Derivation of small signal parameters (1M) Voltage Gain: $A_v = -g_m(r_o // R_d) (R_i / (R_i + R_{s_i}))$ (2M) Input Impedance: $R_i = R_1 // R_2$ (2M) Output Impedance: $R_o = R_d // r_o$ (2M) Current Gain: $A_i = \text{Infinite}$ (2M)</p>
2	<p>Enumerate on the voltage swing limitations, general conditions under which a source follower amplifier would be used. (13M) (April 2018) BTL1 Answer: Page 219 – Donald & Godse :4.13 Circuit diagram: Source Follower Circuit. (2M) AC equivalent circuit: Short circuiting - input – output - bypass -coupling capacitors -Set DC voltage - zero. (2M) Small signal equivalent circuit: Replace transistor – Small signal hybrid pi equivalent model. (2M) Derivation of small signal parameters (1M) Voltage Gain: $A_v = -g_m(r_o // R_d) (R_i / (R_i + R_{s_i}))$ (2M) Input Impedance: $R_i = R_1 // R_2$ (2M) Output Impedance: $R_o = R_d // r_o$ (2M) Current Gain: $A_i = \text{Infinite}$ (2M)</p>
3	<p>Draw a common Gate MOSFET amplifier and derive for A_v, A_i and R_i using small signal equivalent circuit. (13M) (April-2017) BTL3 Answer: Page 239 - Donald & Godse :4.17 Circuit diagram: Common Gate MOSFET (2M) AC equivalent circuit: Short circuiting - input – output - bypass -coupling capacitors -Set DC voltage - zero. (2M) Small signal equivalent circuit: Replace transistor – Small signal hybrid pi equivalent model. (2M) Derivation of small signal parameters (1M) Voltage Gain: $A_v = g_m * (R_l // R_d) / (1 + g_m * R_{s_i})$ (2M) Input Impedance: $R_i = 1 / g_m$ (2M) Output Impedance: $R_o = R_d$ (2M) Current Gain: $A_i = \{ g_m * R_{s_i} / (1 + g_m * R_{s_i}) \} \{ R_d / (R_d + R_l) \}$ (2M)</p>
4	<p>With a neat diagram explain the small signal analysis of common source Amplifier with a source resistance for MOSFET. (13M) (Nov 2017) BTL1 Answer: Page 225 - Donald & Godse :4.25 Circuit diagram: Common source MOSFET Amplifier (2M) AC equivalent circuit: Short circuiting - input – output - bypass -coupling capacitors -Set DC voltage - zero. (2M) Small signal equivalent circuit: Replace transistor – Small signal hybrid pi equivalent model. (2M)</p>

	<p>Derivation of small signal parameters (1M)</p> <p>Voltage Gain: $A_v = -g_m(r_o // R_d) (R_i / (R_i + R_{si}))$ (2M)</p> <p>Input Impedance: $R_i = R_1 // R_2$ (2M)</p> <p>Output Impedance: $R_o = R_d // r_o$ (2M)</p> <p>Current Gain: $A_i = \text{Infinite}$ (2M)</p>
5	<p>With a neat diagram explain the source follower amplifier using MOSFET and derive the necessary equations to calculate the voltage gain, input and output resistance. (13M) (Nov 2017) BTL1</p> <p>Answer: Page 231 - Donald & Godse :4.32</p> <p>Circuit diagram: Source follower amplifier using MOSFET (2M)</p> <p>AC equivalent circuit: Short circuiting - input - output - bypass - coupling capacitors - Set DC voltage - zero. (2M)</p> <p>Small signal equivalent circuit: Replace transistor - Small signal hybrid pi equivalent model. (2M)</p> <p>Derivation of small signal parameters (1M)</p> <p>Voltage Gain: $A_v = \{R_s // r_o / (1/g_m + R_s // r_o)\} \{R_i / (R_i + R_{si})\}$ (2M)</p> <p>Input Impedance: $R_i = R_1 // R_2$ (2M)</p> <p>Output Impedance: $R_o = R_d // r_o$ (2M)</p> <p>Current Gain: $A_i = \text{Infinite}$ (2M)</p>
6	<p>Determine the small signal voltage gain of the multistage Cascode circuit shown below. The transistor parameters are $K_{n1} = 0.5 \text{ mA/V}^2$, $K_{n2} = 0.2 \text{ mA/V}^2$, $V_{tn1} = V_{tn2} = 1.2 \text{ V}$, $\lambda_1 = \lambda_2 = 0$. The quiescent drain currents are $I_{D1} = 0.2 \text{ mA}$, $I_{D2} = 0.5 \text{ mA}$. (13M) (Nov 2016) BTL3</p>  <p>Answer: Page 260 - Donald.</p> <p>Circuit diagram (2M)</p> <p>AC equivalent circuit: Short circuiting - input - output - bypass - coupling capacitors - Set DC voltage - zero. (2M)</p> <p>Small signal equivalent circuit: Replace transistor - Small signal hybrid pi equivalent model. (2M)</p> <p>Derivation of small signal parameters (1M)</p> <p>Output Voltage: $V_o = g_{m2} * V_{gs2} (R_{s2} // R_L)$ (2M)</p> <p>Input Voltage: $V_i = \{-[1 + g_{m2}(R_{s2} // R_L)] / g_{m1} * R_{d1}\} \{R_i / (R_i + R_{si})\}$ (2M)</p> <p>Voltage Gain: $A_v = V_o / V_i = -6.14$ (2M)</p>
7	<p>Determine voltage gain of the circuit assuming the following parameters, $V_{dd} = 0.3 \text{ V}$, $R_d = 10 \text{ K}$, $R_{g1} = 140 \text{ k}$, $R_{g2} = 60 \text{ K}$, and $R_{si} = 4 \text{ k}$, the transistor parameters are $V_{tn} = 0.4 \text{ V}$, $K_n = 0.5 \text{ mA/V}^2$ and $\lambda = 0.02 \text{ V}^{-1}$. (13M) (Nov 2016) BTL3</p> <p>Answer: Page 233 - Donald.</p>

	<p>Calculation: Find V_{gsq} - I_{dq} - DC analysis (2M)</p> <p>Transconductance: $g_m = 2K_n (V_{gsq} - V_{tn}) = ?$ (3M)</p> <p>Output Impedance: $R_o = [\lambda I_{dq}]^{-1}$ (2M)</p> <p>Input Impedance: $R_i = R_1 // R_2$ (2M)</p> <p>Voltage Gain: $A_v = \{g_m (R_s // r_o) / (1 + g_m (R_s // r_o))\} \{R_i / (R_i + R_{si})\}$ (4M)</p>
8	<p>Derive the voltage gain of BiMOS cascade amplifiers shown in fig. (10M) (April-2015) BTL3</p>  <p>Answer: Page 400 – Donald & Godse :4.46</p> <p>Circuit diagram: BiMOS (2M)</p> <p>AC equivalent circuit: Short circuiting - input – output - bypass -coupling capacitors -Set DC voltage - zero. (2M)</p> <p>Small signal equivalent circuit: Replace transistor – Small signal hybrid pi equivalent model. (2M)</p> <p>Derivation of small signal parameters (1M)</p> <p>Voltage Gain: Stage 1-A_{v1}- Stage 2- A_{v2} (3M)</p> <p>Total Voltage Gain: $A_v = A_{v1} * A_{v2}$. (2M)</p>
9	<p>Draw a discrete common gate JFET amplifier and derive voltage gain A_v, Input impedance, R_{in} and output impedance R_{out} with small signal equivalent circuit. (13M) (April-2015) BTL1</p> <p>Answer: Page 239 – Donald & Godse :4.17</p> <p>Circuit diagram: Common gate JFET (2M)</p> <p>AC equivalent circuit: Short circuiting - input – output - bypass -coupling capacitors -Set DC voltage - zero. (2M)</p> <p>Small signal equivalent circuit: Replace transistor – Small signal hybrid pi equivalent model. (2M)</p> <p>Derivation of small signal parameters (1M)</p> <p>Voltage Gain: $A_v = g_m * (R_l // R_d) / (1 + g_m R_{si})$ (2M)</p> <p>Input Impedance: $R_i = 1/g_m$ (2M)</p> <p>Output Impedance: $R_o = R_d$ (2M)</p> <p>Current Gain: $A_i = \{g_m * R_{si} / (1 + g_m R_{si})\} \{R_d / (R_d + R_l)\}$ (2M)</p>
10	<p>Determine the current gain of JFET source follower amplifier. (13M) (April-2015) BTL1</p> <p>Answer: Page 219 - Donald & Godse :4.13</p> <p>Circuit diagram (2M)</p> <p>AC equivalent circuit: Short circuiting - input – output - bypass -coupling capacitors -Set DC voltage - zero. (2M)</p>

	<p>Small signal equivalent circuit: Replace transistor – Small signal hybrid pi equivalent model. (2M)</p> <p>Derivation of small signal parameters (1M)</p> <p>Voltage Gain: $A_v = -g_m(r_o // R_d) (R_i / (R_i + R_{si}))$ (2M)</p> <p>Input Impedance: $R_i = R_1 // R_2$ (1M)</p> <p>Output Impedance: $R_o = R_d // r_o$ (1M)</p> <p>Current Gain: $A_i = \text{Infinite}$ (2M)</p>
11	<p>Consider the PMOS amplifier shown in fig. The transistor parameters are $V_{tp} = -1V$, $\beta_p = (\mu_p C_{ox}(W/L)) = 1 \text{ mA/V}^2$ and $\lambda = 0$. Determine R_D and R_S, such that $I_{DQ} = 0.75 \text{ mA}$ and $V_{SDQ} = 6V$. determine input impedance R_i and output impedance R_o voltage gain, current gain and maximum output voltage swing. (13M) (April-2015) BTL3</p>  <p>Answer: Page 242 - Donald.</p> <p>Circuit diagram (2M)</p> <p>AC equivalent circuit: Short circuiting - input - output - bypass -coupling capacitors -Set DC voltage - zero. (2M)</p> <p>Small signal equivalent circuit: Replace transistor – Small signal hybrid pi equivalent model. (2M)</p> <p>Derivation of small signal parameters (1M)</p> <p>Voltage Gain: $A_v = g_m * (R_i // R_d) / (1 + g_m R_{si})$ (2M)</p> <p>Input Impedance: $R_i = 1 / g_m$ (2M)</p> <p>Output Impedance: $R_o = R_d$ (1M)</p> <p>Current Gain: $A_i = \{ g_m * R_{si} / (1 + g_m R_{si}) \} \{ R_d / (R_d + R_l) \}$ (2M)</p>
12	<p>Derive gain input and output impedance of multistage FET amplifier with neat circuit diagram and equivalent circuit. (13M) (Nov-2014) BTL1</p> <p>Answer: Page: Godse :4.38</p> <p>Types: Cascade- Cascode (2M)</p> <p>Circuit diagram (2M)</p>

	<p>AC equivalent circuit: Short circuiting - input – output - bypass -coupling capacitors -Set DC voltage - zero. (2M)</p> <p>Small signal equivalent circuit: Replace transistor – Small signal hybrid pi equivalent model. (2M)</p> <p>Derivation of small signal parameters (1M)</p> <p>Voltage Gain: $A_v = -g_{m1} * g_{m2} \{ R_{D1}(R_{s2}/R_L)/(1+g_{m2}(R_{s2}/R_L)) \} (R_i/R_i+R_{s1})$ (Cascade) (2M)</p> <p>Voltage Gain: $A_v = -g_m R_D$ (Cascode) (2M)</p>
--	---

PART * C

1	<p>Design a JFET source follower circuit (for the Figure shown below) with a specified small signal voltage gain given $I_{DSS}=12mA$, $V_p=-4V$, $\lambda=0.01 V^{-1}$. Determine R_s and I_{DQ} Such that the small signal voltage gain is a least $A_V = V_o / V_i = 0.90$. (15M) (May 2016) BTL3</p> <div style="text-align: center;"> </div> <p>Answer: Page 232 - Donald.</p> <p>Calculation: Apply KVL – Input – Output loop- find $I_{dq}=3mA$ (4M)</p> <p>Source Resistance: $R_s=4K$ (4M)</p> <p>Drain current (Id) or Drain saturation current. $I_D = I_{DSS}(1-V_{gs}/V_p)^2$ (3M)</p> <p>Explanation: Procedure - finding - resistances (4M)</p>
---	---

2	<p>Determine the small signal voltage gain of a common source circuit containing a source resistor. The transistor parameters are $V_{tn}=0.8V$, $K_n =1 mA/V^2$ and $\lambda =0$. (15M) (May 2016). BTL3</p> <div style="text-align: center;"> </div> <p>Answer: Page 225- Donald.</p> <p>Circuit diagram (2M)</p>
---	---

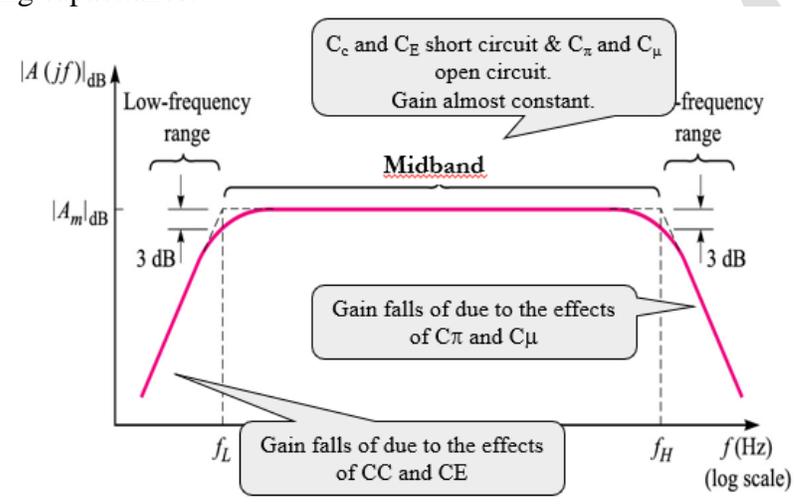
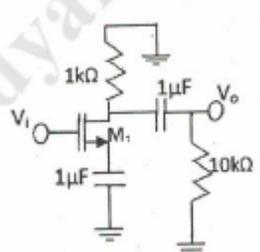
	<p>AC equivalent circuit: Short circuiting - input – output - bypass -coupling capacitors -Set DC voltage - zero. (2M)</p> <p>Small signal equivalent circuit: Replace transistor – Small signal hybrid pi equivalent model. (2M)</p> <p>Derivation of small signal parameters (2M)</p> <p>Voltage Gain: $A_v = -g_m(r_o//R_d) (R_i/R_i+R_{s_i})$ (7M)</p>
3	<p>Derive CMRR of basic FET differential amplifier with neat circuit diagram and equivalent circuit. (15M) (Nov-2014) BTL1</p> <p>Answer: Page: Godse :4.40</p> <p>Circuit diagram (2M)</p> <p>AC equivalent circuit: Short circuiting - input – output - bypass -coupling capacitors -Set DC voltage - zero. (2M)</p> <p>Small signal equivalent circuit: Replace transistor – Small signal hybrid pi equivalent model. (2M)</p> <p>Derivation of small signal parameters (1M)</p> <p>Common mode gain $= -g_m R_d / (1 + 2 g_m R_o)$ (2M)</p> <p>Differential mode gain: $= g_m R_d / 2$ (2M)</p> <p>CMRR: $= A_d / A_c$ (2M)</p> <p>CMRR: $= A_d / A_c = 1/2 (1 + 2(2K_n I_q)^{1/2} R_o)$ (2M)</p>

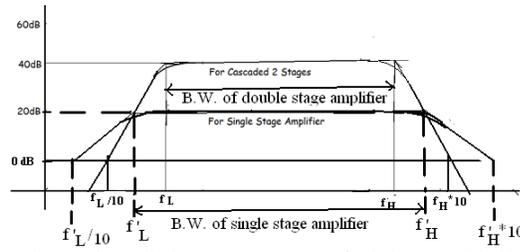
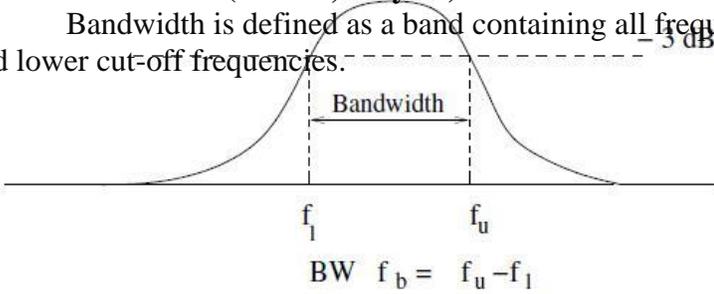
UNIT IV– FREQUENCY RESPONSE OF AMPLIFIERS

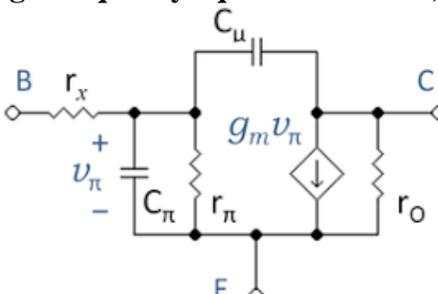
Amplifier frequency response – Frequency response of transistor amplifiers with circuit capacitors – BJT frequency response – short circuit current gain - cut off frequency – f_{α} , f_{β} and unity gain bandwidth – Miller effect - frequency response of FET - High frequency analysis of CE and MOSFET CS amplifier - Transistor Switching Times.

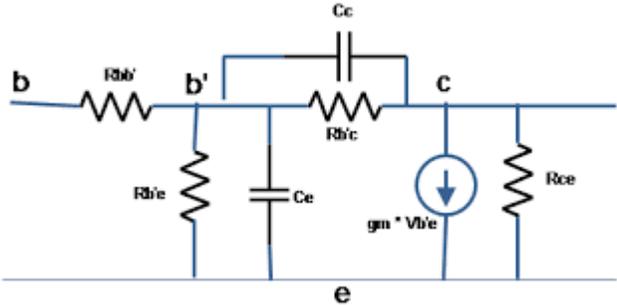
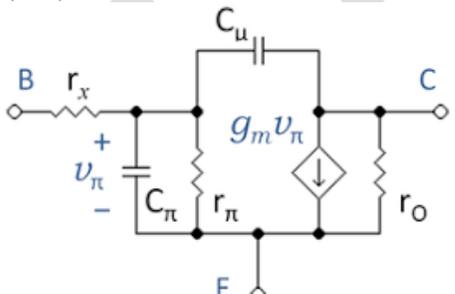
PART * A

Q.No.	Questions
1	<p>What is 3_{dB} frequency? (April 2018) BTL1</p> <p>It is defined as the frequency at which the current gain of the amplifier drops to 0.707 times or 3dB below the maximum gain. It is also called as Upper and Lower cut off frequencies, Corner frequencies.</p>
2	<p>What is beta frequency? (April 2018) BTL1</p> <p>It is defined as the frequency at which the current gain β of the of the common emitter BJT drops to 0.707 times or 3dB below the maximum gain, and is denotes by f_{β}, it can be defined by, $f_{\beta} = 1/(2\pi r_{\pi}(C_{\pi} + C_{\mu}))$</p>
3	<p>How does MOSFET works as an amplifier? (April 2018) BTL2</p> <p>Metal Oxide Semiconductor Field Effect Transistor, or MOSFET for short, is an excellent choice for small signal linear amplifiers as their input impedance is extremely high making them easy to bias. But for a MOSFET to produce linear amplification, it has to operate in its saturation region, unlike the Bipolar Junction Transistor. But just like the BJT, it too needs to be biased around a centrally fixed Q-point.</p>
4	<p>Define rise time. Give the relationship between bandwidth and rise time. (April 2017) (Nov 2015) BTL1</p> <p>Rise time is the time required for the signal to change from 10% to 90% of its value. Relation between Bandwidth and Rise time is Bandwidth = $0.35/t_r$; Where t_r = rise time.</p>
5	<p>Sketch hybrid π equivalent model of BJT. (April 2017) (Nov - 2015) Sketch the expanded hybrid π model of the BJT. (May-2016) BTL1</p>
6	<p>What is Miller effect? (Nov-2017) BTL1</p> <p>The feedback capacitor connected between input and output of the transistor [(CE-BJT) and (CS-FET)] is called junction capacitance, which causes a multiplication effect, when miller theorem is applied for high frequency analysis. $C_M = C_f (1 + g_m R)$ C_M – miller capacitance, C_f- junction capacitance This multiplicative effect by $(1 + g_m R)$ reduces the high frequency gain of amplifier and is called miller effect.</p>

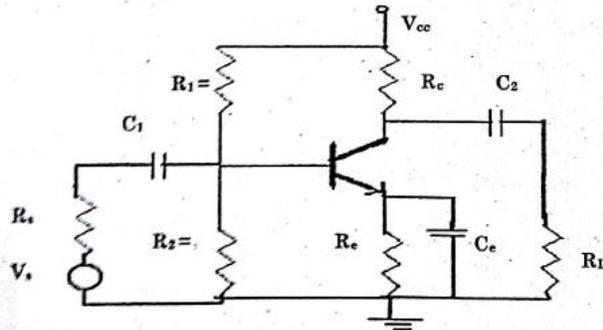
7	<p>What is unity gain amplifier? (Nov-2017) BTL1 The amplifier in which the gain is unity is called unity gain amplifier.</p>
8	<p>A bipolar transistor has parameter $\beta_0 = 150$, $C_\pi = 2\text{pF}$, $C_\mu = 0.3\text{pF}$ and is biased at $I_{CQ} = 0.5\text{mA}$. Determine the beta cut off frequency. (May-2016) BTL3 $f_\beta = 1/(2\pi r_\pi(C_\pi + C_\mu))$ where $r_\pi = \beta * V_T / I_{CQ}$</p>
9	<p>What is the reason for reduction in gain at lower and higher frequencies in case of amplifiers? (Nov-2016) BTL3 The lower the frequency, the lesser will be the gain. This reduction in gain is due to the presence of coupling (Input & output) and bypass capacitors. The higher the frequency, the lesser will be the gain. This is due to the internal capacitances like, junction and wiring capacitance.</p> 
10	<p>Determine the unity gain bandwidth of a FET with parameter, $C_{gd} = 10\text{fF}$, $C_{gs} = 50\text{fF}$ and $g_m = 1.2\text{mA/V}$. (Nov-2016) BTL 3 $f_T = g_m / 2\pi(C_{gs} + C_{gd})$</p>
11	<p>Find the unity gain bandwidth of MOSFET where $g_m = 6\text{mA/V}$, $C_{gx} = 8\text{pF}$, $C_{gd} = 4\text{pF}$ and $C_{ds} = 1\text{pF}$. (April-2015) BTL 3 $f_T = g_m / 2\pi(C_{gs} + C_{gd})$</p>
12	<p>The AC schematic of an NMOS common – source stage is shown in the figure where part of the biasing circuits has been omitted for simplicity. For the N- channel MOSFET, the transconductance, $g_m = 1\text{mA/V}$, and body effect and channel length modulation effect are to be neglected. Find the lower cutoff frequency. (April-2015) BTL 3</p>  <p>Draw small signal equivalent circuit Lower Cut off frequency: $f_L = g_m / 2\pi(C_{gs} + C_{gd})$</p>

<p>13</p>	<p>Relate gain and bandwidth of single and multistage amplifier. (NOV/DEC2014) BTL1 Gain: Improved in multistage amplifier than single stage. Bandwidth: Decreases in Multistage amplifier when compared to Single stage.</p>  <p>Fig. 6 . Gain Magnitude-Frequency Response of a single stage and double stage amplifier</p>
<p>14</p>	<p>What is the effect of miller’s capacitance on the frequency response of an amplifier. (NOV/DEC2014) BTL1 The Miller effect accounts for an increase in the equivalent input capacitance of an inverting voltage amplifier due to amplification of capacitance between the input and output terminals. Although Miller effect normally refers to capacitance, any impedance connected between the input and another node exhibiting high gain can modify the amplifier input impedance via the Miller effect. This increase in input capacitance is given by $C_M=C(1-A_v)$. where A_v is the gain of the amplifier and C is the feedback capacitance. The Miller effect is a special case of Miller's theorem.</p>
<p>15</p>	<p>Define Bandwidth. (Nov 13, May 13) BTL1 Bandwidth is defined as a band containing all frequencies between upper cut-off and lower cut-off frequencies.</p>  <p>$BW f_b = f_u - f_l$</p> <p>Upper and lower cut-off (or 3dB) frequencies corresponds to the frequencies where the magnitude of signal's Fourier Transform is reduced to half (3dB less than) its maximum value.</p>
<p>16</p>	<p>Define the frequency response of an amplifier. (Dec-2006) BTL1 The frequency response of an amplifier can be defined as the variation of output quantity (Output Voltage) with respect to input signal frequency. In other words, it can be defined as a graph drawn between the input frequency and the gain of an amplifier.</p>
<p>17</p>	<p>Define lower and upper cut-off frequencies of an amplifier. (Dec-2005) BTL1 Lower cut – off frequency: - The frequency (on lower side) at which the voltage gain of the amplifier is exactly 70.7% of the maximum gain is known as lower cut – off frequency. Upper cut – off frequency: - The frequency (on higher side) at which the voltage gain of the amplifier is exactly 70.7% of the maximum gain is known as upper cut – off frequency.</p>

18	<p>What are the high frequency effects in an amplifier? (May-2004) BTL1</p> <p>At high frequencies the gain was reduced by the following factors</p> <ol style="list-style-type: none"> 1. Internal or junction or Stray Capacitance 2. Wiring capacitance
19	<p>What is the significance of gain bandwidth product? (May-2008) BTL1</p> <p>It is very helpful in the preliminary design of a multistage wide band amplifier. This can be used to setup a tentative circuit which is often used for this purpose.</p>
20	<p>Sketch the hybrid π model (high frequency equivalent circuit) of FET. (DEC 2012) BTL1</p> 
21	<p>Define Gain band width product. (NOV 2012) BTL1</p> <p>It is defined as product of amplifier band width and gain at which BW is measured it is denoted as GBW, GBP, GBWP. It is also known as transition frequency or unity gain bandwidth.</p>
22	<p>Discuss the effect of bypass capacitor on BW of amplifier. (MAY 15) BTL1</p> <p>At medium and high frequencies, it offers a very low reactance hence it can be short circuited so it has no effect.</p> <p>At low frequencies it offers finite reactance thus it has the effect at low frequency.</p>
23	<p>Define unity gain BW of BJT. BTL1</p> <p>It is the frequency at which the gain of the amplifier is dropped to unity and is denoted by f_T.</p> $f_T = \beta_0 / (2\pi * r_{\pi} (C_{\pi} + C_{\mu}))$
24	<p>Define unity gain BW of FET. BTL1</p> <p>It is the frequency at which the gain of the amplifier is dropped to unity and is denoted by f_T.</p> $f_T = g_m / (2\pi (C_{gs} + C_{gd}))$
25	<p>What are the components affect the frequency response of RC coupled amplifier? BTL1</p> <p>Low frequency response is affected by</p> <ol style="list-style-type: none"> 1. Input, Output coupling capacitors 2. Bypass capacitors <p>High frequency response is affected by</p> <ol style="list-style-type: none"> 1. Junction or internal capacitance 2. Stray and wiring capacitance
PART*B	
1	<p>With a neat sketch, explain hybrid π CE transistor model also derive the expression for various components in terms of 'hybrid pi' parameters. (13M) (April- 2018) (Nov - 2015) BTL1</p> <p>Answer: Page: 506 – Donald & 5.11- Bakshi</p> <p>Circuit diagram: Common Emitter BJT Amplifier (2M)</p> <p>AC equivalent circuit: Short circuiting - input – output - bypass -coupling capacitors -Set DC voltage - zero. (2M)</p> <p>Small signal equivalent circuit: Replace transistor – Small signal hybrid pi equivalent model.</p>

	<p>Derivation of small signal parameters (1M)</p> <p>Short circuit current gain: $hfe = \frac{gm r\pi}{1+j\omega r\pi(C\pi+C\mu)}$ (2M)</p> <p>Cut off frequency: $f\beta = \frac{1}{2\pi*r\pi(C\pi+C\mu)}$ (2M)</p> <p>Unity gain bandwidth: $fT = \frac{\beta o}{2\pi*r\pi(C\pi+C\mu)}$ (2M)</p> <p>Miller effect (2M)</p> 
<p>2</p>	<p>Explain high frequency analysis of JFET with necessary circuit diagram and derive its gain bandwidth product. (13M) (April- 2018) (Nov - 2015) BTL1</p> <p>Answer: Page: 518 – Donald & 5.26- Bakshi</p> <p>Circuit diagram: Common source FET Amplifier. (2M)</p> <p>AC equivalent circuit: Short circuiting - input – output - bypass -coupling capacitors -Set DC voltage - zero. (2M)</p> <p>Small signal equivalent circuit: Replace transistor – Small signal hybrid pi equivalent model.</p> <p>Derivation of small signal parameters (1M)</p> <p>Short circuit current gain: $Ai = \frac{gm}{j\omega(Cgs+Cgd)}$ (3M)</p> <p>Unity gain bandwidth: $fT = \frac{gm}{2\pi(Cgs+Cgd)}$ (3M)</p> <p>Miller effect (2M)</p> 
<p>3</p>	<p>Determine low frequency response of the amplifier circuit shown in Fig. (10M) (April-2017) BTL1</p>

$R_s = 600 \Omega$; $R_1 = 68 K \Omega$; $R_2 = 22 K \Omega$; $R_e = 1K$ $V_{cc} = 10 V$
 $C_1 = C_2 = 0.1 \mu F$; $C_E = 10 \mu F$.
 $R_s = 2.2 K \Omega$; $R_L = 10 K \Omega$; $\beta = 100$, $h_{ie} = r_{\pi} = 1.1 k$



Answer: Page: 506 - Donald.

Circuit diagram: Common Emitter BJT Amplifier.

(2M)

AC equivalent circuit: Short circuiting - input - output - bypass -coupling capacitors -Set DC voltage - zero. (2M)

Small signal equivalent circuit: Replace transistor - Small signal hybrid pi equivalent model.

Derivation of small signal parameters

(2M)

Cut off frequency due to C1 $= 1/(2\pi R_{in} C_1)$ (2M)

Cut off frequency due to C2 $= 1/(2\pi (R_c + R_L))$ (2M)

4

Define f_a and f_{β} and f_T . Also derive for f_a and f_{β} and f_T with two source terminal and one sink terminal and derive for source and sink terminal as a function of reference current. (13M) (Nov-2017) BTL 3

Answer: Page: 506 - Donald.

Circuit diagram: Common Emitter BJT Amplifier.

(1M)

AC equivalent circuit: Short circuiting - input - output - bypass -coupling capacitors -Set DC voltage - zero. (2M)

Small signal equivalent circuit: Replace transistor - Small signal hybrid pi equivalent model.

Derivation of small signal parameters

(1M)

Short circuit current gain: $h_{fe} = \frac{g_m r_{\pi}}{1 + j\omega r_{\pi} (C_{\pi} + C_{\mu})}$

(2M)

Cut off frequency: $f_{\beta} = \frac{1}{2\pi * r_{\pi} (C_{\pi} + C_{\mu})}$

(1M)

Circuit diagram: Common Base BJT Amplifier.

(1M)

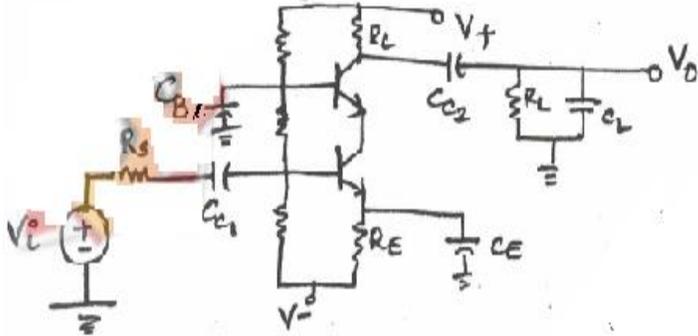
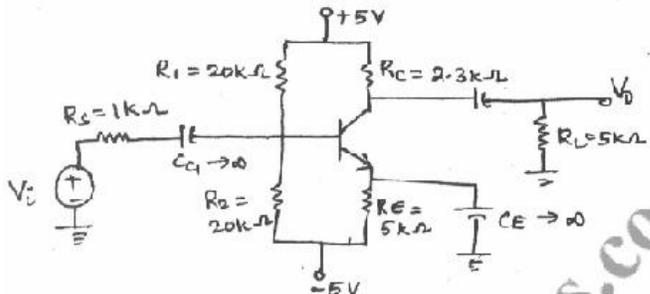
AC equivalent circuit: Short circuiting - input - output - bypass -coupling capacitors -Set DC voltage - zero.

(2M)

Small signal equivalent circuit: Replace transistor - Small signal hybrid pi equivalent model.

Derivation of small signal parameters

(2M)

	<p>Cut off frequency: $f\alpha = \frac{1+\square}{2\pi*r\pi(C\pi+C\mu)}$ (1M)</p>
<p>5</p>	<p>Determine the 3 dB frequencies and mid band gain of a cascade circuit. For the Figure, the parameters are $V_+ = 10, V_- = -10V, R_s = 0.1 K\Omega, R_1 = 42.5 K\Omega, R_2 = 28.3 K\Omega, R_E = 5.4 K\Omega, R_c = 5 K\Omega, R_L = 10K\Omega, C_L = 0$. The transistor parameters are $\beta = 150, V_{be} (on) = 0.7 V, V_A = \infty, C\pi = 35pF$ and $C\mu = 4pF$. (13M) (May-2016) BTL3</p>  <p>Answer: Page: 515 - Donald.</p> <p>Circuit diagram: Cascade BJT Amplifier. (2M) AC equivalent circuit: Short circuiting - input - output - bypass -coupling capacitors -Set DC voltage - zero. (2M) Small signal equivalent circuit: Replace transistor – Small signal hybrid pi equivalent model. Derivation of small signal parameters (3M) Short circuit current gain: $hfe = \frac{gm r\pi}{1+j\omega r\pi(C\pi+C\mu)}$ (2M) Cut off frequency: $f\beta = \frac{1}{2\pi*r\pi(C\pi+C\mu)}$ (2M) Unity gain bandwidth: $fT = \frac{\beta o}{2\pi*r\pi(C\pi+C\mu)}$ (2M)</p>
<p>6</p>	<p>The transistor in figure has parameters $\beta = 125, V_{be} (on) = 0.7V, V_A = 200V, C\pi = 24 pF$ and $C\mu = 3 pF$.</p> <ol style="list-style-type: none"> 1. Calculate the miller capacitance 2. Determine the upper 3 dB frequency. 3. Determine the small signal mid band voltage gain (13M) (May-2016) BTL3  <p>Answer: Page :516 - Donald.</p>

Circuit diagram: Common Emitter BJT Amplifier.

(1M)

AC equivalent circuit: Short circuiting - input - output - bypass -coupling capacitors -Set DC voltage - zero. (1M)

Small signal equivalent circuit: Replace transistor – Small signal hybrid pi equivalent model.

Derivation of small signal parameters

(1M)

Short circuit current gain: $hfe = \frac{gm r\pi}{1+j\omega r\pi(C\pi+C\mu)}$

(2M)

Cut off frequency: $f\beta = \frac{1}{2\pi*r\pi(C\pi+C\mu)}$

(2M)

Unity gain bandwidth: $fT = \frac{\beta o}{2\pi*r\pi(C\pi+C\mu)}$

(2M)

Miller effect (1M)

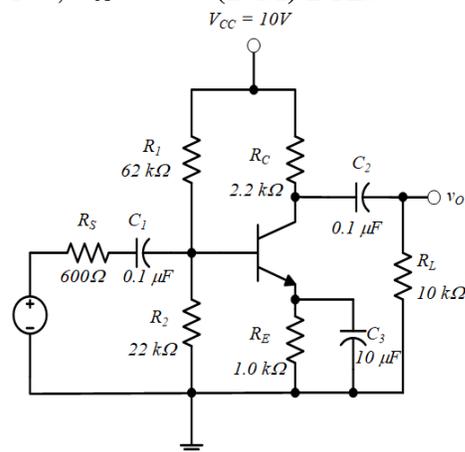
Miller Capacitance $C_m=C\mu(1+|Av|)$

(2M)

Voltage gain $Av=-gm (Rc//RL)$ (2M)

7

Determine the total low-frequency response of the amplifier shown in figure. Assume $\beta = 100$, $V_A = 70$ V (13M) BTL3



Answer: Page: 516 - Donald.

Therefore,

$r\pi = 1.59$ kΩ, $r_o = 42.74$ kΩ, $g_m = 63$ mA/V

(2M)

Low frequency due to C_1 :

(3M)

$R_{1s} = R_s + (R_b || r\pi) = 600 + (16.24k || 1.59k) = 2.05k\Omega$

$R_{Th} = R_1 || R_2 = 16.24k\Omega$

$f_{C_1(input)} = \frac{1}{2\pi R_{1s} C_1} = \frac{1}{2\pi(2.05k\Omega)(0.1\mu F)} = 776.37 Hz \cong 776.4 Hz$

Low frequency due to C_2 :

(3M)

$R_{2s} = R_L + (R_c || r_o) = 10k + (2.2k || 43.74k) = 12.092k\Omega$

$f_{C_2(output)} = \frac{1}{2\pi R_{2s} C_2} = \frac{1}{2\pi(12.092k\Omega)(0.1\mu F)} = 131.62 Hz \cong 132 Hz$

Low frequency due to C_3 :

(3M)

$$R_{3S} = R_E \parallel \frac{r_\pi + R_{th}}{\beta + 1} = 1k \parallel \frac{1.59k + 579}{101} = 21.02\Omega$$

$$R_{th} = R_S \parallel R_{TH} = 0.579k\Omega$$

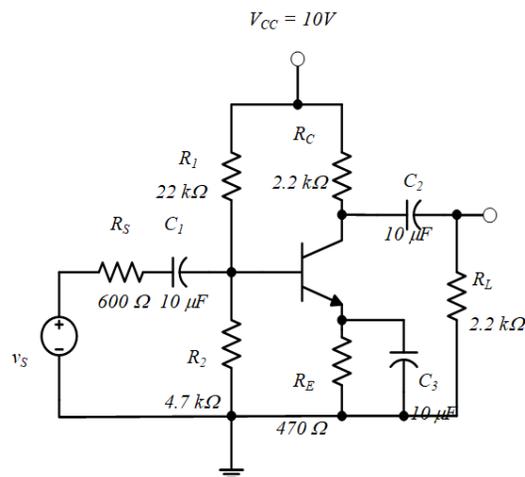
$$f_{Cl(bypass)} = \frac{1}{2\pi R_{3S} C_3} = \frac{1}{2\pi(21.02\Omega)(10\mu F)} = 757Hz$$

Dominant lower cutoff frequency is: $f_{cl(input)} = 776.4Hz$ & Dominant network (2M)

Determine:

i-Upper cutoff frequencies

ii- Dominant upper cutoff frequency for the given BJT amplifier. Assume $\beta = 125$, $V_A = 70$ V, $C_{be} = 20$ pF, $C_{bc} = 2.4$ pF. (13M) BTL3



8

Answer: Page: 516 - Donald.

Mid band gain:

(1M)

$$A = -g_m \left(\frac{R_1 \parallel R_2 \parallel r_\pi}{R_S + R_1 \parallel R_2 \parallel r_\pi} \right) (r_o \parallel R_C \parallel R_L) = -56.36$$

Miller's equivalent capacitor at the input:

(1M)

$$C_{Mi} = C_{bc} (1 + A) = (2.4p)(57.36) = 137.66pF$$

Miller's equivalent capacitor at the output:

(1M)

$$C_{Mo} = C_{bc} \left(1 + \frac{1}{A} \right) = (2.4p)(1.018) = 2.44pF$$

Thevenin's equivalent resistance at the input:

(1M)

$$R_i = R_S \parallel R_1 \parallel R_2 \parallel r_\pi = 600 \parallel 22k \parallel 4.7k \parallel 1.55k = 389.47\Omega$$

Thevenin's equivalent resistance at the output:

(1M)

$$R_o = R_C \parallel R_L \parallel r_o = 2.2k \parallel 2.2k \parallel 47.62k = 1.08k\Omega$$

Total input capacitance:

(1M)

$$C_{in} = C_{be} + C_{Mi} = 20p + 137.66p = 157.66pF$$

Total output capacitance:

(1M)

$$C_{out} = C_{Mo} = 2.44pF$$

Upper cutoff frequency introduced by input capacitance:

(2M)

$$f_{c_{(input)}} = \frac{1}{2\pi R_i C_{in}} = \frac{1}{2\pi(389.47)(157.66p)} = 2.59MHz$$

Upper cutoff frequency introduced by output capacitance:

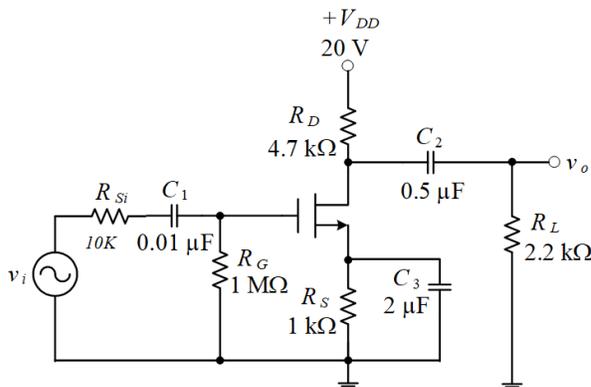
(2M)

$$f_{c_{(output)}} = \frac{1}{2\pi R_o C_{out}} = \frac{1}{2\pi(1.08k)(2.44p)} = 60.39MHz$$

Dominant upper cut off frequency: Lowest frequency- $f_H = 2.59MHz$

(2M)

Determine the lower cutoff frequency for the FET amplifier. Given $K = 0.4mA/V^2$, $V_{TN} = 1V$, $\lambda = 0$. (13M) BTL3



9

Answer: Page: 518 - Donald.

Input RC circuit:

(3M)

$$f_c = \frac{1}{2\pi R_{C1} C_1} = \frac{1}{2\pi(10K + 1M)(0.01\mu)} = 15.8Hz$$

Bypass RC circuit:

(3M)

$$f_c = \frac{1}{2\pi R_{C3} C_3} = \frac{1}{2\pi(1K \parallel 1/2m)(2\mu)} = 238.73Hz$$

Output RC circuit:

(3M)

$$f_c = \frac{1}{2\pi R_{C2} C_2} = \frac{1}{2\pi(4.7K + 2.2K)(0.5\mu)} = 46.13Hz$$

Dominant frequency: Highest Frequency = $f_H = f_c = 238.73Hz$

(2M)

Dominant Network diagram:
(2M)

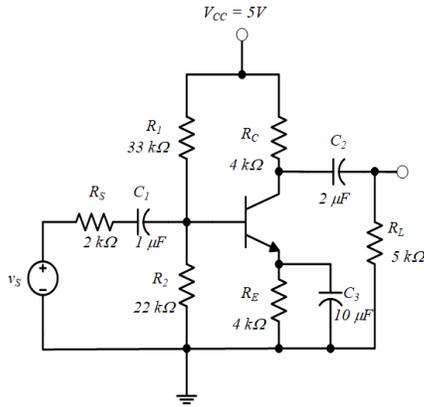
Determine the following for the CE amplifier given below.

i- Lower and upper cutoff frequencies

ii- Mid band gain

Assume $\beta = 120$, $C_{be} = 2.2 \text{ pF}$, $C_{bc} = 1 \text{ pF}$, $V_A = 100\text{V}$, $V_{BE(on)} = 0.7\text{V}$. (13M) BTL3

10



Answer: Page: 516 - Donald.

Base Current: Apply KVL- input Loop
(1M)

$$I_B = \frac{V_{BB} - V_{BE(on)}}{R_B + (\beta + 1)R_E} = 2.615 \mu\text{A}$$

Collector Current:

$$I_{CQ} = \beta I_B = 0.314 \text{ mA}$$

Transistor parameters values:

(1M)

$$r_\pi = \frac{\beta V_T}{I_{CQ}} = 9.94 \text{ k}\Omega, \quad r_o = \frac{V_A}{I_{CQ}} = 318.47 \text{ k}\Omega, \quad g_m = \frac{I_{CQ}}{V_T} = 12.08 \text{ mS}$$

Mid band Gain:

(1M)

$$A_{mid} = -g_m \frac{(R_B \parallel r_\pi)}{(R_S + R_B \parallel r_\pi)} (r_o \parallel R_C \parallel R_L) = -19.47$$

Lower cutoff frequency:

Due to C1, C2, C3:

(1M)

$$\omega_1 = \frac{1}{R_{1S}C_1} = 130.38 \text{ rad/s}, \quad \omega_2 = \frac{1}{R_{2S}C_2} = 55.87 \text{ rad/s}, \quad \omega_3 = \frac{1}{R_{3S}C_3} = 1060.9 \text{ rad/s}$$

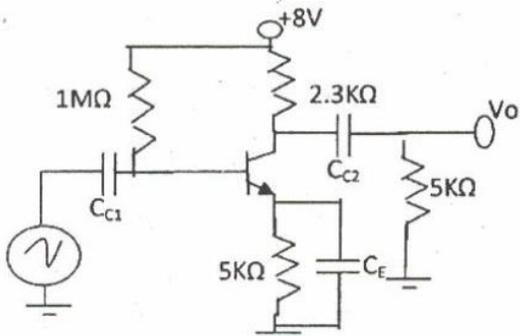
Dominant Lower cutoff frequency: highest value

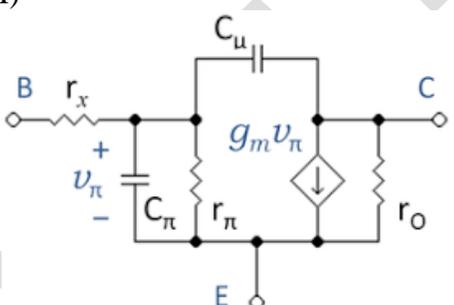
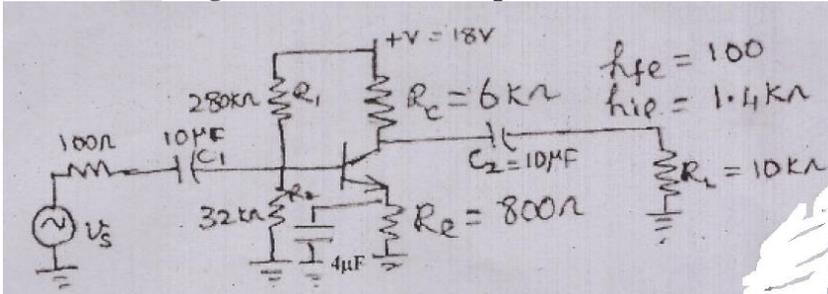
(1M)

$$f_L = \frac{\omega_3}{2\pi} = 169 \text{ Hz}$$

Upper cutoff frequency:

Miller Capacitance:

	<p>(1M)</p> $C_{Mi} = C_{bc}(1 + A) = (1p)(20.47) = 20.47 pF$ $C_{Mo} = C_{bc} \left(1 + \frac{1}{A} \right) = (1p)(1.051) = 1.05 pF$ $C_{in} = C_{be} + C_{Mi} = 22.67 pF, C_{out} = C_{Mo} = 1.05 pF$ <p>Input & output resistances:</p> <p>(1M)</p> $R_i = R_S \parallel R_1 \parallel R_2 \parallel r_\pi = 1.48 k\Omega, R_o = R_C \parallel R_L \parallel r_o = 2.18 k\Omega$ <p>Input side: (1M)</p> $f_{Hi} = \frac{1}{2\pi R_i C_{in}} = \frac{1}{2\pi(1.48k)(22.67p)} = 4.74 MHz$ <p>Output side: (1M)</p> $f_{Ho} = \frac{1}{2\pi R_o C_{out}} = \frac{1}{2\pi(2.18k)(1.05p)} = 69.53 MHz$ <p>Upper cutoff frequency: smallest value - $f_H = 4.74 MHz$ (1M)</p> <p>Frequency Response Diagram (2M)</p>
PART *C	
1	<p>For the circuit in fig has following parameters $h_{fe}=125$, $C_\pi=24pF$, $C_\mu=3pF$, determine its mid band and upper cut off frequencies, find the value of C_{c1}, C_{c2}, and C_e by assuming lower cutoff frequency of 100 Hz. (15M) (May 2015) BTL3</p>  <p>Answer: Page: 516 - Donald.</p> <p>Circuit diagram: Common Emitter BJT Amplifier. (1M)</p> <p>AC equivalent circuit: Short circuiting - input - output - bypass -coupling capacitors -Set DC voltage - zero. (1M)</p> <p>Small signal equivalent circuit: Replace transistor - Small signal hybrid pi equivalent model.</p> <p>Derivation of small signal parameters (1M)</p> <p>Short circuit current gain: $h_{fe} = \frac{gm r_\pi}{1 + j\omega r_\pi (C_\pi + C_\mu)}$ (2M)</p> <p>Cut off frequency: $f_\beta = \frac{1}{2\pi * r_\pi (C_\pi + C_\mu)}$ (2M)</p>

	<p>Unity gain bandwidth: $fT = \frac{f_o}{2\pi r\pi(C\pi+C\mu)}$</p> <p>(2M)</p> <p>Miller effect: (2M)</p> <p>Miller Capacitance $C_m=C\mu(1+ Av)$</p> <p>(2M)</p> <p>Voltage gain $Av=-g_m (R_c//R_L)$ (2M)</p>
<p>2</p>	<p>Construct the high frequency equivalent circuit of a MOSFET from its geometry and derive the expression for short circuit current gain in the common-source configuration. (15M) (Nov-2016) BTL 1</p> <p style="text-align: center;">(OR)</p> <p>Explain the high frequency operating of common source amplifier with its equivalent circuit. (15M) (April-2014) BTL1</p> <p>Answer: Page: 518 - Donald.</p> <p>Circuit diagram: Common source FET Amplifier. (2M)</p> <p>AC equivalent circuit: Short circuiting - input - output - bypass -coupling capacitors -Set DC voltage - zero. (2M)</p> <p>Small signal equivalent circuit: Replace transistor – Small signal hybrid pi equivalent model.</p> <p>Derivation of small signal parameters (2M)</p> <p>Short circuit current gain: $A_I = \frac{g_m}{j\omega(C_{gs}+C_{gd})}$ (3M)</p> <p>Unity gain bandwidth: $fT = \frac{g_m}{2\pi(C_{gs}+C_{gd})}$ (3M)</p> <p>Miller effect (3M)</p> <div style="text-align: center;">  </div>
<p>3</p>	<p>For the circuit given find cut off frequencies due to C1 and C2. (15M)(Nov 2014) BTL3</p> <div style="text-align: center;">  </div> <p>Answer: Page: 506 - Donald.</p> <p>Circuit diagram: Common Emitter BJT Amplifier.</p>

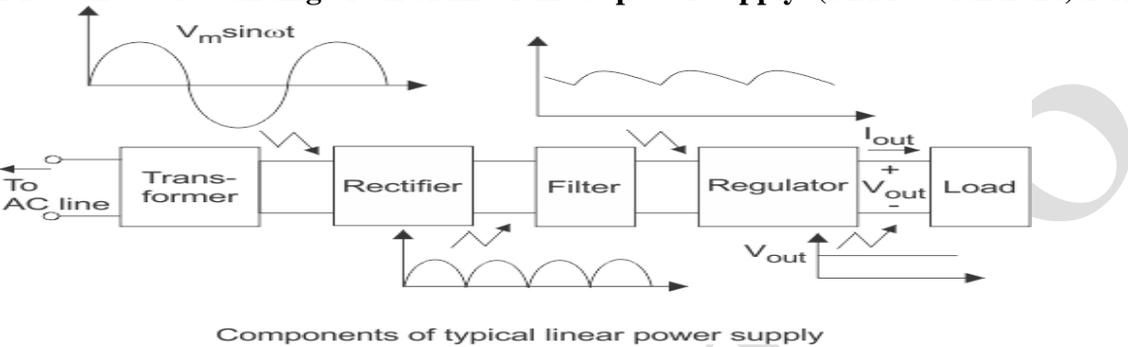
(2M)	AC equivalent circuit: Short circuiting - input – output - bypass -coupling capacitors -Set DC voltage - zero. (2M)
	Small signal equivalent circuit: Replace transistor – Small signal hybrid pi equivalent model.
Derivation	of
of	small
of	signal
of	parameters
(2M)	Cut off frequency due to C1= $1/(2\pi R_{in}C_1)=11.36\text{Hz}$
(2M)	Cut off frequency due to C2 = $1/(2\pi(R_C+R_L))=0.99\text{Hz}$ (2M)
(2M)	Cut off frequency due to bypass Capacitor $=\frac{1}{2\pi[(h_{ie}+R_{th})/\beta//R_e]C_e}=369\text{Hz}$
(2M)	Frequency Response: (3M)

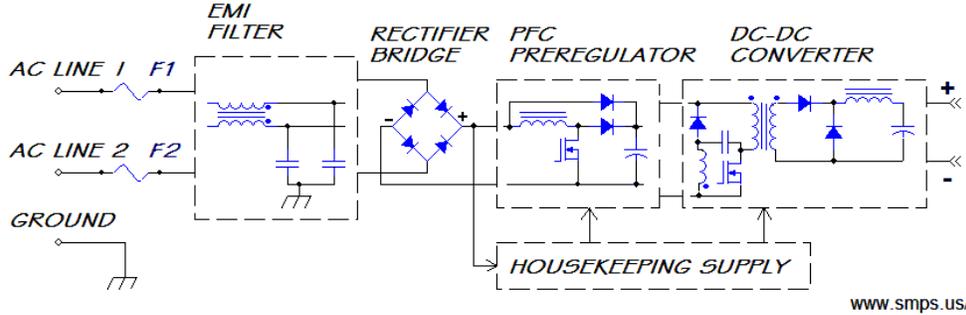
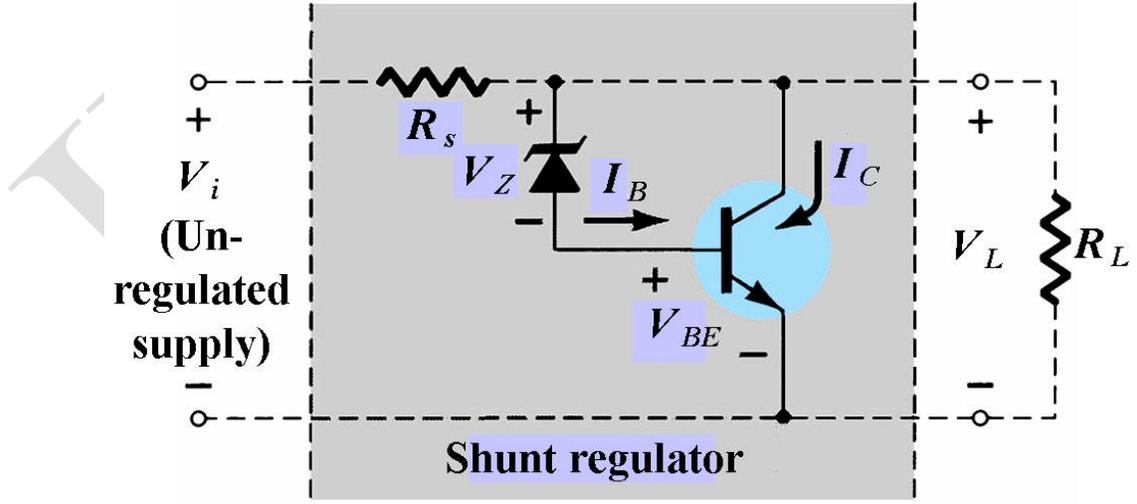
UNIT V–POWER SUPPLIES AND ELECTRONIC DEVICE TESTING	
Linear mode power supply - Rectifiers - Filters - Half-Wave Rectifier Power Supply - Full-Wave Rectifier Power Supply - Voltage regulators: Voltage regulation - Linear series, shunt and switching Voltage Regulators - Over voltage protection - BJT and MOSFET – Switched mode power supply (SMPS) - Power Supply Performance and Testing - Troubleshooting and Fault Analysis, Design of Regulated DC Power Supply.	
PART * A	
Q.No.	Questions
1.	Write necessity of a dc power supply in electronic circuits. BTL1 The dc power supply provides a unipolar voltage. A number of electronic circuits such as amplifiers, oscillators, etc., and appliances such as TV, VCR, etc., operate fully or partly on dc power supply. Hence it is an important device.
2	What is a rectifier? What are its types? BTL1 A rectifier is a device which converts ac voltage to pulsating dc voltage, using one or more p-n junction diodes. The types are half wave rectifier and full wave rectifier.
3	What are the important points to be studied while Analyzing the various rectifier circuits? BTL1 <ol style="list-style-type: none"> 1. Waveform of the load current 2. Regulation of the output voltage 3. Rectifier efficiency 4. Peak value of current in the rectifier circuit 5. Peak inverse voltage of the diode 6. Ripple factor
4	Write the expression for rectification efficiency and the values for the same for the rectifiers. BTL1 Rectification efficiency $\eta = \text{DC output power} / \text{AC input power} = P_{DC} / P_{AC}$ η of HWR = 40.6% η of FWR = 81.2%
5	What are the disadvantages of an HWR? BTL1 <ol style="list-style-type: none"> 1. HWR uses only one diode hence the output is obtained for only one-half cycle of the input. Hence the theoretical rectification efficiency is only 40.6%. Practical value will still be less. 2. Also, the circuit suffers from dc saturation. 3. Since the dc current through the load also flows through the secondary winding of the transformer, the core of the transformer experience dc saturation. To minimize the saturation, the transformer size has to be increased accordingly. 4. This increases the cost. The ripple factor is too high. So, the output contains a lot of varying components. The circuit has low transformer utilization factor, showing that the transformer is not fully utilized.
6	What is voltage regulation? BTL1 The voltage regulation is the ratio of change in dc output voltage between no load and full load to dc voltage at full load. $\% \text{ Voltage Regulation} = \frac{V_{dc(NL)} - V_{dc(FL)}}{V_{dc(FL)}} * 100$
7	Compare HWR and FWR. (May 2010) BTL1

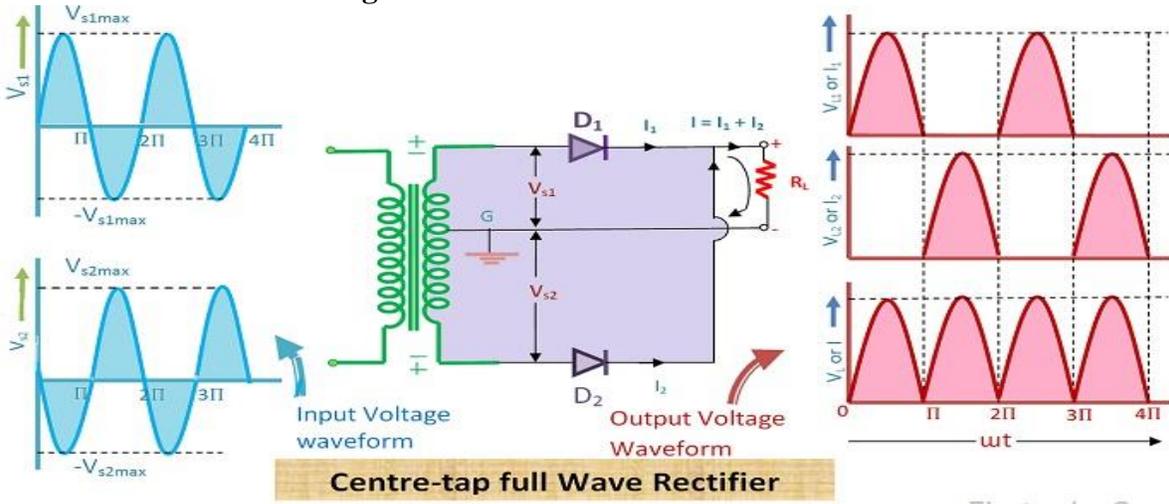
S.No	Item	Half-wave	Full-wave centre tapped	Full-wave Bridge
1.	No. of diodes	1	2	4
2.	Peak Inverse voltage of diode	V_m	$2V_m$	V_m
3.	DC output voltage	$0.318V_m$	$0.636V_m$	$0.636V_m$
4.	Ripple factor	1.21	0.482	0.482
5.	Ripple frequency	f_m	$2 f_m$	$2 f_m$
6.	TUF	0.287	0.693	0.81

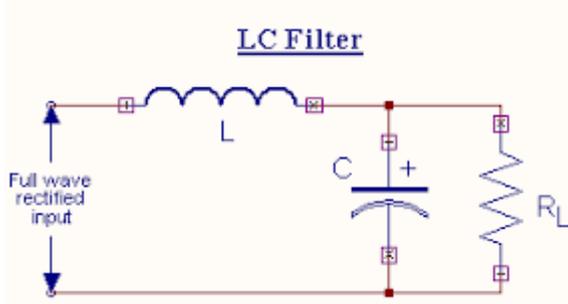
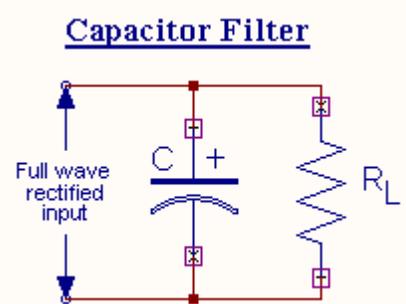
8	<p>Write some applications of bridge rectifier. BTL1</p> <p>This is used as a power rectifier circuit for converting ac power to dc power and a rectifying system in rectifier type ac meters such as ac voltmeter.</p>
9	<p>Compare centre tapped FWR and bridge rectifier circuits. (May 2012) BTL2</p> <ol style="list-style-type: none"> The transformer used in centre tapped FWR has three terminals in secondary but in bridge rectifier two terminals in the secondary are sufficient. The peak inverse voltage of each diode in bridge rectifier is V_m whereas in centre tapped FWR is $2 V_m$.
10	<p>What is CLC filter? (MAY JUNE 2014) BTL1</p> <p>CLC filter, the capacitor-input filter, also called pi Filter due to its shape that looks like the Greek letter π is a type of electronic filter. Filter circuits are used to remove unwanted or undesired frequencies from a signal.</p>
11	<p>Define TUF and rectification efficiency. (May 2009) BTL1</p> <p>TUF may be defined as the ratio of dc power delivered to the load and the ac rating of the transformer secondary. Mathematically, the transformer utilization factor or the TUF is given by</p> $\text{TUF} = \text{DC power delivered to the load} / \text{AC rating of the transformer secondary} = P_{dc} / P_{ac} (\text{rated})$ <p>Rectification efficiency is defined as the ratio of the dc power delivered to the load to the ac input power from the secondary winding of the transformer. This is given by,</p> $\eta = \text{DC power delivered to the load} / \text{AC input power from the transformer secondary} = P_{dc} / P_{ac}$
12	<p>Which filter is used in high current applications? BTL1</p> <p>Inductor filter is used in high current applications since its ripple factor reduces with low load resistance.</p>
13	<p>What is the advantage of fold back current limiting? BTL1</p> <p>This method uses the variation of output voltage and varies the load current accordingly. So, if the load resistance decreases, both current and voltage are brought to minimum, so the power consumption by the load is small.</p>
14	<p>Explain briefly the term critical inductance. BTL1</p> <p>The value of the inductance of the choke filter that makes the diode to conduct the entire 180° of the ac supplies is called critical inductance.</p>
15	<p>List three reasons why an unregulated supply is not good enough for some applications? BTL1</p> <ol style="list-style-type: none"> For electronic circuits, and appliances unregulated power supply possess a serious problem because any irregular variation in voltage will prevent proper operation of devices. A surge current or any such increase in current may damage the low current devices.

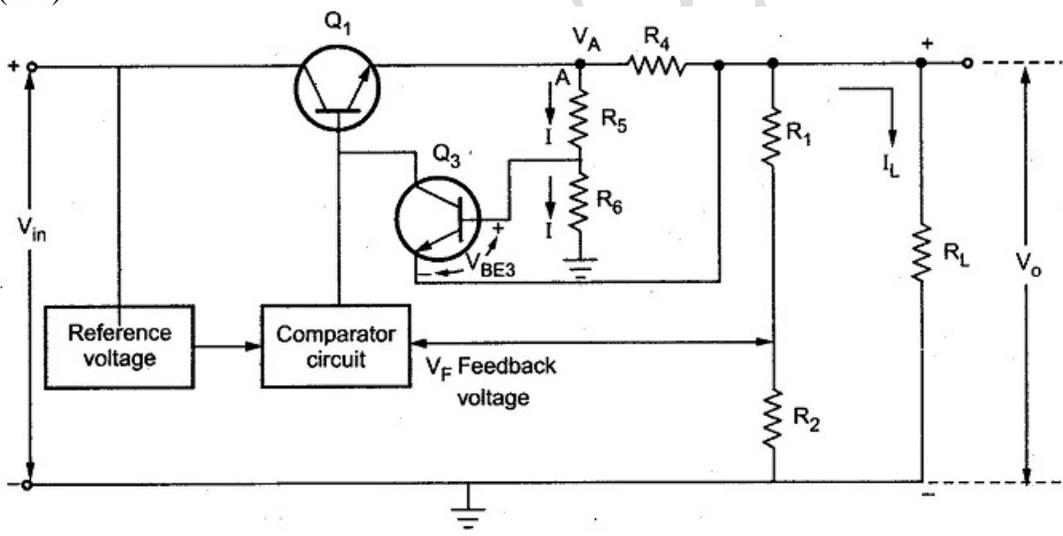
	3. For various load conditions, an unregulated power supply outputs a continuously varying output which decreases the performance of the circuit.
16	What is the function of a filter? BTL1 A filter smoothes out the ripples present in the output of a rectifier and hence produces unregulated dc output.
17	Why are protection circuits required for dc power supplies? BTL1 In dc power supplies short circuiting or overload condition draws a heavy current which damages the devices in series. Hence protection circuits are required.
18	List the merits of IC regulators. BTL1 They are compact, easy to use and provide a fixed voltage. The connections necessary are very less. They provide local regulation in electronics systems that may require several different supply voltages.
19	What are the values of PIV for HWR and FWR using ideal diode and sinusoidal input? BTL1 The PIV for <ol style="list-style-type: none"> 1. HWR, is V_m 2. Center tapped FWR, is $2V_m$ 3. Bridge rectifier, is V_m.
20	For a voltage regulator, the output voltage at a load current of 100mA is 6V. The percentage regulation is 30%. Find the no load output voltage. BTL3 $\% \text{ Regulation} = \frac{V_{NL} - V_{FL}}{V_{FL}} \times 100$ $V_{NL} = \frac{(\text{Regulation} \times V_{FL})}{100} + V_{FL}$ $= \frac{(30 \times 6)}{100} + 6$ $= 7.80$ The no load voltage = 7.80V
21	What is the frequency of dc signal? BTL1 The frequency of DC signal is 0 Hz.
22	What is the function of a bleeder resistor? BTL1 <ol style="list-style-type: none"> 1. It maintains the minimum current necessary for optimum operation of the inductor and hence limits the values of critical inductance. 2. It prevents dangerous shocks and provides safety to the persons handling the equipment, by acting as a discharging path for capacitors. 3. It acts as a preload on the supply and draws a fixed amount of current continuously from the power supply so that the output voltage at no load is reduced and voltage regulation is improved.
23	List the disadvantages of Zener regulator. BTL1 <ol style="list-style-type: none"> 1. The maximum load current $I_{L_{max}}$ is limited between $I_{Z_{max}}$ and $I_{Z_{min}}$ which is usually of few milliamperes. 2. A large amount of power is wasted in the Zener diode and the source resistance so that the power output is decreased. 3. The regulation factor and the output resistance are not very low.
24	Mention how overload protection is provided in series voltage regulators. BTL1 Overload protection is provided by current limiting and foldback limiting methods. When the load resistance decreases to a minimum, the current drawn is usually very high. This is limited using current limiting circuitry and thus overload protection is provided.
25	What is voltage multiplier? (May 2008) BTL1 Voltage multiplier circuits have the capability of delivering a DC voltage two or more times the peak value V_m of the applied AC voltage.

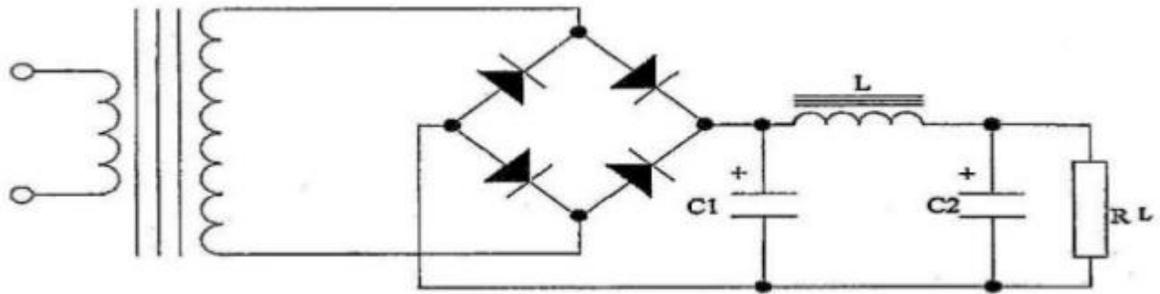
26	<p>Define Line regulation and Load regulation. (May 2012) BTL1</p> <ol style="list-style-type: none"> 1. Load regulation 2. The ability of the power supply to maintain the constant DC output voltage for a wide variation in load current is called load regulation. 3. Line regulation 4. The ability of the power supply to maintain the constant output voltage for the input supply fluctuations for a constant load is called line regulation.
27	<p>Draw the basic building block of linear mode power supply. (MAY JUNE 2014) BTL1</p>  <p style="text-align: center;">Components of typical linear power supply</p>
PART *B	
1	<p>Explain the circuit of voltage regulator and also discuss the short circuit protection mechanism. (8M) (Nov 2009) BTL1 Answer: Page 754 – S. Salivahanan & 6.36,6.52- Bakshi</p> <p>Definition: Ratio - change in dc output voltage between no load and full load - dc voltage at full load.</p> <p>Circuit provides- regulated supply - regulators. (2M)</p> <p>Types – Series, Shunt (2M)</p> <p>IC Voltage regulators (2M)</p> <p>Short Circuit Protection. $R_{sc}=0.7/I_{limit}$ (2M)</p>
2	<p>Design Zener regulator for following specification. $V_{in}=8V$ to $12V$, $V_o=10V$, $R_i=10K$ Assume that Zener diode is Ideal. (13M) (Nov 2009) BTL3 Answer: Page 756 – S. Salivahanan.</p> <p>Load Resistance: $R_{Lmin}=V_o/I_{Lmax}$ (4M) $R_{Lmax}=V_o/I_{Lmin}$</p> <p>(4M)</p> <p>Input Resistance: $R=1/2*(R_{max}+R_{min})$ (5M)</p>
3	<p>In a full wave rectifier, a signal of $300 V$ $50Hz$ is applied at the input, each diode has an internal resistance of 800Ω. If the load is 2000Ω, Determine Instant peak value of current in the output, Output DC current and efficiency of power transfer. (8M) (Nov 2012) BTL1 Answer: Page 733 – S. Salivahanan.</p> <p>Maximum Current $I_m=V_m/(r_s+r_f+R_L)$ (4M)</p> <p>Output DC current $I_{dc}=2*I_m/\pi$ (2M)</p> <p>Efficiency $\eta = P_{dc}/P_{ac}$ (2M)</p>

<p>4</p>	<p>Explain SMPS. (13M) (Nov 2012) (April 2011) (April 2010) (June 2013) (June 2014) BTL1 Answer: Page 772– S.Salivahanan & 6.60- Bakshi</p> <p>Definition: A switched-mode power supply (SMPS) - electronic circuit - converts power using switching devices - turned - off at high frequencies - storage components - inductors -capacitors - supply power -switching device - non-conduction state. (2M)</p> <p>Block diagram (2M)</p>  <p>Types of SMPS (2M) Buck Converter (2M) Boost Converter (2M) Buck-Boost Converter (2M) Comparison (1M)</p>
<p>5</p>	<p>Describe the operation of a shunt voltage regulator (8M) (Nov 2011) BTL1 Answer: Page 765 – S.Salivahanan. & 6.41- Bakshi</p> <p>Definition: The transistor shunt voltage regulator- regulates voltage - shunting current - load - regulate the output voltage; (2M)</p> <p>Zener shunt Regulator: (3M) Transistorized Shunt Regulator: (3M)</p> 
<p>6</p>	<p>Explain the operation of capacitor filter in full wave rectifier circuit. And derive the equation for ripple factor for the circuit and explain advantages of capacitor filter. (13M) (Nov 2011)</p>

	<p>BTL1 Answer: Page 743 – S.Salivahanan & 6.20- Bakshi Capacitor Filter: Capacitor - connected across - load - reduce ripples. (3M) Waveform and Circuit Diagram: (3M)</p>  <p style="text-align: right;">Electronics Coach</p> <p>RMS value: $V_{rms} = I_{dc} / 4\sqrt{3}fC$ (4M) Ripple Factor $= \frac{1}{4\sqrt{3}fCR_L}$ (3M)</p>
<p>7</p>	<p>Derive the expression for conversion efficiency of full wave rectifier. Assume forward resistance as R_f (8M) (April 2011) BTL1 Answer: Page 730 – S.Salivahanan & 6.8- Bakshi Definition: Rectification efficiency (Conversion efficiency) - ratio - dc power delivered to the load - ac input power - secondary winding - transformer. (2M) Circuit Diagram & Wave form (4M) Conversion efficiency $\eta = P_{dc} / P_{ac} = 81.2\%$ (2M)</p>
<p>8</p>	<p>Explain various techniques for ripple reduction in Rectifiers. (13M) (April 2011) BTL1 Answer: Page 740 – S.Salivahanan & 6.20- Bakshi Filters: Ripples present - filter output - reduced - various filters. (3M) Types (2M) Inductor Filter (2M) Capacitor Filter (2M) LC Filter (2M) CLC Filter (2M)</p>
<p>9</p>	<p>Derive the expression for rectification efficiency, ripple factor, TUF, form factor and peak factor of HWR and FWR. (13M) (April 2010) BTL1 Answer: Page 754 – S.Salivahanan & 6.3- Bakshi Definition: Convert AC to DC (2M) Types: Half Wave Rectifier, Full Wave Rectifier (1M) Circuit Diagram, Working principal & Wave form (2M) Rectification efficiency $\eta = P_{dc} / P_{ac} = 81.2\%$ (FWR), 40.6% (HWR) (2M) Ripple Factor = 0.482 (FWR) , 1.21(HWR) (2M) Form Factor =1.11 (FWR), 1.57(HWR)</p>

	(2M) Peak Factor = $\sqrt{2}$ (FWR) , 2 (HWR) (2M)									
10	<p>Explain working of FWR with CLC filter and derive its ripple factor. (8M) (Nov 2010) BTL1 Answer: Page 750 – S.Salivahanan & 6.33- Bakshi Definition: A rectifier circuit - 2 diodes - CLC filter circuit - converting AC to DC. (2M) Circuit Diagram & Wave form (4M) Ripple factor = $3300/C_1C_2L_1R_L$ (2M)</p>									
11	<p>Compare HWR and FWR with respect to output average voltage and ripple factor (4M). BTL1 Answer: Page 722 – S.Salivahanan.</p> <table border="1" style="width: 100%; border-collapse: collapse; text-align: center;"> <thead> <tr> <th style="width: 30%;">Parameter</th> <th style="width: 35%;">HWR</th> <th style="width: 35%;">FWR</th> </tr> </thead> <tbody> <tr> <td>Output average voltage (2M)</td> <td>$V_{dc}=V_m/\pi$</td> <td>$V_{dc}=2*V_m/\pi$</td> </tr> <tr> <td>Ripple factor (2M)</td> <td>1.21</td> <td>0.482</td> </tr> </tbody> </table>	Parameter	HWR	FWR	Output average voltage (2M)	$V_{dc}=V_m/\pi$	$V_{dc}=2*V_m/\pi$	Ripple factor (2M)	1.21	0.482
Parameter	HWR	FWR								
Output average voltage (2M)	$V_{dc}=V_m/\pi$	$V_{dc}=2*V_m/\pi$								
Ripple factor (2M)	1.21	0.482								
12	<p>Draw and explain FWR with resistive load. (13M) (Dec 2013) (Dec 2014) BTL1 Answer: Page 730 – S.Salivahanan & 6.8- Bakshi Introduction: A rectifier circuit - one diode - resistive load is considered. (2M) Circuit Diagram & Wave form (2M) Rectification efficiency $\eta = P_{dc}/P_{ac} = 81.2\%$ (2M) Ripple Factor = 0.482 (2M) Form Factor = 1.11 (2M) Peak Factor = $\sqrt{2}$ (3M)</p>									
13	<p>Explain the use of C and LC filters for improving performance of the circuit (13M) (Dec 2013) BTL1 Answer: Page 743 – S.Salivahanan & 6.20- Bakshi Capacitor Filter: Capacitor - connected - load - reduce ripples. (2M) Waveform and Circuit Diagram (2M)</p> <div style="display: flex; justify-content: space-around; align-items: flex-start;"> <div style="text-align: center;"> <p><u>LC Filter</u></p>  </div> <div style="text-align: center;"> <p><u>Capacitor Filter</u></p>  </div> </div> <p>Ripple Factor = $\frac{1}{4\sqrt{3}fCR_L}$ (2M) LC Filter: Inductor is connected across the load to reduce ripples. (2M)</p>									

	<p>Waveform and Circuit Diagram (2M)</p> <p>Ripple Factor $= \frac{\sqrt{2}}{3\omega^2 C_L}$ (3M)</p>
<p>14</p>	<p>Describe the principle of operation of Zener voltage regulator. (10M) (Nov 2013) BTL1 Answer: Page 755 – S.Salivahanan & 5.11- Bakshi Definition and Block Diagram: Basic Zener diode - used - voltage regulator. (4M) Load Resistance: $R_{Lmin} = V_o / I_{Lmax}$ (2M) $R_{Lmax} = V_o / I_{Lmin}$ (2M) Input Resistance: $R = 1/2 * (R_{max} + R_{min})$ (2M)</p>
<p>15</p>	<p>Draw a neat diagram of series voltage regulator with foldback protection and explain its working. (6M) (Dec 2014) BTL1 Answer: Page 765 – S. Salivahanan & 6.54- Bakshi Definition : Foldback is a current limiting feature (a type of overload protection) - power supplies - power amplifiers. When - load attempts - draw overcurrent - supply, foldback - reduces - output voltage - current - below - normal operating limits. Under a short circuit, -output voltage - reduced to zero- current - typically limited - small fraction - maximum current. (1M) Block Diagram (2M)</p>  <p>Explanation (3M)</p>
<p>16</p>	<p>Explain working of FWR with π filter and derive its ripple factor. (10M) (June 2013) BTL1 Answer: Page 750 – S. Salivahanan & 6.33- Bakshi Definition: A rectifier circuit - 2 diodes - π filter circuit - considered - converting AC - DC (2M) Block Diagram: (2M)</p>



Explanation:

(3M)

Ripple factor = $3300/C_1C_2L_1R_L$

(3M)

PART *C

1

Explain the basic operation of FWR and Bridge rectifier and derive its ripple factor, efficiency and TUF. (15M) (June 2014) BTL1

Answer: Page 731 – S.Salivahanan & 6.33- Bakshi

Definition:

Maximum Current: $I_m = V_m / (r_s + r_f + R_L)$

(2M)

Output DC current: $I_{dc} = 2 * I_m / \pi$

(2M)

Efficiency: $\eta = P_{dc} / P_{ac}$

(2M)

Ripple Factor = $\sqrt{((V_{rms} / V_{dc}))^2 - 1}$

(3M)

TUF = 0.693

(2M)

Form Factor = 1.11

(2M)

Peak Factor = $\sqrt{2}$

(2M)

2

An HWR is supplied from with a step-down ratio of 3:1 to resistive load of 10K. Diode forward resistance is 75K, transformer sec resistance is 10K, Find I_{max} , I_{avg} , I_{rms} , I_{dc} , Efficiency and ripple factor. (15M) (may 2015) Answer: Page 722– S.Salivahanan. BTL3

Output DC current $I_{dc} = I_m / \pi$

(2M)

Efficiency $\eta = P_{dc} / P_{ac}$

(2M)

Ripple Factor = $\sqrt{((V_{rms} / V_{dc}))^2 - 1}$

(3M)

TUF = 0.287

(3M)

Form Factor = 1.57

(3M)

Peak Factor = 2

(2M)

3

With neat diagram explain Buck and Boost switching regulator. (15M) (May 2015) BTL1

Answer: Page 772 – S.Salivahanan & 6.61- Bakshi

Definition: Step-down/up switching regulators, - called buck-boost converters.

Output level - either higher or lower - input voltage.

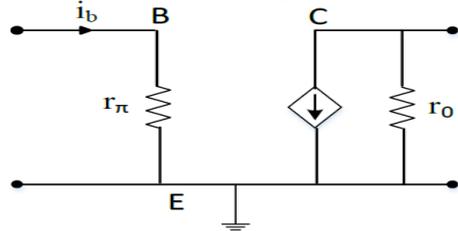
Combining buck - boost technology - single DC-DC converter- step-down/up converter - handle -

wide range of input voltages - either higher - lower - required by the circuit.	(2M)
Types: Buck and boost regulator.	(4M)
Block diagram and model graph. (4M)	
Explanation	(5M)

JIT - 2106

MULTIPLE CHOICE QUESTIONS-UNIT I

The current I_b through base of a silicon NPN transistor is $1+0.1 \cos (1000\pi)t$ ma. At 300K, the r_{π} in the small signal model of the transistor is

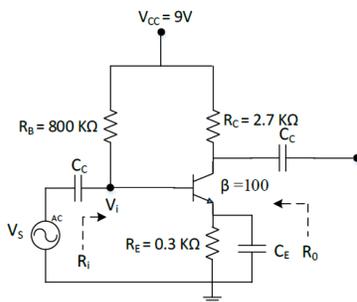


1

- (a) 250Ω
- (b) 27.5Ω
- (c) 25Ω
- (d) 22.5Ω

Ans :(c) 25Ω

The amplifier circuit shown below uses a silicon transistor. The capacitors C_C and C_E can be assumed to be short at signal frequency and the effect of output resistance r_o can be ignored. If C_E is disconnected from the circuit, which one of the following statements is TRUE?

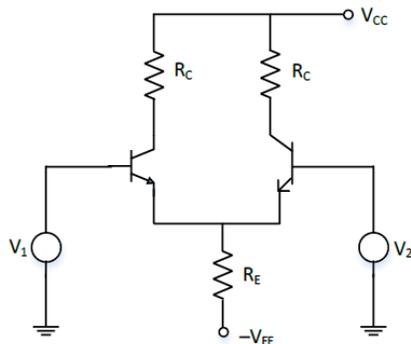


2

- (a) The input resistance R_i increases and the magnitude of voltage gain A_V decreases.
- (b) The input resistance R_i decreases and the magnitude of voltage gain A_V increases.
- (c) Both input resistance R_i and the magnitude of voltage gain A_V decrease.
- (d) Both input resistance R_i and the magnitude of voltage gain A_V increase.

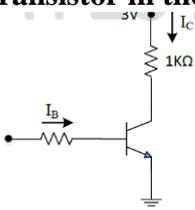
Answer (a)The input resistance R_i increases and the magnitude of voltage gain A_V decreases.

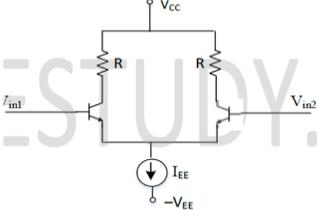
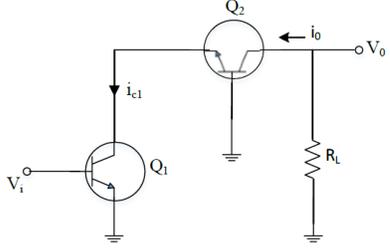
In an ideal differential amplifier shown in the figure, a large value of (R_E) .

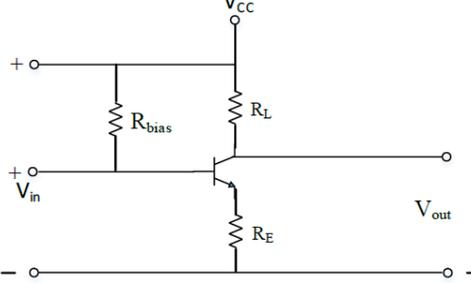
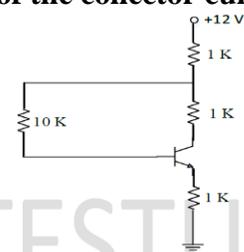


3

- (a) Increases both the differential and common-mode gains.
- (b) Increases the common-mode gain only

	<p>(c) Decreases the differential-mode gain only (d) Decreases the common-mode gain only Answer (d)Decreases the common-mode gain only</p>
4	<p>The cascode amplifier is a multistage configuration of (a) CC-CB (b) CE-CB (c) CB-CC (d) CE-CC Ans: (b) CE-CB</p>
5	<p>Assuming $V_{CEsat} = 0.2\text{ V}$ and $\beta = 50$, the minimum base current (I_B) required to drive the transistor in the figure to saturation is</p>  <p>(a) $56\ \mu\text{A}$ (b) $140\ \mu\text{A}$ (c) $60\ \mu\text{A}$ (d) $3\ \mu\text{A}$ Ans: (a) $56\ \mu\text{A}$</p>
6	<p>Generally, the gain of a transistor amplifier falls at high frequency due to the (a) Internal capacitance of the device (b) Coupling capacitor at the input (c) Skin effect (d) Coupling capacitor at the output Ans:(a) Internal capacitance of the device</p>
7	<p>The current gain of a BJT is (a) $g_m r_0$ (b) g_m / r_0 (c) $g_m * r_\pi$ (d) g_m / r_π Ans: (c) $g_m * r_\pi$</p>
8	<p>The current gain of a bipolar transistor drops at high frequencies because of (a) Transistor capacitances (b) High current effects in the base (c) Parasitic inductive elements (d) The Early effect Ans: a) Transistor capacitances</p>
9	<p>In the differential amplifier of the figure, if the source resistance of the current source IEE is infinite, then common-mode gain is</p>

	 <p>(a) Zero (b) Infinite (c) Indeterminate (d) $(V_{in1} + V_{in2}) + 2VT$ Ans:(a) Zero</p>
10	<p>In the Cascode amplifier shown in the figure, if the common-emitter stage (Q1) has a trans conductance g_{m1} and the common base stage (Q2) has a trans conductance g_{m2} then the overall trans conductance $g(=i_o / V_i)$ of the Cascode amplifier is</p>  <p>(a) g_{m1} (b) g_{m2} (c) $g_{m1} / 2$ (d) $g_{m2} / 2$ Ans:(a) g_{m1}</p>
11	<p>The unit of q / KT are</p> <p>(a) V (b) V-1 (c) J (d) J / K Ans:(b) V-1</p>
12	<p>A multistage Amplifier has a low-pass Response with three-real poles at $s = -\omega_1, -\omega_2$ and ω_3 The approximate overall bandwidth B of the Amplifier will be given by</p> <p>(a) $B = \omega_1 + \omega_2 + \omega_3$ (b) $1/B=1/\omega_1+1/\omega_2+1/\omega_3$ (c) $B=(\omega_1+\omega_2+\omega_3)1/3$ (d) $B=\sqrt{\omega_1^2+\omega_2^2+\omega_3^2}$ Ans: (b) $1/B=1/\omega_1+1/\omega_2+1/\omega_3$</p>
13	<p>From measurement of the rise time of the o/p pulse of an amplifier whose input is a small amplitude square wave, one can estimate the following parameter of the amplifier.</p> <p>(a) Gain-bandwidth product (b) Slew-Rate (c) Upper-3-dB frequency (d) Lower-3-dB frequency</p>

	Ans: (c) Upper-3-dB frequency
14	<p>Cascode amplifier stage is equivalent to</p> <p>(a) A common emitter stage following by a common base stage (b) A common base stage followed by an emitter follower (c) An emitter follower stage followed by a common base stage (d) A common base stage followed by a common emitter stage</p> <p>Ans: (a) A common emitter stage following by a common base stage</p>
15	<p>In the BJT amplifier shown in the figure is the transistor is biased in the forward active region putting a capacitor across RE will</p>  <p>(a) Decrease the voltage gain and decrease the i/p impedance (b) Increase the voltage gain and decrease the i/p impedance (c) Decrease the voltage gain and increase the i/p impedance (d) Increase the voltage gain and increase the i/p impedance</p> <p>Ans:(b) Increase the voltage gain and decrease the i/p impedance</p>
16	<p>A transistor having $\alpha = 0.99$ and $V_{BE} = 0.7V$, is used in the circuit of the figure is the value of the collector current will be</p>  <p>a) 1mA b) 3.44mA c) 2mA d) 5.33mA</p> <p>Answer d) 5.33 mA</p>
17	<p>A BJT is said to be operating in the saturation Region if</p> <p>(a) Both the junction are reverse biased. (b) Base-emitter junction is reverse biased and base-collector junction is forward biased. (c) Base-emitter junction is forward biased and base-collector junction is reverse-biased. (d) Both the junction are forward biased.</p> <p>Ans:(d) Both the junction are forward biased.</p>
18	<p>which of the following statements are correct for basic transistor amplifier configurations</p> <p>(a) CB amplifier has low input impedance and low current gain.</p>

	<p>(b) CC amplifier has low output impedance and high current gain (c) CE amplifier has very poor voltage gain but very high input impedance (d) The current gain of CB amplifier is higher than the current gain of CC</p> <p>Answer (a) & (b)</p>
19	<p>The bandwidth of an n-stage tuned amplifier, with each stage having a bandwidth of B, is given by.</p> <p>(a) B/n (b) B/\sqrt{n} (c) $B\sqrt{2^{1/n}-1}$ (d) $B/\sqrt{2^{1/n}-1}$</p> <p>Ans:(c) $B\sqrt{2^{1/n}-1}$</p>
20	<p>The quiescent collector current I_C of a transistor is increased by changing resistances. As a result.</p> <p>(a) gm will not be affected (b) gm will decrease (c) gm will increase (d) gm will increase or decrease depending upon bias stability.</p> <p>Ans:(c) gm will increase</p>
MULTIPLE CHOICE QUESTIONS-UNIT II	
1.	<p>Early effect in BJT refers to</p> <p>(a) avalanche breakdown (b) thermal breakdown (c) base narrowing (d) Zener breakdown</p> <p>Ans: (c) base narrowing</p>
2.	<p>The emitter of the transistor is generally doped the heaviest because it</p> <p>(a) has to dissipate maximum power (b) has to supply the charge carriers (c) is the first region of transistor (d) must possess low resistance</p> <p>Ans :(b) has to supply the charge carriers</p>
3.	<p>In a properly Biased NPN transistor most of the electrons from the emitter</p> <p>(a) recombine with holes in the base (b) recombine in the emitter its self (c) pass through the base to the collector (d) are stopped by the junction barrier</p> <p>Ans: (c) pass through the base to the collector</p>
4.	<p>In a transistor amplifier, the reverse saturation current I_{CO}</p> <p>(a) double for every 100rise in temperature</p>

	<p>(b) doubles for every 10rise in temperature (c) increase linearly with the temperature (d) doubles for every 50rise in temperature Ans:(a) double for every 100rise in temperature</p>
5.	<p>Which of the following transistor configuration circuit is much less temperature dependent (a) common base (b) common emitter (c) common collector (d) none of the above Ans: (c) common collector</p>
6.	<p>The CE amplifier circuit are preferred over CB amplifier circuit because they have (a) lower amplification factor (b) larger amplification factor (c) high input resistance and low output resistance (d) none of these Ans:(b) larger amplification factor</p>
7.	<p>Transistor connected in common base configuration has (a) a high input resistance and low output resistance (b) a low input resistance and high output resistance (c) a low input resistance and low output resistance (d) a high input resistance and a high output resistance Ans: (b) a low input resistance and high output resistance</p>
8.	<p>A transistor when connected in CE mode has (a) a low input resistance and a low output resistance (b) a high input resistance and high output resistance (c) a high input resistance and low output resistance (d) a medium input resistance and high output resistance Ans:(d) a medium input resistance and high output resistance</p>
9.	<p>The collector characteristics of a common- emitter connected transistor may be used to find its (a) input resistance (b) base current (c) output resistance (d) voltage gain Ans: (c) output resistance</p>
10.	<p>The dc load line of transistor circuit (a) is a graph between I_C and V_{CE} (b) is a graph between I_C and I_B (c) does not contain the Q Point (d) is a curved line Ans:(a) is a graph between I_C and V_{CE}</p>

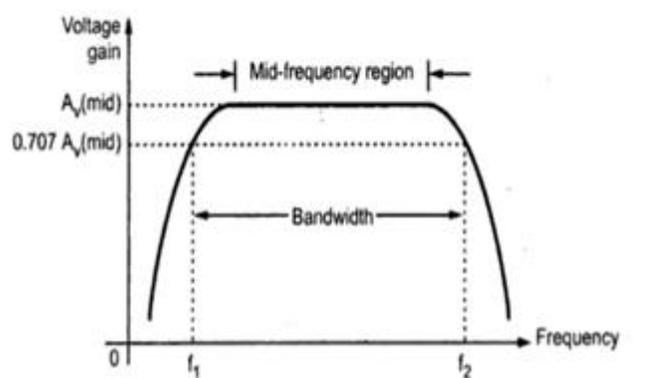
11.	<p>The ac load line of a transistor circuit is steeper than its dc line because</p> <p>(a) ac signal sees less load resistance (b) IC is higher (c) input signal varies in magnitude (d) none of the above</p> <p>Ans:(a) ac signal sees less load resistance</p>
12.	<p>The maximum peak to peak output voltage swing is obtained when Q point of a circuit is located</p> <p>(a) near saturation point (b) near cut off point (c) at the centre of the load line (d) at least on the load line</p> <p>Ans:(c) at the centre of the load line</p>
13.	<p>The positive part of the output signal in a transistor circuit starts clipping, if Q point of the circuit moves</p> <p>(a) toward the saturation point (b) toward the cut-off point (c) toward the centre of the load line (d) none of the above</p> <p>Ans:(b) toward the cut-off point</p>
14.	<p>The biasing circuit that gives best stability to Q point is</p> <p>(a) base resistance biasing (b) feedback resistor biasing (c) potential divider biasing (d) emitter resistor biasing</p> <p>Ans:(c) potential divider biasing</p>
15.	<p>The Q-point in a voltage amplifier is selected in the middle of the active region because</p> <p>(a) it gives better stability (b) the circuit needs a small (c) the biasing circuit then need less number of resistors (d) it gives distortions less output</p> <p>Ans:(d) it gives distortions less output</p>
16.	<p>The ideal value of stability factor of a biasing circuit is</p> <p>(a) 1 (b) 5 (c) 10 (d) 100</p> <p>Ans:(a) 1</p>
17.	<p>The universal bias stabilization circuit is the most popular because</p> <p>(a) IC does not depend on transistor characteristic (b) its β sensitivity is low</p>

	<p>(c) voltage divider is heavily loaded by transistor base (d) IC equals to IE Ans:(b) its β sensitivity is low</p>
18.	<p>For a transistor amplifier with self- biasing network, the following components are used: $R_1 = 4K\Omega$, $R_2 = 4K\Omega$ and $R_E = 1K\Omega$, the approximate value of stability factor will be (a) 4 (b) 3 (c) 2 (d) 1.5 Ans:(b) 3</p>
19.	<p>Which of the following components are used for bias compensation in transistor circuit (a) resistors (b) rectifier diodes (c) thermistors (d) both (b) and (c) above Ans:(d) both (b) and (c) above</p>
20.	<p>The voltage divider biasing circuit is used in amplifiers quite often because it (a) limits the ac signal going to base (b) makes the operating point almost independent of β (c) reduces the dc base current (d) reduces the cost of the circuit Ans:(b) makes the operating point almost independent of β</p>
MULTIPLE CHOICE QUESTIONS-UNIT III	
1	<p>A field effect transistor (FET) a. Uses a forward bias p-n junction b. Uses a high concentration emitter junction c. Has a very high input resistance d. Depends on flow of minority carrier Ans:c. Has a very high input resistance</p>
2	<p>As compared to transistor amplifier JFET amplifier has a. Higher voltage gain, less input impedance b. Less voltage gain, less input impedance c. Less voltage gain, higher input impedance d. Higher voltage gain, higher input impedance Ans:c. Less voltage gain, higher input impedance</p>
3	<p>The best location for setting a Q-point on dc load line of an FET Amplifier is at a. Saturation point b. Cutoff point c. Mid- point</p>

	<p>d. None of these</p> <p>Ans:c. Mid- point</p>
4	<p>The pinch off voltage is the voltage</p> <p>a. At which gate source junction breaks down b. Which causes depletion regions to meet c. The voltage applied between drain & source d. Neither of these</p> <p>Ans:b. Which causes depletion regions to meet</p>
5	<p>If properly biased JFET acts as</p> <p>a. Current controlled current source b. Voltage controlled voltage source c. Voltage controlled current source d. Current controlled voltage source</p> <p>Ans:c. Voltage controlled current source</p>
6	<p>The voltage gain of a common source JFET amplifier depends upon its</p> <p>a. Transconductance (gm) b. Amplification factor (μ) c. External load resistance d. Both (a) and (c)</p> <p>Ans:d. Both (a) and (c)</p>
7	<p>A common gate amplifier has</p> <p>a. High input resistance and high output resistance b. Low input resistance and high output resistance c. Low input resistance and low output resistance d. High input resistance and low output resistance</p> <p>Ans:b. Low input resistance and high output resistance</p>
8	<p>Transconductance amplifier has</p> <p>a. High input impedance and low output impedance b. Low input impedance and high output impedance c. High input and output impedances d. Low input and output impedances</p> <p>Ans:a. High input impedance and low output impedance</p>
9	<p>A JFET is similar is operation to</p> <p>a. Diode b. Pentode c. Triode</p>

	<p>d. Tetrode</p> <p>Ans:b. Pentode</p>
10	<p>In a common source JFET amplifier the output voltage is</p> <p>a. 180° out of phase with input b. In phase with input c. 90° out of phase with input d. None of the above</p> <p>Ans: a. 180° out of phase with input</p>
11	<p>A common source (CS) amplifier has a voltage gain of</p> <p>a. $g_m r_d$ b. $g_m r_s$ c. $g_m r_s / (1+g_m r_s)$ d. $g_m r_d / (1+g_m r_d)$</p> <p>Ans:a. $g_m r_d$</p>
12	<p>A source follower has a voltage gain of</p> <p>a. $g_m r_d$ b. $g_m r_s$ c. $g_m r_s / (1+g_m r_s)$ d. $g_m r_d / (1+g_m r_d)$</p> <p>Ans:c. $g_m r_s / (1+g_m r_s)$</p>
13	<p>A Cascode amplifier has the advantage of</p> <p>a. Large voltage gain b. Low input capacitance c. Low input impedance d. Higher g_m</p> <p>Ans:b. Low input capacitance</p>
14	<p>If a JFET has $I_{DSS}=8\text{mA}$ and $V_P=4\text{V}$, then R_{DS} equals</p> <p>a. 200Ω b. 320Ω c. 500Ω d. $5\text{K}\Omega$</p> <p>Ans:c. 500Ω</p>
15	<p>In Enhancement n-channel MOSFET, an induced n type channel can be produced between the source and the drain if</p> <p>a. $V_{GS} = 0$ b. V_{GS} is positive</p>

	<p>c. VGS is negative d. None of these</p> <p>Ans: b. VGS is positive</p>
16	<p>The threshold voltage of an n-channel enhancement mode MOSFET is 0.5V when the device is biased at gate voltage of 3V, pinch off would occur at the drain voltage of</p> <p>a. 1.5V b. 2.5V c. 3.5V d. 4.5V</p> <p>Ans:b. 2.5V</p>
17	<p>The term IDSS is not used in</p> <p>a. D-MOSFET b. E-MOSFET c. JFET d. BJT</p> <p>Ans:b. E-MOSFET</p>
18	<p>The polarity of VGS for E only MOSFET is</p> <p>a. Positive b. Negative c. Zero d. Depends on P or N channel</p> <p>Ans:d. Depends on P or N channel</p>
19	<p>When an n-channel D-MOSFET has $I_D > I_{DSS}$ it</p> <p>a. Will be destroyed b. Is operating in depletion mode c. Is forward biased d. Is operating in the enhancement mode</p> <p>Ans:d. Is operating in the enhancement mode</p>
20	<p>A certain p-channel E-MOSFET has $V_{GS(th)} = -2V$. If $V_{GS} = 0V$, the drain current is</p> <p>a. 0 mA b. $I_D(on)$ c. Maximum d. I_{DSS}</p> <p>Ans:a. 0 mA</p>

MULTIPLE CHOICE QUESTIONS-UNIT IV	
1	<p>The frequency f_1 and f_2 from the below picture are respectively called</p>  <p>a) lower cut-off frequency and upper cut-off frequency b) upper cut-off frequency and lower cut-off frequency c) left frequency, right frequency d) there is no specific name</p> <p>Ans: a) lower cut-off frequency and upper cut-off frequency</p>
2	<p>Bandwidth of amplifier is</p> <p>a) Difference between upper cut-off frequency and lower cut-off frequency b) Sum of upper cut-off frequency and lower cut-off frequency c) Average of upper cut-off frequency and lower cut-off frequency d) Independent to cut off frequency</p> <p>Ans: a) Difference between upper cut-off frequency and lower cut-off frequency</p>
3	<p>At 3dB cut-off frequency the voltage gain will be</p> <p>a) 100% of maximum gain b) 70.7% of maximum gain c) 80.7% of maximum gain d) 47.5% of maximum gain</p> <p>Ans: b) 70.7% of maximum gain</p>
4	<p>At 3dB cut-off frequencies power will be</p> <p>a) Half of maximum value b) Quarter of maximum value c) 70.7% of maximum value d) Same as maximum value</p> <p>Ans: a) Half of maximum value</p>
5	<p>A voltage amplifier has a voltage gain of 100. What will be gain at 3dB cut-off frequencies</p> <p>a) 70.7 b) 80.7 c) 45.7 d) 50</p> <p>Ans: a) 70.7</p>

6	<p>What is the roll-off rate of single order filter</p> <p>a) 20dB/decade b) 5dB/octave c) 40dB/decade d) 10dB/octave</p> <p>Ans: a) 20dB/decade</p>
7	<p>-6dB is equivalent to _____ power gain</p> <p>a) 0.5 b) 0.25 c) 0.75 d) 0.8</p> <p>Ans: b) 0.25</p>
8	<p>Voltage gain of 1,00,000 is equivalent to</p> <p>a) 10dB b) 1000dB c) 100dB d) 50dB</p> <p>Ans: c) 100dB</p>
9	<p>If the output power from an audio amplifier is measured at 100W when the signal frequency is 1kHz, and 1W when the signal frequency is 10kHz. Calculate the dB change in power.</p> <p>a) -10dB b) -20dB c) -30dB d) 15dB</p> <p>Ans: b) -20dB</p>
10	<p>If an electronic system produces a 48mV output voltage when a 12mV signal is applied, calculate the decibel value of the systems output voltage gain.</p> <p>a) 6dB b) 10dB c) 20dB d) 4dB</p> <p>Ans: a) 6dB</p>
11	<p>The decibel gain of a cascaded system is the _____ of the decibel gains of each stage.</p> <p>a) sum b) difference c) product d)quotient</p> <p>Ans: a) Sum</p>
12	<p>The best frequency response is of coupling</p> <p>a) RC</p>

	<p>b) Transformer c) Direct d) None of the above Ans: c) Direct</p>
13	<p>The lower and upper cut off frequencies are also called frequencies a) Sideband b) Resonant c) Half-resonant d) Half-power Ans: d) Half power</p>
14	<p>A gain of 1,000,000 times in power is expressed by a) 30 db b) 60 db c) 120 db d) 600 db Ans: b) 60db</p>
15	<p>1 dB corresponds to change in power level a) 50% b) 35% c) 26% d) 22% Ans: c) 26%</p>
16	<p>In the input RC circuit of a single-stage BJT or FET amplifier, as the frequency _____, the capacitive reactance _____ and _____ of the input voltage appears across the output terminals. a) increases, decreases, more b) increases, decreases, less c) increases, increases, more d) decreases, decreases, less Ans: a. increases, decreases, more</p>
17	<p>In the low-frequency region, the _____ low-frequency cutoff determined by CS, CC, or CE will have the greatest impact on the network. a) highest b) average c) lowest d) None of the above Ans: a. highest</p>
18	<p>The Miller effect is meaningful in the _____ amplifier. a) inverting b) noninverting c) inverting/noninverting d) None of the above Ans: a. inverting</p>

19	<p>Which of the following elements is (are) important in determining the gain of the system in the high-frequency region?</p> <p>a) Interelectrode capacitances b) Wiring capacitances c) Miller effect capacitance d) All of the above</p> <p>Ans: d. All of the above</p>
20	<p>What is the range of the capacitor Cds?</p> <p>a) 0.01 to 0.1 pF b) 0.1 to 1 pF c) 0.1 to 1 nF d) 0.1 to 1 F</p> <p>Ans: b) 0.1 to 1 pF</p>
MULTIPLE CHOICE QUESTIONS-UNIT V	
1	<p>In a half wave rectifier, the load current flows for what part of the cycle.</p> <p>a. 00 b. 900 c. 1800 d. 3600</p> <p>Ans:c. 1800</p>
2	<p>In a full wave rectifier, if the input frequency is 50 Hz, then output frequency will be</p> <p>a. 50 Hz b. 75 Hz c. 100 Hz d. 200 Hz</p> <p>Ans:c. 100 Hz</p>
3	<p>In a center tap full wave rectifier, if V_m is the peak voltage between center tap and one end of the secondary, the maximum voltage coming across the reverse bias diode is</p> <p>a. V_m b. $2 V_m$ c. $V_m/2$ d. $V_m/\sqrt{2}$</p> <p>Ans:b. $2 V_m$</p>
4	<p>The maximum efficiency of full wave rectification is</p> <p>a. 40.6% b. 100% c. 81.2% d. 85.6%</p> <p>Ans:c. 81.2%</p>
5	<p>The basic purpose of filter is to</p> <p>a. minimizes variations in ac input signal</p>

	<p>b. suppresses harmonics in rectified output c. removes ripples from the rectified output d. stabilizes dc output voltage Ans:c. removes ripples from the rectified output</p>
6	<p>A half wave rectifier is equivalent to a. clamper circuit b. a clipper circuit c. a clamper circuit with negative bias d. a clamper circuit with positive bias Ans:b. a clipper circuit</p>
7	<p>In a LC filter, the ripple factor, a. Increases with the load current b. increases with the load resistance c. remains constant with the load current d. has the lowest value Ans:c. remains constant with the load current</p>
8	<p>The dc output polarity from a half-wave rectifier can be reversed by reversing a. the diode b. transformer primary c. transformer secondary d. both (b) and (c) Ans:a. the diode</p>
9	<p>Which of the following is not an essential element of a dc power supply? a. Rectifier b. Filter c. Voltage regulator d. Voltage amplifier Ans:d. Voltage amplifier</p>
10	<p>A Zener diode a. Is a battery b. Has a constant voltage in the breakdown region c. Has a barrier potential of 1 V d. Is forward biased Ans:b. Has a constant voltage in the breakdown region</p>
11	<p>In a loaded Zener regulator, which is the largest current? a. Series current b. Zener current c. Load current d. None of these Ans:c. Load current</p>
12	<p>If the Zener diode in a Zener regulator is connected with the wrong polarity, the load</p>

	<p>voltage will be closest to</p> <p>a. 0.7 V b. 10 V c. 14 V d. 18 V</p> <p>Ans:a. 0.7 V</p>
13	<p>The percentage voltage regulation of voltage supply providing 100V unloaded and 95V at full load is</p> <p>a. 5.3% b. 5.0% c. 0.53% d. None of the above</p> <p>Ans:a. 5.3%</p>
14	<p>Which of the following voltage regulator is preferred for providing large values of load Current?</p> <p>a. Zener diode shunt regulator b. Transistor series regulator c. Transistor shunt regulator d. None of the above</p> <p>Ans:b. Transistor series regulator</p>
15	<p>The main job of a voltage regulator is to provide a nearly output voltage.</p> <p>a. sinusoidal b. constant c. smooth d. fluctuating</p> <p>Ans:b. constant</p>
16	<p>A 10-V dc regulator power supply has a regulation of 0.005 per cent. Its output voltage will vary within an envelope ofmillivolt.</p> <p>a. ± 2.5 b. ± 0.5 c. ± 5 d. ± 0.05</p> <p>Ans:a. ± 2.5</p>
17	<p>An ideal voltage regulator has a voltage regulation of</p> <p>a. 1 b. 100 c. 50 d. 0</p> <p>Ans:d. 0</p>
18	<p>In a Zener diode shunt voltage regulator, the diode regulates so long as it is kept in</p>

	<p>.....condition.</p> <p>a. forward b. reverse c. loaded d. unloaded</p> <p>Ans: b. reverse</p>
19	<p>A transistor series voltage regulator is called emitter-follower regulator because the emitter of the pass transistor follows thevoltage.</p> <p>a. output b. input c. base d. collector</p> <p>Ans: c. base</p>
20	<p>The ripple factor of a bridge rectifier is</p> <p>a. 0.482 b. 0.812 c. 1.11 d. 1.21</p> <p>Ans:a. 0.482</p>

EC8352

SIGNALS AND SYSTEMS

L T P C

4 0 0 4

OBJECTIVES:

- To understand the basic properties of signal & systems
- To know the methods of characterization of LTI systems in time domain
- To analyze continuous time signals and system in the Fourier and Laplace domain
- To analyze discrete time signals and system in the Fourier and Z transform domain
-

UNIT I - CLASSIFICATION OF SIGNALS AND SYSTEMS

12

Standard signals- Step, Ramp, Pulse, Impulse, Real and complex exponentials and Sinusoids_ Classification of signals – Continuous time (CT) and Discrete Time (DT) signals, Periodic & Aperiodic signals, Deterministic & Random signals, Energy & Power signals - Classification of systems- CT systems and DT systems- – Linear & Nonlinear, Time-variant & Time-invariant, Causal & Non-causal, Stable & Unstable.

UNIT II - ANALYSIS OF CONTINUOUS TIME SIGNALS

12

Fourier series for periodic signals - Fourier Transform – properties- Laplace Transforms and properties

UNIT III - LINEAR TIME INVARIANT CONTINUOUS TIME SYSTEMS

12

Impulse response - convolution integrals- Differential Equation- Fourier and Laplace transforms in Analysis of CT systems - Systems connected in series / parallel.

UNIT IV ANALYSIS OF DISCRETE TIME SIGNALS

12

Baseband signal Sampling – Fourier Transform of discrete time signals (DTFT) – Properties of DTFT - Z Transform & Properties

UNIT V LINEAR TIME INVARIANT-DISCRETE TIME SYSTEMS

12

Impulse response – Difference equations-Convolution sum- Discrete Fourier Transform and Z Transform Analysis of Recursive & Non-Recursive systems-DT systems connected in series and parallel.

TOTAL: 60 PERIODS**OUTCOMES:**

After studying this course, the student should be able to:

To be able to determine if a given system is linear/causal/stable

Capable of determining the frequency components present in a deterministic signal

Capable of characterizing LTI systems in the time domain and frequency domain

To be able to compute the output of an LTI system in the time and frequency domains

TEXT BOOKS:

Allan V.Oppenheim, S.Wilsky and S.H.Nawab, —Signals and Systems, Pearson, 2015.(Unit 1-V)

REFERENCES

1 B. P. Lathi, —Principles of Linear Systems and Signals, Second Edition, Oxford, 2009.

2. R.E.Zeimer, W.H.Tranter and R.D.Fannin, —Signals & Systems - Continuous and Discrete, Pearson, 2007.

3. John Alan Stuller, —An Introduction to Signals and Systems, Thomson, 2007.

Subject Code: EC8352

Year/Semester: II /03

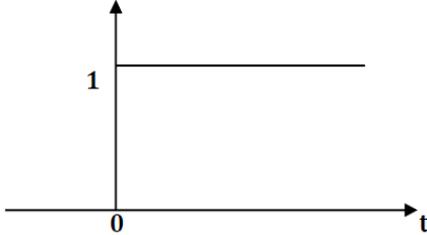
Subject Name: SIGNALS AND SYSTEMS

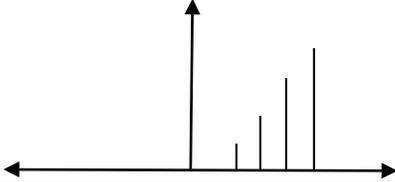
Subject Handler: Mrs.S.Mary Cynthia

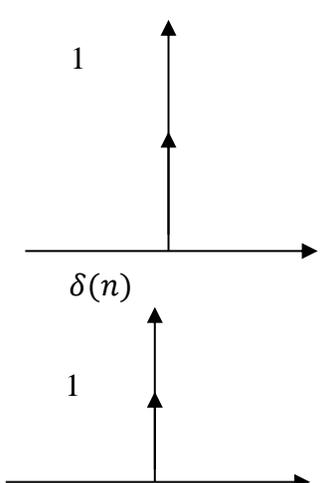
UNIT I- CLASSIFICATION OF SIGNALS AND SYSTEMS

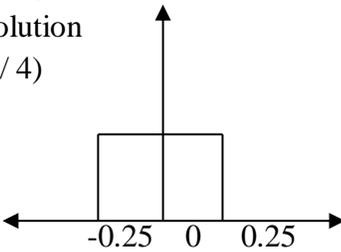
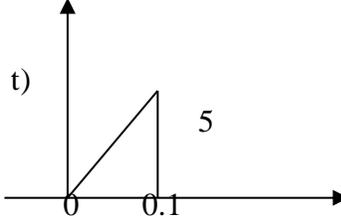
Standard signals- Step, Ramp, Pulse, Impulse, Real and complex exponentials and Sinusoids_ Classification of signals – Continuous time (CT) and Discrete Time (DT) signals, Periodic & Aperiodic signals, Deterministic & Random signals, Energy & Power signals - Classification of systems- CT systems and DT systems- – Linear & Nonlinear, Time-variant & Time-invariant, Causal & Non-causal, Stable & Unstable.

PART A

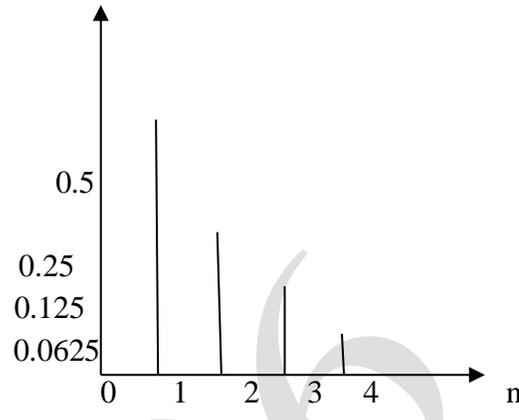
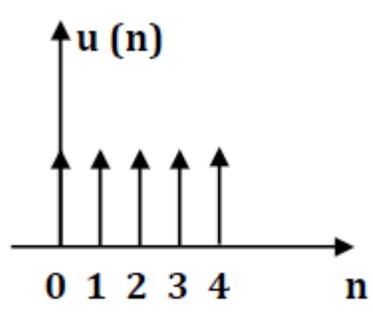
Q.No	Questions
1	<p>Find the even and odd part of the signal. (May 2019-BTL1)</p>  $x(t) = \begin{cases} 1 & \text{for } t \geq 0 \\ 0 & \text{otherwise} \end{cases}$ $x(-t) = \begin{cases} 1 & \text{for } -t \geq 0 \\ 0 & \text{otherwise} \end{cases}$
2	<p>Determine whether the given discrete time sequence is periodic or not. If the sequence is periodic, find the fundamental period. (May 2019)BTL3</p> $x(n) = \cos\left(\frac{n}{8}\right) \cos\left(\frac{\pi n}{8}\right)$ <p>Solution</p> <p>Given that, $x(n) = \cos\left(\frac{n}{8}\right) \cos\left(\frac{\pi n}{8}\right)$</p> <p>In DT signal periodic,</p> $N_1 = \frac{2\pi}{\omega} \text{ (m)}$ $\omega = \frac{1}{8}$ $N_1 = 16\pi \text{ (m)}$ $N_2 = \frac{2\pi}{\omega} \text{ (m)}$ $\omega = \frac{\pi}{8}$ $N_2 = 16 \text{ (m)}$ <p>The given sequence is non-periodic.</p>

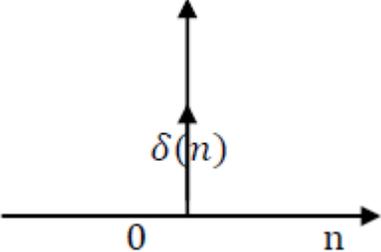
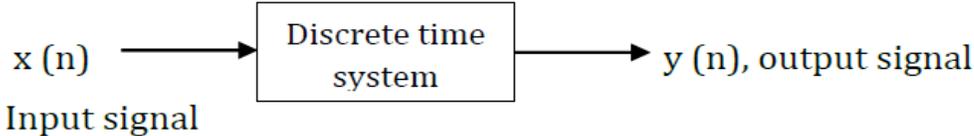
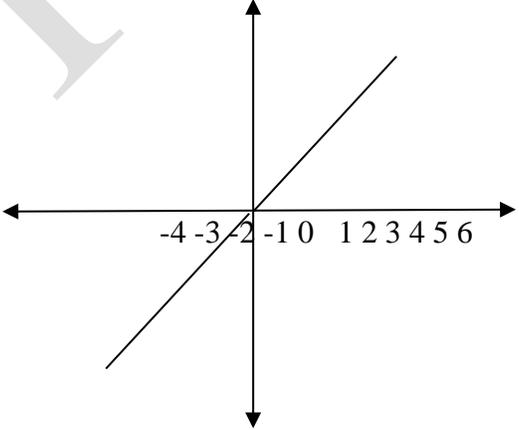
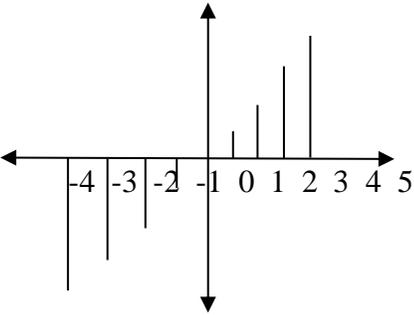
<p>3</p>	<p>Give the mathematical and graphical representations of a discrete time Ramp sequence. (Nov 2018)- BTL1</p> <p>Solution</p> <p>Ramp signal</p> $r(n) = n, n \geq 0, n < 0$ 
<p>4</p>	<p>Evaluate the following integral (Nov 2018)- BTL5</p> $\int_{-1}^1 (2t^2 + 3) \delta(t) dt$ <p>Solution</p> $\int_{-1}^1 (2t^2 + 3) \delta(t) dt$ <p>put</p> $t = 0$ $= 3$
<p>5</p>	<p>Determine if the signal x (n) given below is periodic. If yes give its fundamental Period. If not, state why it is aperiodic. x (n) = sin [(6πn/7)+1] (Nov 2017)- BTL2</p> <p>Solution</p> <p>In DT signal periodic,</p> $N = \frac{2\pi}{\omega} (m)$ $\omega = \frac{6\pi}{7}$ $N = \frac{2\pi}{6\pi/7} (m)$ $N = \frac{7}{3} \text{ samples.}$ <p>m = 3, N = 7</p> <p>Therefore, signal is periodic and fundamental time period = 7.</p>
<p>6</p>	<p>Check whether the following system is time invariant / time variant and also causal / non-causal. (Nov 2017)- BTL4</p> $y(t) = x(t/3)$ <p>Solution</p> $y(t) = x(t/3)$ <p>Delay the input by T</p> $y(t) = x[(t/3)-T] \dots \dots \dots 1$ <p>Delay the output by t = t - T</p> $y(t) = x [(t-T)/3] \dots \dots \dots 2$

	$1 \neq 2$ Therefore it is called Time Variant system. Causal or non-causal $y(t) = x(t/3)$ The output of the system depends on present input. Therefore it is called causal system.
7	Find the summation $x(n) = \sum_{n=-\infty}^{\infty} \delta(n-1) \sin 2n$ (May 2017)- BTL2 Solution Given that, $x(n) = \sum_{n=-\infty}^{\infty} \delta(n-1) \sin 2n$ $n = 1$ $x(n) = \sin 2$ $x(n) = 0.909$
8	Define linear system. (May 2017)- BTL1 A system of equations is a set or collection of equations that you deal with all together at once. Linear equations (ones that graph as straight lines) are simpler than non-linear equations, and the simplest linear system is one with two equations and two variables.
9	Give the mathematical and graphical representation of continuous time and discrete unit impulse functions. [Nov 2013, 2016] -BTL1 Continuous time unit impulse functions The impulse signal is a signal with infinite magnitude and zero duration, but with an area of A. mathematically, impulse signal is defined as, $\delta(t)$ $\delta(t) = \begin{cases} \infty, & t = 0 \\ 0, & t \neq 0 \end{cases}$ Discrete time impulse function Impulse signal can be defined as, $\delta(n) = \begin{cases} \infty, & n = 0 \\ 0, & n \neq 0 \end{cases}$ 
10	State the difference between causal and non-causal system [Nov 2013, 2016] – BTL2 Causal system A system is said to be causal system if its output depends on present and past inputs only and not on future inputs. Examples: The output of casual system depends on present and past inputs, it means $y(n)$ is a function of $x(n)$, $x(n-1)$, $x(n-2)$, $x(n-3)$...etc Non causal

	<p>An anti causal system is a hypothetical system with outputs and internal states that depend solely on future input values.</p>
<p>11</p>	<p>Sketch the following signals: Rect (t+1/ 4) and 5 ramp (0.1 t) [May 2016] –BTL3</p> <p>Solution</p> <p>Rect (t+1/ 4)</p>  
<p>12</p>	<p>Find the value of the integral $\int_{-\infty}^{\infty} e^{-2t} \delta(t + 2) dt$ [Nov 2015] –BTL5</p> <p>Solution</p> $\int_{-\infty}^{\infty} e^{-2t} \delta(t + 2) dt$ $= \int_{-\infty}^{\infty} e^{-2t} \delta(t - (-2)) dt$ $= e^{-2t} \text{ for } t = -2$ $= e^4$ $= 54.5982$
<p>13</p>	<p>Give the relation between continuous time unit impulse function $\delta(t)$. Step function $u(t)$ and ramp function $r(t)$. [Nov 2015] - BTL1</p> <p>The standard signals such as impulse, step, ramp and parabolic signals are related through integration and differentiation as follows,</p> <p>$\delta(t)$ impulse response $\xrightarrow{\text{integration}}$ $u(t)$ unit step $\xrightarrow{\text{integration}}$ t $\xrightarrow{\text{integration}}$ $\frac{t^2}{2}$</p> <p>$\delta(t)$ impulse response $\xrightarrow{\text{differentiation}}$ $u(t)$ unit step $\xrightarrow{\text{differentiation}}$ t $\xrightarrow{\text{differentiation}}$ $\frac{t^2}{2}$</p>
<p>14</p>	<p>Define a power signal. [May 2015] - BTL1</p> <p>The signals which have finite average power are called power signals. The periodic signals like sinusoidal and complex exponential signals will have constant power so periodic signals are power signals,</p> <p>The average power of a continuous time signal $x(t)$ is defined as,</p> $P = \lim_{T \rightarrow \infty} \frac{1}{2T} \int_{-T}^T x(t) ^2 dt$

15	<p>How the impulse response of a discrete time system useful in determining its stability and causality? [May 2015] - BTL4</p> <p>Stability The condition for stability of an LTI system is, $\sum_{-\infty}^{\infty} h(n) < \infty$ An LTI system is stable if the impulse response is absolutely summable.</p> <p>Causality: A system is said to be causal if the output of the system at any time n depends only on the present input, past inputs and past outputs but does not depend on the future inputs and outputs. If the system output at any time n depends on future or outputs then the system is called non causal system. The causality refers to a system that is realizable in real time.</p>
16	<p>State two properties of unit impulse function [Nov 2014] –BTL1</p> <p>Property 1 $\int_{-\infty}^{\infty} \delta(t) dt = 1$</p> <p>Property 2 $\int_{-\infty}^{\infty} x(t)\delta(t) dt = x(0)$</p> <p>Property 3 $\int_{-\infty}^{\infty} x(t)\delta(t - t_0) dt = x(t_0)$</p>
17	<p>Draw the following signals: [Nov 2014]–BTL2</p> <p>u(t) – u(t-10) b. (1/2)ⁿ u(n-1)</p> <p>Solution</p> <p>Given that, $u(t) = 1 ; t \geq 0$ $u(t-10) = 1 ; t \geq 10$</p> <p>The first plot shows the unit step function $u(t)$, which is 0 for $t < 0$ and 1 for $t \geq 0$. The second plot shows the time-shifted unit step function $u(t-10)$, which is 0 for $t < 10$ and 1 for $t \geq 10$. The third plot shows the difference signal $u(t) - u(t-10)$, which is 1 for $0 \leq t < 10$ and 0 elsewhere.</p>

	<p>$(1/2)^n u(n-1)$ $x(n) = (1/2)^n u(n-1)$</p> <p>Solution</p> <p>Given that, $u(n-1) = 1 ; n \geq 0$ $= 0 ; n < 0$</p> <p>$x(n) = (1/2)^n u(n-1) = (1/2)^n ; n \geq 1$</p> <p>$n=1; (1/2)^n = (1/2)^1 = 0.5$ $n= 2; (1/2)^n = (1/2)^2 = 0.25$ $n= 3; (1/2)^n = (1/2)^3 = 0.125$ $n= 4; (1/2)^n = (1/2)^4 = 0.0625$</p> 
<p>18</p>	<p>Define a signal and system. [May 2015] -BTL1</p> <p>Signal Any physical phenomenon that conveys or carries some information can be called a signal. A signal is defined as any physical quantity that varies with one or more independent variables.</p> <p>System Any process that exhibits cause and effect relation can be called a system. A system will have an input and an output signal.</p>
<p>19.</p>	<p>What is meant by stability of a system? [May 2015] –BTL1</p> <p>The condition for stability of an LTI system is, $\sum_{-\infty}^{\infty} h(n) < \infty$</p> <p>An LTI system is stable if the impulse response is absolutely summable.</p>  <p>It can be defined as, $u(n) = \begin{cases} 1, & n \geq 0 \\ 0, & n < 0 \end{cases}$</p> <p>Impulse signal Impulse signal can be defined as, $\delta(n) = \begin{cases} 1, & n = 0 \\ 0, & n \neq 0 \end{cases}$</p>

	
<p>20.</p>	<p>Define DT system. (Nov 2015) -BTL1 A system is defined as a physical device that performs an operation on a signal. A discrete time system is a device or algorithm that operates on a discrete time input signal $x(n)$, to produce another discrete time signal $y(n)$ called the output signal.</p> 
<p>21.</p>	<p>Sketch the following signals $x(t) = 2t$ for all t b. $x(n) = 2n - 3$ for all n [May 2014]- BTL2</p> <p>Solution $x(t) = 2t$ for all t Given that, $x(t) = 2t$ $t = -3; x(-3) = 2 * (-3) = -6$ $t = -2; x(-2) = 2 * (-2) = -4$ $t = -1; x(-1) = 2 * (-1) = -2$ $t = 0; x(0) = 2 * (0) = 0$ $t = 1; x(1) = 2 * (1) = 2$ $t = 2; x(2) = 2 * (2) = 4$ $t = 3; x(3) = 2 * (3) = 6$</p>  <p>$x(n) = 2n - 3$ for all n Given that, $x(n) = 2n - 3$ $n = -2; x(-2) = 2 * (-2) - 3 = -7$ $n = -1; x(-1) = 2 * (-1) - 3 = -5$ $n = 0; x(0) = 2 * (0) - 3 = -3$ $n = 1; x(1) = 2 * (1) - 3 = -1$ $n = 2; x(2) = 2 * (2) - 3 = 1$ $n = 3; x(3) = 2 * (3) - 3 = 3$</p> 
<p>22.</p>	<p>Given $x(n) = [1, -4, 3, 1, 5, 2]$. Represents $x(n)$ in terms of weighted shifted impulse functions. [May 2014] -BTL3 Given that, $x(n) = [1, -4, 3, 1, 5, 2]$</p>

	$x(0) = 1$ $x(1) = -4$ $x(2) = 3$ $x(3) = 1$ $x(4) = 5$ $x(5) = 2$ The shifted impulse, $\delta(n-k) = 1$; for $n = k$ $= 0$; for $n \neq k$ Therefore, if we multiply $x(n)$ by $\delta(n-k)$ then it selects only k^{th} sample of $x(n)$. The weighted shifted impulse function is, $x(n) = \delta(n) - 4\delta(n-1) + 3\delta(n-2) + \delta(n-3) + 5\delta(n-4) + 2\delta(n-5)$.
23	What is the condition for a system to be LTI system? [Nov 2013] -BTL1 <div style="text-align: center;"> </div> <p>The operation performed by a continuous time system on input to produce output or response can be expressed as, Response, $y(t) = H\{x(t)\}$ Where, H denotes the system operation also called system operator. When a continuous time system satisfies the properties of linearity and time invariance then it is called LTI CT system.</p>
24	Check whether the discrete time signal $\sin 3n$ periodic [May 2013, 2016] -BTL4 Given that, $x(n) = \sin 3n$ $3N = 2\pi M$ $= \frac{2\pi M}{3}$ Here N cannot be an integer for any integer value of M and so $x(n)$ will not be periodic
25	Determine whether the following signal is energy or power signal and calculate the energy or power $x(t) = e^{-2t}u(t)$ [Nov 2012] - BTL4 Given that, $x(t) = e^{-2t}u(t)$ $x(t) = e^{-2t}u(t)$; for all t $x(t) = e^{-2t}u(t)$; for $t \geq 0$ $\int_{-T}^T x(t) ^2 dt = \int_0^T e^{-2t} ^2 dt = \int_0^T (e^{-2t})^2 dt = \int_0^T (e^{-4t}) dt$ $= \left[\frac{e^{-4t}}{-4} \right] - \frac{e^0}{-4} = \left[\frac{1}{4} \right] - \frac{e^{-4T}}{4}$ Energy $E = \lim_{T \rightarrow \infty} \int_{-T}^T x(t) ^2 dt$ $= \lim_{T \rightarrow \infty} \left[\frac{1}{4} \right] - \frac{e^{-4T}}{4}$ $= \left[\frac{1}{4} \right] - \frac{e^{-4\infty}}{4}$ $E = \frac{1}{4}$ joules Power

	$P = \lim_{t \rightarrow \infty} \frac{1}{2T} \int_{-T}^T x(t) ^2 dt$ $P = \lim_{t \rightarrow \infty} \frac{1}{2T} \left[\frac{1}{4} - \frac{e^{-4T}}{4} \right]$ $P = 0. \text{ The given signal is an energy signal.}$
26	<p>Verify whether the system described by the equation is linear and Time invariant $y(t) = x(t)^2$ [May 2012] –BTL4</p> <p>Solution Linear: The system is linear since an output is direct function of input. Time invariant: The system is time variant since time parameter is squared in the given system function equation.</p>
27	<p>Find the fundamental period of the given signal $x(n) = \sin\left(\frac{6\pi n}{7} + 1\right)$ [May 2012] - BTL3</p> <p>In DT signal periodic, $N = \frac{2\pi}{\omega} \text{ (m)}$ $\omega = \frac{6\pi}{7}$ $N = \frac{2\pi}{6\pi/7} \text{ (m)}$ $N = \frac{7}{3} \text{ samples.}$</p>
	PART B
Q.No	Questions
1	<p>Find out whether the following signals are periodic or not. If periodic find the period $x(t) = 2 \cos(10t + 1) - \sin(4t - 1)$ and $x(n) = \cos(0.1\pi n)$ (7M)[May 2017] -BTL4 Answer: Page 57 - Ramesh babu</p> <p>Solution Given that, $x(t) = 2 \cos(10t + 1) - \sin(4t - 1)$ Let T_1 be the periodicity of $x_1(t)$. on comparing $x_1(t)$ with standard form, Find Time period T_1 $x_1(t) = 2 \cos(10t + 1)$ $2\pi F_{o1} = 10$ $F_{o1} = 5/\pi$ period $T_1 = \frac{1}{F_{o1}} = \frac{5}{\pi}$ Find Time period T_2 $x_2(t) = \sin(4t - 1)$ $2\pi F_{o2} = 4$</p>

	$F_{02} = 2/\pi \quad \text{period } T_2 = \frac{1}{F_{01}} = \frac{\pi}{2}$ $\frac{T_1}{T_2} = T_1 * \frac{1}{T_2} = \frac{5}{\pi} \frac{2}{\pi} \quad (4M)$ <p>Since $x_1(t)$ and $x_2(t)$ are periodic, and the ratio of T_1 and T_2 is a irrational number, the signal $x(t)$ is Aperiodic.</p> <p>$x(n) = \cos(0.1\pi n)$</p> <p>In DT signal periodic,</p> $N = \frac{2\pi}{\omega} \text{ (m)}$ $\omega = 0.1\pi$ $N = \frac{2\pi}{0.1\pi} \text{ (m)}$ $N = 20 \text{ samples.} \quad (3M)$ <p>Hence $x(n)$ is a periodic with fundamental period of 20 samples.</p>
2	<p>Find out whether the following signals are energy or power signal or neither power nor energy. Determine power or energy as the case may be for the signal.</p> <p>$x(t) = u(t) + 5u(t-1) - 2u(t-2)$ (6M)[May 2017] -BTL-4</p> <p>Answer: Page 73 - Ramesh babu(Similar Type)</p> <p>Energy and power signals</p> <p>Energy signal</p> <p>The signals which have finite energy are called energy signal. The nonperiodic signals defined over finite interval will have constant energy and so nonperiodic signals defined over finite interval are energy signals.</p> <p>The energy E of a continuous time signal $x(t)$ is defined as,</p> $E = \lim_{T \rightarrow \infty} \int_{-T}^T x(t) ^2 dt \quad (3M)$ <p>Power signals</p> <p>The signals which have finite average power are called power signals. The periodic signals like sinusoidal and complex exponential signals will have constant power so periodic signals are power signals,</p> <p>The average power of a continuous time signal $x(t)$ is defined as,</p> $P = \lim_{T \rightarrow \infty} \frac{1}{2T} \int_{-T}^T x(t) ^2 dt \quad (3M)$ <p>Note: for energy signals, the energy will be finite or constant and average power will be Zero.</p> <p>For power signals the average power is finite or constant and energy will be infinite.</p>
3	<p>Determine the properties via linearity, causality, time invariance, dynamicity of the given systems.</p> $y(t) = \frac{d^2y}{dt^2} + 3t \frac{dy}{dt} + y(t) = x(t)$ <p>$y_1(n) = x(n^2) + x(n)$</p> <p>$y_1(n) = \log x(n)$ (13M)[May 2017], [Nov 2014]-BTL3</p>

Answer: Page 112 - Ramesh babu

Solution

Given that, $y(t) = \frac{d^2y}{dt^2} + 3t \frac{dy}{dt} + y(t) = x(t)$

Linearity

Consider two signals, $x_1(t)$ and $x_2(t)$.

Let $y_1(t)$ and $y_2(t)$ be the response of the system for inputs $x_1(t)$ and $x_2(t)$ respectively.

$$y_1(t) = \frac{d^2y_1}{dt^2} + 3t \frac{dy_1}{dt} + y_1(t) = x_1(t)$$

$$y_2(t) = \frac{d^2y_2}{dt^2} + 3t \frac{dy_2}{dt} + y_2(t) = x_2(t)$$

$$x_3(t) = a x_1(t) + b x_2(t)$$

Let, $y_3(t)$ be the response the system for input $x_3(t)$.

Therefore,

$$y_3(t) = \frac{d^2y_3}{dt^2} + 3t \frac{dy_3}{dt} + y_3(t) = x_3(t)$$

$$y_3(t) = \frac{d}{dt} [a x_1(t) + b x_2(t)]$$

$$y_3(t) = a y_1(t) + b y_2(t)$$

The given system is linear.

Causality

$$y(t) = \frac{d^2y}{dt^2} + 3t \frac{dy}{dt} + y(t) = x(t)$$

In above equation, for any value of t , the $x(t)$ is present input and past input.

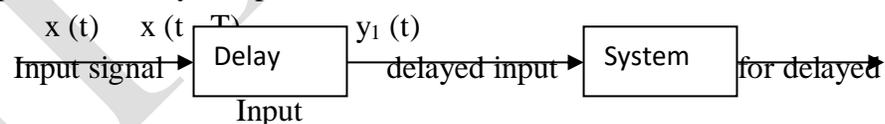
Therefore any value of t depends on present and past input. Hence the system is causal.

Dynamic

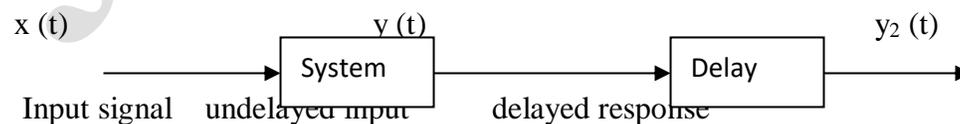
The output of the system depends on differentiation of the input which in turn depends on past and present input. Therefore, the given system is dynamic system.

Time invariance

Response for delayed input



Delayed response



Hence $y_1(t) = y_2(t)$, therefore the system is time invariant

Stability

The given system is LTI system and the stability can be determined from impulse response. Hence the system is stable. (5M)

Result

Linear

Causal

Dynamic

Time invariant

Stable

Given that, $y(n) = x(n^2) + x(n)$

Causality

When $n = 0$; $y(0) = x(0^2) + x(0)$; the response at $n = 0$; $y(0)$ depends on the present input $x(0)$

When $n = 1$; $y(1) = x(1) + x(1)$; the response at $n = 1$; $y(1)$ depends on the present input $x(1)$

When $n = 2$; $y(2) = x(4) + x(2)$; the response at $n = 2$; $y(2)$ depends on the present input $x(2)$ and feature input $x(4)$

From above analysis for any value of n , the system output depends on present and feature inputs. Hence the system is non-causal.

Linearity

Consider two signals, $x_1(n)$ and $x_2(n)$.

Let $y_1(n)$ and $y_2(n)$ be the response of the system for inputs $x_1(n)$ and $x_2(n)$ respectively.

$$y_1(n) = x_1(n^2) + x_1(n)$$

$$y_2(n) = x_2(n^2) + x_2(n)$$

$$x_3(n) = a x_1(n^2) + a x_1(n) + b x_2(n^2) + b x_2(n)$$

Let, $y_3(n)$ be the response the system for input $x_3(n)$.

$$y_3(n) = a x_1(n) + b x_2(n)$$

Therefore,

$$y_3(n) = a x_1(n^2) + a x_1(n) + b x_2(n^2) + b x_2(n)$$

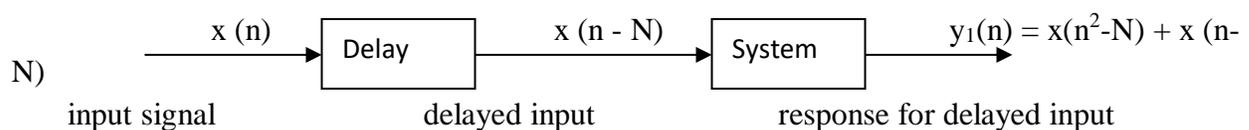
The condition to be satisfied for linearity is,

$$y_3(n) = a y_1(n) + b y_2(n)$$

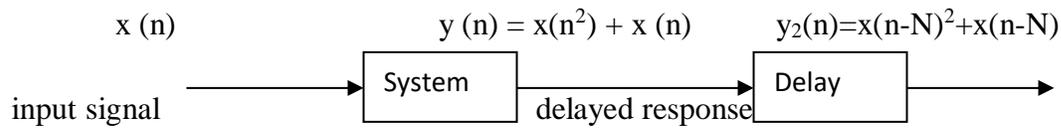
The given system is linear.

Time invariance

Response for delayed input



Delayed response



Hence $y_1(n) \neq y_2(n)$, therefore the system is time variant.

Stability

The given system is an LTI system, so the stability can be determined from impulse response. The system is stable.

Result

(4M)

Non- Causal

Linear

Time variant

Stable

Given that $y(n) = [\log x(n)]$

Linearity

Consider two signals, $x_1(n)$ and $x_2(n)$.

Let $y_1(n)$ and $y_2(n)$ be the response of the system for inputs $x_1(n)$ and $x_2(n)$ respectively.

$$y_1(n) = \log x_1(n)$$

$$y_2(n) = \log x_2(n)$$

$$x_3(n) = a \log x_1(n) + b \log x_2(n)$$

Let, $y_3(n)$ be the response the system for input $x_3(n)$.

Therefore,

$$y_3(n) = \log x_3(n)$$

$$y_3(n) = a \log x_1(n) + b \log x_2(n)$$

$$y_3(n) = \log [a x_1(n) + b x_2(n)]$$

The given system is non linear.

Causality

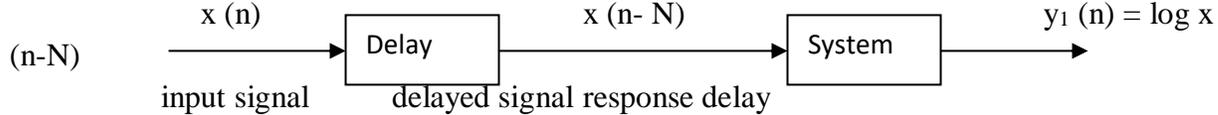
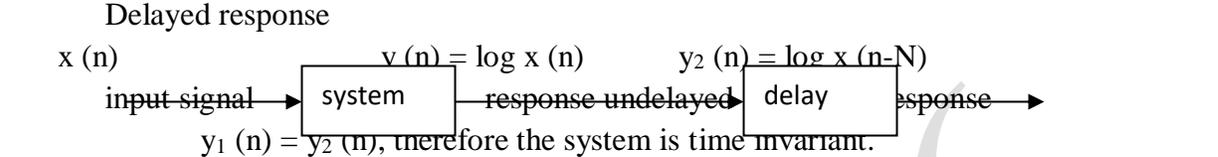
When $n = 0$; $y(0) = \log x(0)$ the response at $n = 0$, $y(0)$ depends on the present Input $x(0)$.

When $n = 1$; $y(1) = \log x(1)$ the response at $n = 1$, $y(1)$ depends on the present input $x(0)$.

When $n = 2$; $y(2) = \log x(2)$ the response at $n = 2$, $y(2)$ depends on the present input $x(2)$.

From above analysis the response for any value of n depends on the present input. Hence the system is causal.

Time invariance

	<p>Response for delayed input</p>  <p>Delayed response</p>  <p>Stability</p> <p>The given system is a non linear system, and so the test for stability should be performed for specific inputs.</p> <p>Case i: $x(n)$ tends to ∞ or zero, as n tends to infinity. In this case, $y(n) = \log x(n)$ will be infinity as n tends to infinity and so the system is unstable.</p> <p>Case ii: $x(n)$ tends to constant as n tends to infinity. Then, $y(n) = \log x(n)$ will be finite as n tends to infinity and so the system is stable.</p> <p>Result (4M)</p> <p>Non linear</p> <p>Causal</p> <p>Time invariant</p>
<p>4</p>	<p>Sketch the following signals</p> <p>$u(-t+2)$</p> <p>$r(-t+3)$</p> <p>$2\delta(n+2) + \delta(n) - 2\delta(n-1) + 3\delta(n-3)$</p> <p>$u(n+2) u(-n+3)$ (13 marks)[Nov 2016] -BTL2</p> <p>Answer: Page 44 - Ramesh babu</p> <p>Solution</p> <p>Draw $u(-t+2)$ (3M)</p> <p>Draw $r(-t+3)$ (3M)</p> <p>Draw $2\delta(n+2) + \delta(n) - 2\delta(n-1) + 3\delta(n-3)$ (7M)</p>
<p>5</p>	<p>Find whether the following signals are periodic or aperiodic.</p> <p>If periodic find the fundamental period and fundamental frequency,</p> <p>$x_1(n) = \sin 2\pi t + \cos \pi t$</p> <p>$x_2(n) = \sin \frac{n\pi}{3} \cos \frac{n\pi}{5}$ (8M) [May 2016] -BTL4</p> <p>Answer: Page 57 - Ramesh babu</p> <p>Solution</p>

	<p>Given that, $x_1(t) = \sin 2\pi t + \cos \pi t$ Let T_1 be the periodicity of $x_1(t)$. on comparing $x_1(t)$ with standard form, Find Time period T_1 $x_1(t) = \sin 2\pi t$ $2\pi F_{o1} = 2\pi$ $F_{o1} = 1$ period $T_1 = \frac{1}{F_{o1}} = 1$ Find Time period T_2 $x_2(t) = \cos \pi t$ $2\pi F_{o2} = \pi$ $F_{o2} = 1/2$ period $T_2 = \frac{1}{F_{o2}} = 2$ $\frac{T_1}{T_2} = T_1 * \frac{1}{T_2} = \frac{1}{2}$ Since $x_1(t)$ and $x_2(t)$ are periodic, and the ratio of T_1 and T_2 is a rational number, the signal $x(t)$ is periodic. (4M) Given that, $x_2(n) = \sin \frac{n\pi}{3} \cos \frac{n\pi}{5}$ In DT signal periodic, $N_1 = \frac{2\pi}{\omega} (m)$ $\omega = \frac{\pi}{3}$ $N_1 = \frac{2\pi}{\pi/3} (m)$ $N_1 = 6 (m)$ samples. If $m = 1$ $N_1 = 6$ samples. Hence the $x_1(n)$ is periodic signals. Fundamental period of 4 samples. In DT signal periodic, $N_2 = \frac{2\pi}{\omega} (m)$ $\omega = \frac{\pi}{5}$ $N_2 = \frac{2\pi}{\pi/5} (m)$ $N_2 = 4 (m)$ samples. If $m = 1$ $N_2 = 4$ samples. Hence the $x_2(n)$ is periodic signals. (4M) From above analysis $x(n)$ is sum of periodic and periodic signals. Therefore, $x(n)$ will be periodic.</p>
6	<p>Given $x(n) = \{1, 4, 3, -1, 2\}$. Plot the following signals, (16M)[Nov 2015] -BTL2 $x(-n-1)$ $x(-n/2)$ $x(-2n + 1)$</p>

$$x\left(-\frac{n}{2} + 2\right)$$

Answer: Page 81 - Ramesh babu(Similar Type)

Solution

$$x(n) = \{1, 4, 3, -1, 2\}$$

$$x(-2) = 1, x(-1) = 4, x(0) = 3, x(1) = -1, x(2) = 2$$

$$x(-n-1)$$

Given that, $x(n) = x(-n-1)$

$$n = -3 ; x_1(-3) = x(-(-3)-1) = x(2) = 2$$

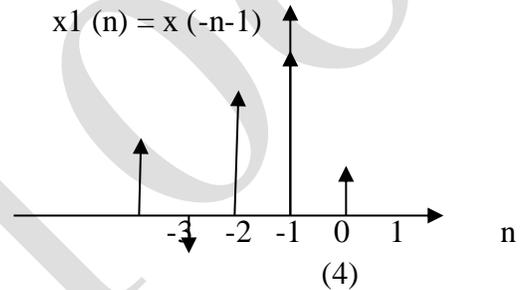
$$n = -2 ; x_1(-2) = x(-(-2)-1) = x(1) = -1$$

$$n = -1 ; x_1(-1) = x(-(-1)-1) = x(0) = 3$$

$$n = 0 ; x_1(0) = x(-(-0)-1) = x(-1) = 4$$

$$n = 1 ; x_1(1) = x(-(-1)-1) = x(-2) = 1$$

$$x_1(n) = x(-n-1) = \{2, -1, 3, 4, 1\}$$



$$x(-n/2)$$

$$n = -4 ; x_2(-4) = x(-(-4/2)) = x(2) = 2$$

$$n = -3 ; x_2(-3) = x(-(-3/2)) = 0$$

$$n = -2 ; x_2(-2) = x(-(-2/2)) = x(1) = -1$$

$$n = -1 ; x_2(-1) = x(-(-1/2)) = x(0.5) = 0$$

$$n = -0 ; x_2(0) = x(-(-0/2)) = x(0) = 3$$

$$n = 1 ; x_2(1) = x(-(-1/2)) = x(-0.5) = 0$$

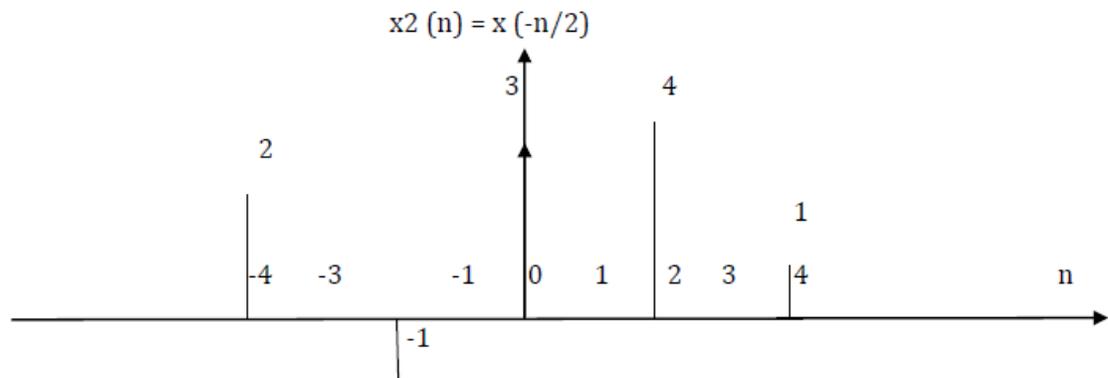
$$n = 2 ; x_2(2) = x(-(-2/2)) = x(-1) = 4$$

$$n = 3 ; x_2(3) = x(-(-3/2)) = x(-1.5) = 0$$

$$n = 4 ; x_2(4) = x(-(-4/2)) = x(-2) = 1$$

$$x_2(n) = x(-n/2) = \{2, 0, -1, 0, 3, 0, 4, 0, 1\}$$

(4M)



$$x(-2n+1)$$

$$n = -1 ; x^3(-1) = x(-2(-1)+1) = x(3) = 0$$

$$n = 0 ; x^3(-1) = x(-2(0)+1) = x(1) = -1$$

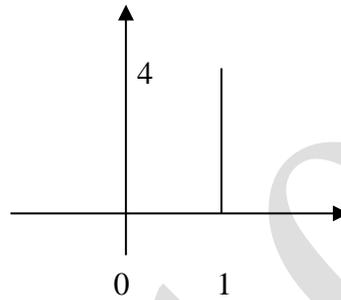
$$n = 1 ; x^3(-1) = x(-2(1)+1) = x(-1) = 4$$

$$n = 2 ; x^3(-1) = x(-2(2)+1) = x(-3) = 0$$

$$x^3(n) = x(-2n+1) = \{-1, 4\}$$

(4M)

$$x^3(n) = x(-2n+1)$$



$$\text{iv. } x\left(-\frac{n}{2} + 2\right)$$

$$n = 0 ; x^4(0) = x\left(-\frac{0}{2} + 2\right) = x(2) = 2$$

$$n = 1 ; x^4(1) = x\left(-\frac{1}{2} + 2\right) = x\left(\frac{3}{2}\right) = 0$$

$$n = 2 ; x^4(2) = x\left(-\frac{2}{2} + 2\right) = x(1) = -1$$

$$n = 3 ; x^4(3) = x\left(-\frac{3}{2} + 2\right) = x\left(\frac{1}{2}\right) = 0$$

$$n = 4 ; x^4(4) = x\left(-\frac{4}{2} + 2\right) = x(0) = 3$$

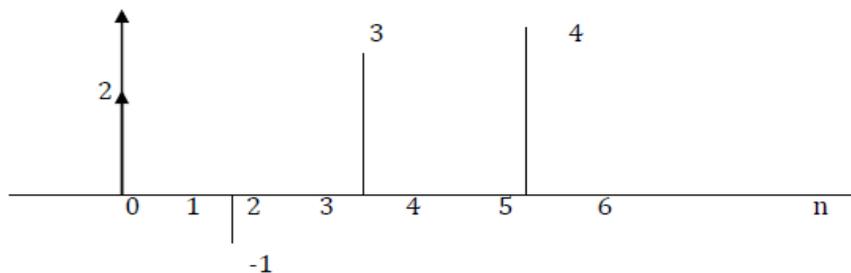
$$n = 5 ; x^4(5) = x\left(-\frac{5}{2} + 2\right) = x\left(-\frac{1}{2}\right) = 0$$

$$n = 6 ; x^4(6) = x\left(-\frac{6}{2} + 2\right) = x(-1) = 4$$

$$x^4(n) = x\left(-\frac{n}{2} + 2\right) = \{2, 0, -1, 0, 3, 0, 4\}$$

(4M)

$$x^4(n) = x\left(-\frac{n}{2} + 2\right)$$



Sketch the following signals.

$[u(t-2) + u(t-4)]$

$[(t-4)u(t-2) - u(t-4)]$

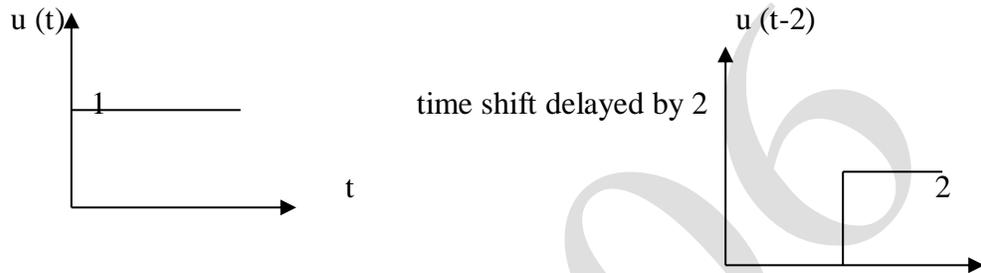
(6M)[May 2015] -BTL2

Answer: Page 81- Ramesh babu(Similar Type)

Solution

Given that, $[u(t-2) + u(t-4)]$

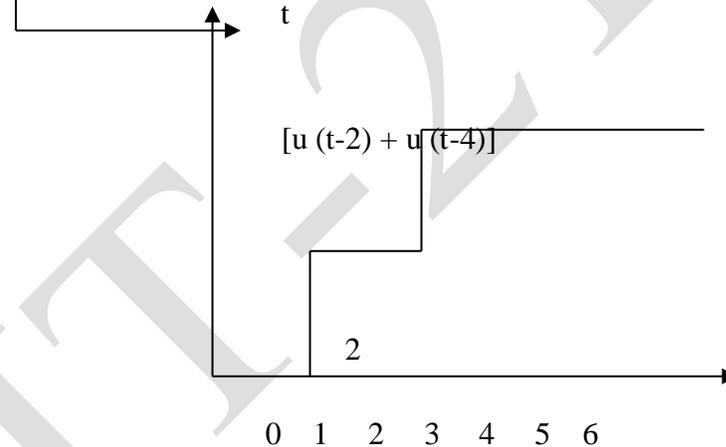
Step 1: step 2:



Step 3:



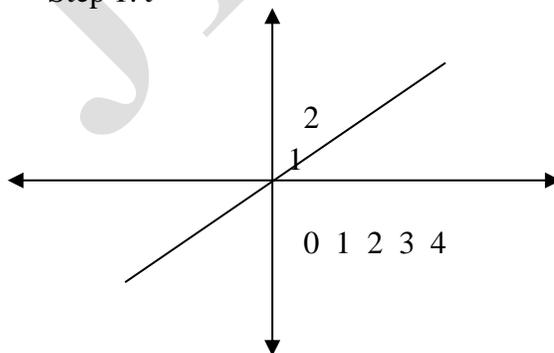
Step 4:



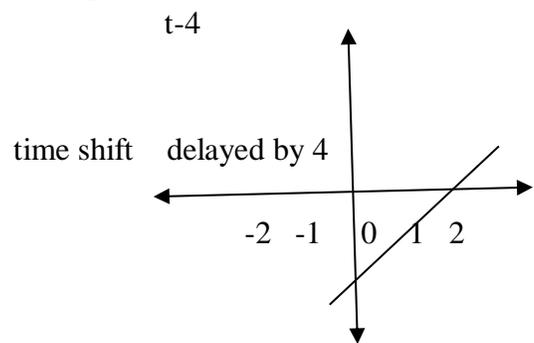
(3M)

$[(t-4)u(t-2) - u(t-4)]$

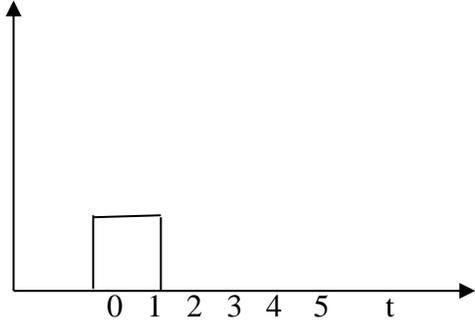
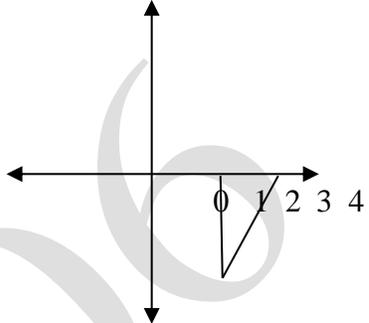
Step 1: t



step 2



7

	<p>Step 3: $u(t-2) - u(t-4)$</p>  <p style="text-align: right;">step 4 $[(t-4) u(t-2) - u(t-4)]$</p> <p style="text-align: right;">(3M)</p> 
<p style="text-align: center;">8</p>	<p>Give an account for the classification of signals in detail. Or How the signals are classified? Explain. (10M)[May 2015] -BTL1</p> <p>Answer: Page 53-80 - Ramesh babu</p> <p>The continuous time signals are classified depending on their characteristics.</p> <ul style="list-style-type: none"> Deterministic and non-deterministic signals Periodic and A periodic signal Symmetric and asymmetric signals Energy and power signals Causal and noncausal signal <p>Deterministic and non-deterministic signals (2M)</p> <p>Deterministic signal</p> <p>The signal that can be completely specified by a mathematical equation is called a deterministic signal. The step, ramp, exponential and sinusoidal signals are examples of deterministic signals.</p> <p>Examples: $x(t) = At$ $x(t) = X_m \sin wt$</p> <p>Non-deterministic signal</p> <p>The signal whose characteristics are random in nature is called a non-deterministic signal. The noise signals from various sources like electronic amplifier, oscillator, and radio receiver are the examples of random signals. (2M)</p> <p>Periodic and A periodic signal</p> <p>A periodic signal will have a definite pattern that repeats again and again over a certain period of time. Therefore, the signal which satisfies the condition, $x(t + T) = x(t)$ is called a periodic signal.</p>

A signal which does not satisfy the condition, $x(t + T) = x(t)$ is called an Aperiodic or non-periodic signal.

In periodic signals, the term T is called the fundamental time period of the signal. Hence, inverse of T is called the fundamental frequency, F_0 in Hz, and $2\pi F_0 = \Omega_0$ is called the fundamental angular frequency in rad / sec.

The sinusoidal signals and complex exponential signals are always periodic with a periodicity of T ,

$$\text{Where, } T = \frac{1}{F_0} = \frac{2\pi}{\Omega_0}$$

Symmetric and asymmetric signals

Odd signal or Symmetric

The signals may exhibit symmetry or antisymmetry with respect to $t = 0$.

When a signal exhibits antisymmetry with respect to $t = 0$, then it is called an odd signal.

Therefore, the odd signal satisfies the condition, $x(-t) = -x(t)$.

$$x(t) = \frac{x(t) - x(-t)}{2}$$

Even signal or asymmetric signals

When a signal exhibits symmetry with respect to $t = 0$, then it is called an even signal.

Therefore, the even signal satisfies the condition, $x(-t) = x(t)$.

$$x(t) = \frac{x(t) + x(-t)}{2}$$

Energy and power signals

(4M)

Energy signal

The signals which have finite energy are called energy signal. The nonperiodic signals defined over finite interval will have constant energy and so nonperiodic signals defined over finite interval are energy signals.

The energy E of a continuous time signal $x(t)$ is defined as,

$$E = \lim_{t \rightarrow \infty} \int_{-T}^T |x(t)|^2 dt$$

Power signals

The signals which have finite average power are called power signals. The periodic signals like sinusoidal and complex exponential signals will have constant power so periodic signals are power signals,

The average power of a continuous time signal $x(t)$ is defined as,

$$P = \lim_{t \rightarrow \infty} \frac{1}{2T} \int_{-T}^T |x(t)|^2 dt$$

Note: for energy signals, the energy will be finite or constant and average power will be Zero.

For power signals the average power is finite or constant and energy will be infinite.

Causal and noncausal signal

(2M)

A signal is said to be causal, if it is defined for $t \geq 0$.

	<p>Therefore if $x(t)$ is causal, then $x(t) = 0$, for $t < 0$.</p> <p>A signal is said to be noncausal, if it is defined for either $t \leq 0$, or both $t \leq 0$ and $t > 0$.</p> <p>Therefore if $x(t)$ is noncausal, then $x(t) \neq 0$, for $t < 0$.</p> <p>When a noncausal signal is defined only for $t \leq 0$, it is called anticausal signal.</p>
9	<p>Check if $x(t) = 4 \cos(3\pi t + \frac{\pi}{4}) + 2 \cos(4\pi t)$ is periodic (6M)[May2015] -BTL4</p> <p>Answer: Page 57 - Ramesh babu(Similar Type)</p> <p>Solution</p> <p>Given that, $x_1(t) = 4 \cos(3\pi t + \frac{\pi}{4})$</p> <p>Let T_1 be the periodicity of $x_1(t)$. on comparing $x_1(t)$ with standard form,</p> <p>Find time period T_1</p> $2\pi F_{o1} = 3\pi$ $F_{o1} = \frac{3}{2} \quad \text{period } T_1 = \frac{1}{F_{o1}} = \frac{2}{3} \quad (3M)$ <p>Find time period T_1</p> $x_1(t) = 2 \cos(4\pi t)$ $2\pi F_{o2} = 4\pi$ $F_{o2} = 2 \quad \text{period } T_2 = \frac{1}{F_{o1}} = \frac{1}{2}$ $\frac{T_1}{T_2} = T_1 * \frac{1}{T_2} = \frac{4}{3} \quad (3M)$ <p>Since $x_1(t)$ and $x_1(t)$ are periodic, and the ratio of T_1 and T_2 is a rational number, the signal $x(t)$ is also periodic.</p>
10	<p>Check whether the following signals are periodic / aperiodic signals.</p> <p>$x(t) = \cos 2t + \sin t/5$</p> <p>$x(n) = 3 + \cos \frac{\pi n}{2} + \cos 2n$ (16M)[Nov 2014]-BTL4</p> <p>Answer: Page 57 - Ramesh babu(Similar Type)</p> <p>Solution</p> <p>Given that, $x(t) = \cos 2t + \sin t/5$</p> $x_1(t) = \cos 2t$ <p>Let T_1 be the periodicity of $x_1(t)$. on comparing $x_1(t)$ with standard form,</p> $2\pi F_{o1} = 2$ $F_{o1} = \frac{2}{2\pi} \quad \text{period } T_1 = \frac{1}{F_{o1}} = \frac{2\pi}{2} = \pi$ $x_2(t) = \sin t/5$ $2\pi F_{o2} = 1/5$ $F_{o2} = \frac{1}{10\pi} \quad \text{period } T_2 = \frac{1}{F_{o1}} = 10\pi$ $\frac{T_1}{T_2} = T_1 * \frac{1}{T_2} = \pi * \frac{1}{10\pi} = \frac{1}{10}$ <p>Since $x_1(t)$ and $x_1(t)$ are periodic, and the ratio of T_1 and T_2 is a rational number, the signal $x(t)$ is also periodic. (6M)</p> <p>$x(n) = 3 + \cos \frac{\pi n}{2} + \cos 2n$</p>

	<p>$x_1(n) = \cos \frac{\pi n}{2}$</p> <p>In DT signal periodic,</p> $N_1 = \frac{2\pi}{\omega} (m)$ $\omega = \frac{\pi}{2}$ $N_1 = \frac{2\pi}{\pi/2} (m)$ <p>$N_1 = 4 (m)$ samples. If $m = 1$</p> <p>$N_1 = 4$ samples. (5M)</p> <p>Hence the $x_1(n)$ is periodic signals. Fundamental period of 4 samples.</p> <p>$x_2(n) = \cos 2n$</p> <p>In DT signal periodic,</p> $N_2 = \frac{2\pi}{\omega} (m)$ $\omega = 2$ $N_2 = \frac{2\pi}{2} (m)$ <p>$N_2 = \pi (m)$ samples. If $m = 1$</p> <p>$N_2 = \pi$ samples. (5M)</p> <p>Hence the $x_2(n)$ is non-periodic signals. (5M)</p> <p>From above analysis $x(n)$ is sum of periodic and non-periodic signals. Therefore, $x(n)$ will be non-periodic.</p>
	PART - C
Q.No	Questions
1	<p>Check whether the following system is linear, causal, time invariant and stable.</p> <p>$y(n) = x(n) - x(n-1)$</p> <p>$y(t) = \frac{d}{dt} x(t)$ (15M)[Nov 2014] -BTL4</p> <p>Answer: Page 113 - Ramesh babu (Similar Type)</p> <p>Solution</p> <p>Given that, $y(n) = x(n) - x(n-1)$</p> <p>Causality</p> <p>When $n = 0$; $y(0) = x(0) - x(-1)$; the response at $n = 0$; $y(0)$ depends on the present input $x(0)$ and past input $x(-1)$</p> <p>When $n = 1$; $y(1) = x(1) - x(0)$; the response at $n = 1$; $y(1)$ depends on the present input $x(1)$ and past input $x(0)$</p> <p>From above analysis for any value of n, the system output depends on present and past inputs. Hence the system is causal.</p> <p style="text-align: center;">Linearity</p>

Consider two signals, $x_1(n)$ and $x_2(n)$.

Let $y_1(n)$ and $y_2(n)$ be the response of the system for inputs $x_1(n)$ and $x_2(n)$ respectively.

$$y_1(n) = x_1(n) - x_1(n-1)$$

$$y_2(n) = x_2(n) - x_2(n-1)$$

$$x_3(n) = a x_1(n) - a x_1(n-1) + b x_2(n) - b x_2(n-1)$$

Let, $y_3(n)$ be the response the system for input $x_3(n)$.

$$x_3(n) = a x_1(n) + b x_2(n)$$

Therefore,

$$y_3(n) = a x_1(n) - a x_1(n-1) + b x_2(n) - b x_2(n-1)$$

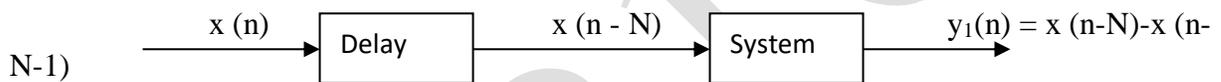
The condition to be satisfied for linearity is,

$$y_3(n) = a y_1(n) + b y_2(n)$$

The given system is linear. (3M)

Time invariance

Response for delayed input

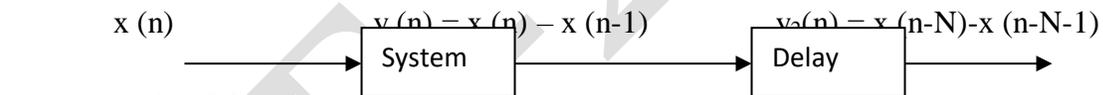


input signal

delayed input

response for delayed input

Delayed response



input signal

delayed response

Hence $y_1(n) = y_2(n)$, therefore the system is time invariant. (2M)

Stability

The given system is an LTI system, so the stability can be determined from impulse response.

The system is stable. (2M)

Result

Causal

Linear

Time invariant

Stable

Given that, $y(t) = \frac{d}{dt} x(t)$

Linearity

Consider two signals, $x_1(t)$ and $x_2(t)$.

Let $y_1(t)$ and $y_2(t)$ be the response of the system for inputs $x_1(t)$ and $x_2(t)$ respectively.

$$y_1(t) = \frac{d}{dt} x_1(t)$$

$$y_2(t) = \frac{d}{dt} x_2(t)$$

$$x_3(t) = a x_1(t) + b x_2(t)$$

Let, $y_3(t)$ be the response the system for input $x_3(t)$.

Therefore,

$$y_3(t) = \frac{d}{dt} x_3(t)$$

$$y_3(t) = \frac{d}{dt} [a x_1(t) + b x_2(t)]$$

$$y_3(t) = a \frac{d}{dt} x_1(t) + b \frac{d}{dt} x_2(t)$$

$$y_3(t) = a y_1(t) + b y_2(t)$$

The given system is linear. (3M)

Causality

$$y(t) = \frac{d}{dt} x(t)$$

In above equation, for any value of t , the $x(t)$ is present input and past input.

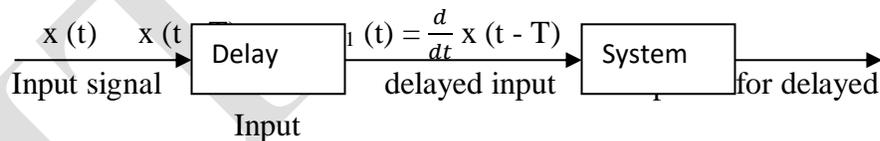
Therefore any value of t depends on present and past input. Hence the system is causal.

Dynamic

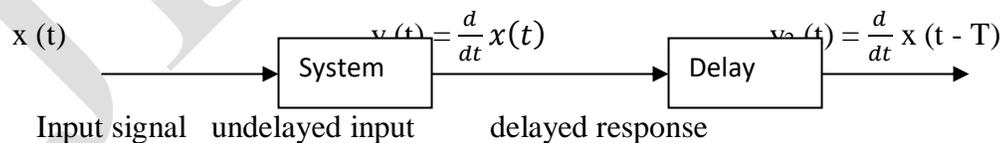
The output of the system depends on differentiation of the input which in turn depends on past and present input. Therefore, the given system is dynamic system.

Time invariance

Response for delayed input



Delayed response



Hence $y_1(t) = y_2(t)$, therefore the system is time invariant (5M)

Stability

The given system is LTI system and the stability can be determined from impulse response. Hence the system is stable.

2

Find whether the following systems are time variant or fixed. Also find whether The systems are linear or nonlinear.

$$\frac{d^3 y(t)}{dt^3} + 4 \frac{d^2 y(t)}{dt^2} + 5 \frac{dy(t)}{dt} + y^2(t) = x(t).$$

$$y(n) = a n^2 x(n) + b n x(n-2)$$

(15M)[May 2016] -BTL4

Answer: Page 112 - Ramesh babu

Given that
$$\frac{d^3 y(t)}{dt^3} + \frac{4 d^2 y(t)}{dt^2} + \frac{5 dy(t)}{dt} + 2y^2(t) = x(t)$$

Linearity

$$\frac{d^3 y(t)}{dt^3} + \frac{4 d^2 y(t)}{dt^2} + \frac{5 dy(t)}{dt} + 2y^2(t) = x(t)$$

The response $y(t)$ involves square root operation which is non-linear operation so system response is non-linear

Causality

The response of the system depends on differentiation of the input which depends on past and present inputs. Hence the system is causal system.

Dynamic

The output of the system depends on differentiation of the input which depends on past and present inputs. Therefore, the given system is dynamic system.

Result

Non-Linear

Causal

Time invariant

Dynamic system

Given that, $y(n) = a n^2 x(n) + b n x(n-2)$

Linearity

Consider two signals, $x_1(n)$ and $x_2(n)$.

Let $y_1(n)$ and $y_2(n)$ be the response of the system for inputs $x_1(n)$ and $x_2(n)$ respectively.

$$y_1(n) = a n^2 x_1(n) + b n x_1(n-2)$$

$$y_2(n) = a n^2 x_2(n) + b n x_2(n-2)$$

$$y_3(n) = a_1 a n^2 x_1(n) + a_1 b n x_1(n-2) + b_1 a n^2 x_2(n) + b_1 b n x_2(n-2)$$

$$x_3(n) = a_1 a n^2 x_1(n) + a_1 b n x_1(n-2) + b_1 a n^2 x_2(n) + b_1 b n x_2(n-2)$$

Let, $y_3(n)$ be the response the system for input $x_3(n)$.

Therefore,

$$y_3(n) = a_1 a n^2 x_1(n) + a_1 b n x_1(n-2) + b_1 a n^2 x_2(n) + b_1 b n x_2(n-2)$$

The given system is linear.

(3M)

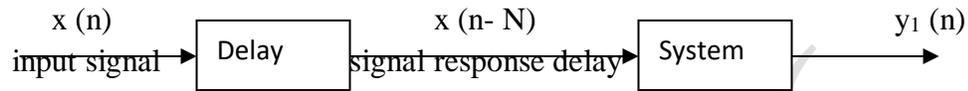
Causality

When $n = 0$; $y(0) = a 0^2 x(0) + b 0 x(0-2)$; the response at $n = 0$, $y(0)$ depends on the Present Input $x(0)$.

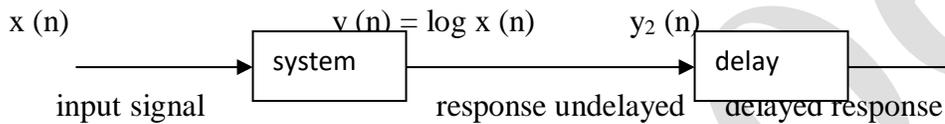
When $n = 1$; $y(1) = a x(1) + b x(-2)$; the response at $n = 1$, $y(1)$ depends on the Present Input $x(1)$ and past input $x(-2)$.
 From above analysis the response for any value of n depends on the present input and past input. Hence the system is causal.

Time invariance (4M)

Response for delayed input



Delayed response



$y_1(n) \neq y_2(n)$, therefore the system is time variant. (4M)

Stability

The given system is a non linear system, and so the test for stability should be performed for specific inputs.

Case i: $x(n)$ tends to ∞ or zero, as n tends to infinity. In this case,

$y(n) = a n^2 x(n) + b n x(n-2)$ will be infinity as n tends to infinity and so the system is unstable.

Case ii: $x(n)$ tends to constant as n tends to infinity. Then, $y(n) = a n^2 x(n) + b n x(n-2)$ will be finite as n tends to infinity and so the system is stable. (4M)

Result

Linear

Causal

Time variant

Given that input – output relationship of a continuous time system $y(t) = t x(-t)$. Determine whether the system is causal, stable, and linear and time invariant.

(15M)[Nov 2015] -BTL4

Answer: Page 112- Ramesh babu(Similar Type)

Solution

Given that, $y(t) = t x(-t)$

Causal

$t = -1$; $y(-1) = -1 * x(1)$ the response $t = -1$, depends on the future input $x(1)$.

$t = 0$; $y(0) = 0 * x(0)$ the response $t = 0$, depends on the present input $x(0)$.

$t = 1$; $y(1) = 1 * x(-1)$ the response $t = 1$, depends on the past input $x(-1)$.

3

From above analysis we can say that the response of the system for $t < 0$ depends on future input. Hence the system is called non-causal.

Linearity

Consider two signals, $x_1(t)$ and $x_2(t)$.

Let $y_1(t)$ and $y_2(t)$ be the response of the system for inputs $x_1(t)$ and $x_2(t)$ respectively.

$$y_1(t) = t x_1(-t)$$

$$y_2(t) = t x_2(-t)$$

$$x_3(t) = a x_1(t) + b x_2(t)$$

Let, $y_3(t)$ be the response the system for input $x_3(t)$.

Therefore,

$$y_3(t) = t x_3(-t)$$

$$y_3(t) = t [a x_1(-t) + b x_2(-t)]$$

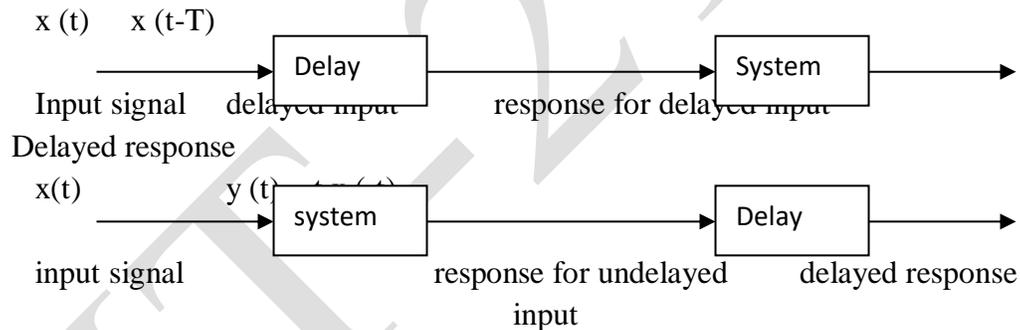
$$y_3(t) = t a x_1(-t) + b t x_2(-t)$$

$$y_3(t) = a y_1(t) + b y_2(t)$$

The given system is linear. (5M)

Time invariance

Response for delayed input



$y_1(t) \neq y_2(t)$, therefore the system is time variant. (5M)

Stability

The given system is a time variant system, and so the test for stability should be performed for specific inputs.

Case i: $x(t)$ tends to ∞ or constant, as t tends to infinity. In this case, $y(t) = t x(-t)$ will be infinity as t tends to infinity and so the system is unstable.

Case ii: $x(t)$ tends to 0 as t tends to infinity. In this case, $y(t) = t x(-t)$ will be 0 as t tends to infinity and so the system is stable. (5M)

Result

Non causal

Linear

Time variant

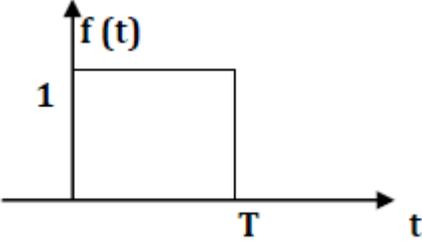
UNIT II- ANALYSIS OF CONTINUOUS TIME SIGNALS

Fourier series for periodic signals - Fourier Transform – properties- Laplace Transforms and properties

PART A

Q.No

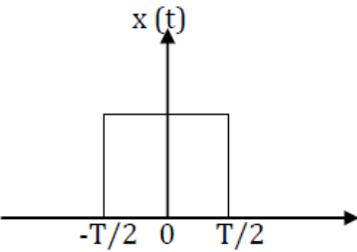
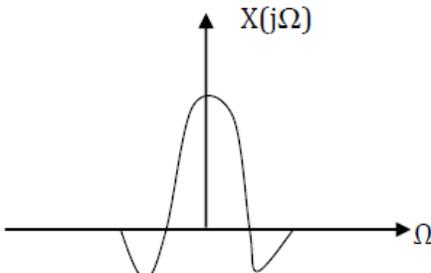
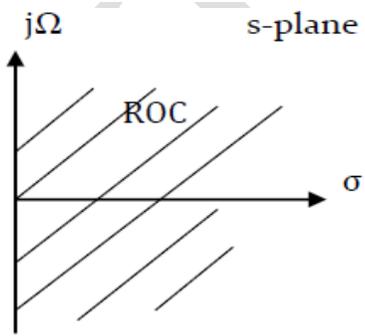
Questions

1	<p>Find the Fourier series co-efficient for the given signal, (May 2019) -BTL3</p> $x(t) = [1 + \cos(2\pi t)] \left[\sin\left(10\pi t + \frac{\pi}{6}\right) \right]$ <p>Solution</p> <p>Given that, $x(t) = [1 + \cos(2\pi t)] \left[\sin\left(10\pi t + \frac{\pi}{6}\right) \right]$</p> $x(t) = \sin\left(10\pi t + \frac{\pi}{6}\right) + \cos(2\pi t) \sin\left(10\pi t + \frac{\pi}{6}\right)$ <p>Using Euler form,</p> $x(t) = \left(\frac{e^{j\pi/6}}{2j} e^{j2\pi t5} - \frac{e^{-j\pi/6}}{2j} e^{-j2\pi t5} \right) + \left(\frac{e^{j2\pi t} + e^{-j2\pi t}}{2} \right) \left(\frac{e^{j\pi/6}}{2j} e^{j2\pi t5} - \frac{e^{-j\pi/6}}{2j} e^{-j2\pi t5} \right)$ <p>Ans :</p> $= \frac{j\pi}{4j}, \frac{-j\pi}{4j}, \frac{j\pi}{2j}, \frac{-j\pi}{2j}$
2	<p>Find the Laplace transform of the given signal, (May 2019)-BTL3</p> <p>Solution</p>  <p>$f(t) = u(t) - u(t - T)$</p> <p>Take Laplace transform of above signal,</p> $= \frac{1}{s} - \frac{1}{s} e^{-sT}$ $= \frac{1}{s} (1 - e^{-sT})$
3	<p>If $X(j\Omega)$ is the Fourier transform of the signal $x(t)$, what is the Fourier transform of the signal $x(3t)$ in terms of $X(j\Omega)$? (Nov 2018)-BTL3</p>

	<p>Solution</p> <p>The Fourier transform of $x(3t)$ is, $\frac{1}{j\Omega} + \pi \delta(\Omega)$</p>
4	<p>Find whether the following system with impulse response $h(t)$ are stable or not. $h(t) = t e^{-t} u(t)$ (Nov 2017)-BTL4</p> <p>Solution</p> $h(t) = t e^{-t} u(t)$ $h(t) = \int_{-\infty}^{\infty} t e^{-t} u(t) dt$ $h(t) = \int_0^{\infty} t e^{-t} dt$ <p>$h(t) = 1$ Condition $1 < \infty$ The system is stable, since system is bounded.</p>
5	<p>Find the Fourier transform of $x(t) = e^{-at} u(t)$ (Nov 2017) -BTL3</p> <p>Solution</p> $X(j\Omega) = \int_{-\infty}^{\infty} x(t) e^{-j\Omega t} dt$ $X(j\Omega) = \int_0^{\infty} e^{-at} e^{-j\Omega t} dt$ $X(j\Omega) = \int_0^{\infty} e^{-(j\Omega+a)t} dt$ $X(j\Omega) = \left[\frac{e^{-(j\Omega+a)t}}{-(j\Omega+a)} \right]$ $X(j\Omega) = \frac{1}{j\Omega+a}$
6	<p>What is the condition for the existence of Fourier series for a signal? –BTL2 State Dirichlets conditions. (or) State the conditions for the convergence of Fourier series Representation of CT periodic signals. [May 2017, Nov 2015, 2014]</p> <p>The Fourier series exists only if the following Dirichlet's conditions are satisfied. The signal $x(t)$ is well defined and single valued, except possibly at a finite number of points. The signal $x(t)$ must possess only a finite number of discontinuities in the period T. The signal must have a finite number of positive and negative maxima in the period T.</p>
7	<p>State parseval's theorem for a continuous time aperiodic signal May 2018, [May 2017] - BTL1</p> <p>The parseval's theorem states that, $x(t) = X(j\Omega)$</p>

	$\int_{-\infty}^{\infty} x(t) ^2 dt = \frac{1}{2\pi} \int_{-\infty}^{\infty} X(j\Omega) ^2$ $ x(t) ^2 = x(t) x^*(t)$ $ X(j\Omega) ^2 = X(j\Omega) X^*(j\Omega)$
8	<p>Find the Fourier series representation of the x(t) and determine Fourier series coefficient (May 2018), [Nov 2016] - BTL3</p> $x(t) = \frac{\cos 2\pi t}{3}$ <p>--</p> $x(t) = \frac{e^{j\omega t} + e^{j\omega t}}{2}$ $x(t) = \frac{1}{2} e^{j\omega t} + \frac{1}{2} e^{-j\omega t} \quad \omega = 2\pi/3$ <p>The Exponential form of Fourier series is,</p> $x(n) = \sum_{n=-\infty}^{\infty} c_n e^{jn\omega t}$ $x(t) = c_{-1} e^{-jt\omega} + c_0 + c_1 e^{j\omega t} + \dots$ <p>Comparing above equations, $c_0 = 0$ $c_1 = c_{-1} = 1/2$</p>
9	<p>Find the Laplace transform of x(t) = e^{-at} u(t) [Nov 2016] -BTL3</p> <p>Solution</p> $X(s) = \int_{-\infty}^{\infty} x(t) e^{-st} dt$ $X(s) = \int_0^{\infty} e^{-at} e^{-st} dt$ $X(s) = \int_0^{\infty} e^{-(s+a)t} dt$ $X(s) = \left[\frac{e^{-(s+a)t}}{-(s+a)} \right]$ $X(s) = \frac{1}{s+a}$
10	<p>Give the Laplace transform of x(t) [May 2016] -BTL1</p> $x(t) = 3e^{-2t} u(t) - 2e^{-t} u(t)$ <p>Solution</p>

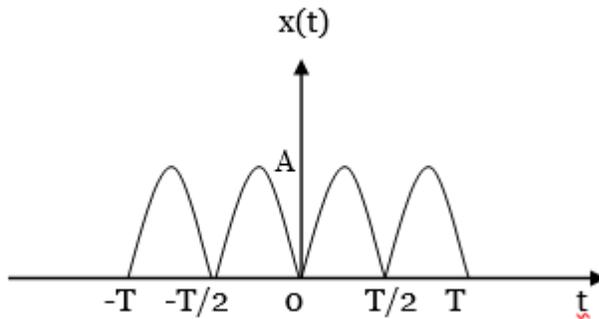
	$X(s) = \int_{-\infty}^{\infty} x(t)e^{-st} dt$ $X(s) = \frac{3}{s+2} - \frac{2}{s+1}$
11	<p>Give the relation between Fourier Transform and Laplace Transform. -BTL4 [Nov 2015], [Nov 2014], [May 2016] x(t) be a continuous time signal, defined as, The definition of Laplace Transform of x(t) is,</p> $X(s) = \int_{-\infty}^{\infty} x(t)e^{-st} dt$ <p>On substituting $s = \sigma + j\Omega$ in above equation,</p> $X(s) = \int_{-\infty}^{\infty} x(t)e^{-(\sigma+j\Omega)t} dt$ <p>$\sigma = 0$, the definition of Fourier Transform of x(t) is,</p> $X(j\Omega) = \int_{-\infty}^{\infty} x(t)e^{-j\Omega t} dt$
12	<p>Find the Fourier coefficients of the signal $x(t) = 1 + \sin 2\omega t + 2 \cos 2\omega t + \cos(3\omega t + \pi/3)$ [May 2015] -BTL3</p> <p>Given: $x(t) = 1 + \sin 2\omega t + 2 \cos 2\omega t + \cos\left(3\omega t + \frac{\pi}{3}\right)$</p> $x(t) = 1 + \frac{e^{j2\omega t} - e^{-j2\omega t}}{2j} + 2\left(\frac{e^{j2\omega t} + e^{-j2\omega t}}{2}\right) + \frac{e^{j(3\omega t + \frac{\pi}{3})} - e^{-j(3\omega t + \frac{\pi}{3})}}{2}$ $= 1 + \frac{1}{2j} e^{j2\omega t} - \frac{1}{2j} e^{-j2\omega t} + e^{j2\omega t} + e^{-j2\omega t} + \frac{1}{2} \left(e^{j3\omega t} e^{j\frac{\pi}{3}} \right) + \frac{1}{2} \left(e^{-j3\omega t} e^{-j\frac{\pi}{3}} \right)$ $= 1 + \frac{1}{2j} e^{j2\omega t} - \frac{1}{2j} e^{-j2\omega t} + e^{j2\omega t} + e^{-j2\omega t} + \frac{1}{2} \left\{ e^{j3\omega t} \left(\cos \frac{\pi}{3} + j \sin \frac{\pi}{3} \right) \right\} +$ $\frac{1}{2} \left\{ e^{-j3\omega t} \left(\cos \frac{\pi}{3} - j \sin \frac{\pi}{3} \right) \right\}$ $= 1 + e^{j2\omega t} \left(1 + \frac{1}{2j} \right) + e^{-j2\omega t} \left(1 - \frac{1}{2j} \right) + \frac{1}{2} \left\{ e^{j3\omega t} (0.5 + j0.866) \right\} + \frac{1}{2} \left\{ e^{-j3\omega t} (0.5 - j0.866) \right\}$ $= 1 + (1 - 0.5j) e^{j2\omega t} + (1 + 0.5j) e^{-j2\omega t} + (0.25 + 0.433j) e^{j3\omega t} + (0.25 - 0.433j) e^{-j3\omega t}$ $= (0.25 - 0.433j) e^{-j3\omega t} + (1 + 0.5j) e^{-j2\omega t} + 1 + (1 - 0.5j) e^{j2\omega t} + (0.25 + 0.433j) e^{j3\omega t}$

	<p>The exponential form of Fourier series is $c_{-3} = 0.25 - 0.433j$ $c_1 = 0$ $c_{-2} = 1 + 0.5j$ $c_2 = 1 - 0.5j$ $c_{-1} = 0$ $c_3 = 0.25 + 0.433j$</p>
<p>13</p>	<p>Draw the spectrum of a CT rectangular pulse. [May 2015] -BTL1</p> <div style="display: flex; justify-content: space-around; align-items: center;"> <div style="text-align: center;">  <p>$x(t)$</p> </div> <div style="text-align: center;">  <p>$X(jΩ)$</p> </div> </div>
<p>14</p>	<p>Find the ROC of the Laplace Transform of $x(t) = u(t)$. [Nov 2014] -BTL2</p> <p>Solution</p> $X(s) = \int_{-\infty}^{\infty} x(t)e^{-st} dt$ $X(s) = \int_0^{\infty} e^{-st} dt$ $X(s) = \left[\frac{e^{-st}}{-s} \right]$ $X(s) = \frac{1}{s}$ <div style="text-align: center;">  <p>$jΩ$ s-plane</p> <p>ROC</p> <p>$σ$</p> </div>
<p>15</p>	<p>What is the Fourier Transform of $x(t) = \delta(t)$ [May 2015] -BTL1</p> <p>The impulse signal is defined as, $x(t) = \delta(t) = 1$ for $t = 0$ 0 for $t \neq 0$</p>

	$X(j\Omega) = \int_{-\infty}^{\infty} x(t)e^{-j\Omega t} dt$ $X(j\Omega) = \int_{-\infty}^{\infty} 1 \cdot e^{-j\Omega t} dt$ $X(j\Omega) = 1$
16	<p>Obtain Fourier Series Coefficients for $x(n) = \sin n\omega$ [May 2015] -BTL3</p> $x(n) = \frac{e^{j\omega n} + e^{-j\omega n}}{2j}$ $x(n) = \frac{1}{2j} e^{j\omega n} - \frac{1}{2j} e^{-j\omega n}$ <p>The Exponential form of Fourier series is,</p> $x(n) = \sum_{n=-\infty}^{\infty} c_n e^{jn\omega t}$ $x(n) = c_{-1} e^{-j\omega t} + c_0 + c_1 e^{j\omega t} + \dots$ <p>Comparing above equations,</p> $c_0 = 0 \qquad c_1 = c_{-1} = 1/2$
17	<p>State any two properties of ROC of Laplace transform X(s) of a Signal x(t). [May 2014] -BTL1</p> <p>Convolution property Laplace transform of convolution of two functions are equivalent to multiplications of their Laplace Transform.</p> <p>Laplace Transform of, $x_1(t) = X_1(s)$ Laplace Transform of, $x_2(t) = X_2(s)$ Laplace Transform of, $x_1(t) * x_2(t) = X_1(s) * X_2(s)$</p> <p>Time shifting property The Time shifting property of Laplace Transform says that, $x(t) = X(s)$ Laplace Transform of, $x(t+a) = e^{as} X(s)$ Laplace Transform of, $x(t-a) = e^{-as} X(s)$</p>
18	<p>Give the equation for trigonometric Fourier series. [Nov 2013]-BTL1</p> <p>The trigonometric form of Fourier series of a periodic signal, $x(t)$ with period T is Defined as,</p> $x(t) = \frac{a_0}{2} + \sum_{n=1}^{\infty} a_n \cos n\Omega_0 t + \sum_{n=1}^{\infty} b_n \sin n\Omega_0 t$ <p>Where, $\Omega_0 = 2\pi f_0 =$ Fundamental frequency $F_0 =$ Fundamental frequency $n =$ Harmonic order $n\Omega_0 =$ Harmonic frequency a_n, a_n and $b_0 =$ Fourier coefficients of trigonometric form of Fourier series.</p>

19	<p>States the time scaling property of Laplace transform. [May 2013] -BTL1</p> <p>The time scaling property of Laplace transform says that, Laplace transform of $x(t) = X(s)$</p> $x(at) = \frac{1}{ a } X\left(\frac{s}{a}\right)$								
20	<p>What is a FT of a DC signal of amplitude 1? [May 2013] -BTL2</p> <p>Let $x(t) = A$, where A is constant Where $A = \lim_{a \rightarrow 0} A e^{-at}$ $x(t) = \lim_{a \rightarrow 0} A e^{-at}$ $X(j\Omega) = \delta(\Omega)$</p>								
21	<p>Give the synthesis and analysis equations of CTFT. [Nov 2012] -BTL1</p> <p>Synthesis equation: $x(t) = \int_{-\infty}^{\infty} X(j\Omega) e^{jn\Omega t} d\Omega$</p> <p>It is also called as inverse Fourier Transform. Analysis equation: $X(j\Omega) = \int_{-\infty}^{\infty} x(t) e^{-jn\Omega t} dt$</p> <p>It is also called as Fourier Transform</p>								
22	<p>Define the region of convergence of the Laplace transform. [Nov 2012] -BTL1</p> <p>The Region of Convergence of $X(s)$ is the set of set all values of σ for which the Laplace Transform converges. Condition for convergence: The necessary condition for convergence of the Laplace transform is absolutely integrable of $x(t)$ exist if, $\int_{-\infty}^{\infty} x(t) e^{-\sigma t} < \infty$</p>								
23	<p>Distinguish between Fourier series and Fourier Transform. -BTL2</p> <table border="1" data-bbox="235 1566 1425 1856"> <thead> <tr> <th data-bbox="235 1566 824 1633">Fourier series</th> <th data-bbox="824 1566 1425 1633">Fourier Transform</th> </tr> </thead> <tbody> <tr> <td data-bbox="235 1633 824 1724">Defined only for periodic signals</td> <td data-bbox="824 1633 1425 1724">Defined both periodic and non-periodic Signals</td> </tr> <tr> <td data-bbox="235 1724 824 1770">The spectrum is discrete</td> <td data-bbox="824 1724 1425 1770">The spectrum is continuous</td> </tr> <tr> <td data-bbox="235 1770 824 1856">Parseval's relation of Fourier series is used to calculate power spectral density</td> <td data-bbox="824 1770 1425 1856">Parseval's relation of Fourier Transform is used to calculate power spectral density</td> </tr> </tbody> </table>	Fourier series	Fourier Transform	Defined only for periodic signals	Defined both periodic and non-periodic Signals	The spectrum is discrete	The spectrum is continuous	Parseval's relation of Fourier series is used to calculate power spectral density	Parseval's relation of Fourier Transform is used to calculate power spectral density
Fourier series	Fourier Transform								
Defined only for periodic signals	Defined both periodic and non-periodic Signals								
The spectrum is discrete	The spectrum is continuous								
Parseval's relation of Fourier series is used to calculate power spectral density	Parseval's relation of Fourier Transform is used to calculate power spectral density								

24	<p>Determine the Laplace transform of the signal $\delta(t-5)$ and $u(t-5)$ [May 2012] –BTL3</p> <p>$\delta(t-5)$</p> $X(s) = \int_{-\infty}^{\infty} x(t)e^{-st} dt$ $X(s) = \int_{-\infty}^{\infty} \delta(t-5)e^{-st} dt$ <p>If $t = 5$</p> $X(s) = e^{-s5}$ <p>$u(t-5)$</p> $X(s) = \int_{-\infty}^{\infty} x(t)e^{-st} dt$ $X(s) = \int_{-\infty}^{\infty} u(t-5)e^{-st} dt$ $X(s) = \int_5^{\infty} e^{-st} dt$ $X(s) = \frac{e^{-5s}}{s}$
25	<p>Compare double sided and single sided spectrums. BTL2</p> <p>The method of representing spectrums of positive as well as negative frequencies are called double sided spectrums.</p> <p>The method of representing spectrums only in the positive frequencies is known as single sided spectrums.</p>
	PART-B
Q.No.	Questions
1	<p>Obtain the Fourier co-efficient and write the Quadrature form of a fully rectified sine wave. [May 2017] -BTL3(13M)</p> <p>Answer: Page 165- Ramesh babu</p>



(2M)

The output of full wave rectifier and it has even symmetry

$$a_0 = \frac{4}{T} \int_0^{T/2} x(t) dt$$

$$a_n = \frac{4}{T} \int_0^{T/2} x(t) \cos n\Omega_0 t dt$$

$$b_n = 0$$

(2M)

The mathematical equation of full wave rectified output is,

$$x(t) = A \sin \Omega_0 t ; \text{ for } t = 0 \text{ to } \frac{T}{2}$$

$$\Omega_0 = \frac{2\pi}{T}$$

Find a_0

$$a_0 = \frac{4}{T} \int_0^{T/2} x(t) dt$$

$$a_0 = \frac{4}{T} \int_0^{T/2} A \sin \Omega_0 t dt$$

$$= \frac{4A}{T} \left[-\frac{\cos \Omega_0 t}{\Omega_0} \right]_0^{T/2}$$

$$= \frac{4A}{T} \left[-\frac{\cos \frac{2\pi}{T} t}{\frac{2\pi}{T}} \right]_0^{T/2}$$

$$\begin{aligned}
 &= \frac{4A}{T} \left[-\frac{\cos \frac{2\pi}{T} t}{\frac{2\pi}{T}} \right]_0^{T/2} \\
 &= \frac{4A}{T} \left[\frac{\cos \frac{2\pi}{T} t}{\frac{2\pi}{T}} + \frac{\cos 0}{\frac{2\pi}{T}} \right] && \cos \pi = -1 \\
 &= \frac{2A}{\pi} [-\cos \pi + \cos 0] && \cos 0 = 1 \\
 &= \frac{2A}{\pi} [1 + 1] = \frac{4A}{\pi} && (4M)
 \end{aligned}$$

Find a_n

$$a_n = \frac{4}{T} \int_0^{T/2} x(t) \cos n\Omega t dt$$

$$a_n = \frac{4}{T} \int_0^{T/2} \sin \Omega t \cos n\Omega t dt \quad ; \quad 2 \sin A \sin B = \sin (A+B) + \sin (A-B)$$

$$\begin{aligned}
 a_n &= \frac{4A}{T} \int_0^{T/2} \frac{\sin (\Omega t + n\Omega t) + \sin(\Omega t - n\Omega t)}{2} dt \\
 a_n &= \frac{2A}{T} \int_0^{T/2} \sin(1+n)\Omega t dt + \frac{2A}{T} \int_0^{T/2} \sin(1-n)\Omega t dt \\
 &= \frac{2A}{T} \left[\frac{-\cos(1+n)\Omega t}{(1+n)\Omega} \right]_0^{T/2} + \frac{2A}{T} \left[\frac{-\cos(1-n)\Omega t}{(1-n)\Omega} \right]_0^{T/2} \\
 &= \frac{2A}{T} \left[\frac{-\cos(1+n)\frac{2\pi}{T} \frac{T}{2}}{(1+n)\Omega} \right] + \frac{2A}{T} \left[\frac{-\cos(1-n)\frac{2\pi}{T} \frac{T}{2}}{(1-n)\Omega} \right] \\
 &= \frac{2A}{T} \left[\frac{-\cos(1+n)\frac{2\pi}{T} \frac{T}{2}}{(1+n)\frac{2\pi}{T}} \frac{\cos 0}{(1+n)\frac{2\pi}{T}} \right] + \frac{2A}{T} \left[\frac{-\cos(1-n)\frac{2\pi}{T} \frac{T}{2}}{(1-n)\frac{2\pi}{T}} \frac{\cos 0}{(1-n)\frac{2\pi}{T}} \right] \\
 &= \frac{-A \cos(1+n)\pi}{(1+n)\pi} + \frac{A}{(1+n)\pi} - \frac{A \cos(1-n)\pi}{(1-n)\pi} + \frac{A}{(1-n)\pi} && (3M)
 \end{aligned}$$

When n is even integer, $(1+n)$ and $(1-n)$ will be odd, Therefore, $\cos(1+n)\pi = -1$; $\cos(1-n)\pi = -1$

When n is odd integer, $(1+n)$ and $(1-n)$ will be even,

Therefore, $\cos(1+n)\pi = 1$; $\cos(1-n)\pi = 1$

$$a_n = \frac{A}{(1+n)\pi} + \frac{A}{(1+n)\pi} + \frac{A}{(1-n)\pi} + \frac{A}{(1-n)\pi}; \text{ for even values of } n$$

Fourier series equation

The trigonometric form Fourier series of $x(t)$ is,

	$x(t) = \frac{a_0}{2} + \sum_{n=1}^{\infty} a_n \cos n\Omega t + \sum_{n=1}^{\infty} b_n \sin n\Omega t$ <p style="text-align: right;">(2M)</p> <p>here, $b_n = 0$ and a_n exists only for even values of n</p> $x(t) = \frac{a_0}{2} + \sum_{n=1}^{\infty} a_n \cos n\Omega t$ $x(t) = \frac{2A}{\pi} + \sum_{n=\text{even}} \left[\frac{A}{(1+n)\pi} + \frac{A}{(1+n)\pi} + \frac{A}{(1-n)\pi} + \frac{A}{(1-n)\pi} \right] \cos n\Omega t$
2	<p>Determine the inverse Laplace transform of the following (13M) [May 2017] -BTL3</p> <p>i. $x(s) = \frac{1-2s^2-14s}{s(s+3)(s+4)}$</p> <p>ii. $x(s) = \frac{2s^2+10s+7}{(s+1)(s^2+3s+2)}$</p> <p>Answer: Page 404 - Ramesh babu(Similar Type) Solution Given that,</p> $x(s) = \frac{1-2s^2-14s}{s(s+3)(s+4)}$ <p>By partial fraction expansion technique, $X(s)$ can be expressed as,</p> $X(s) = \frac{1-2s^2-14s}{s(s+3)(s+4)} = \frac{A}{s} + \frac{B}{(s+3)} + \frac{C}{(s+4)}$ <p>Case i Given that ROC lies between lines passing through $s = -5$ to $s = 3$. Hence $x(t)$ will be two sided signal. The term pole -5 will be causal and term 3 will be anticausal (7M)</p> $x(t) = \frac{-1}{8} e^{-5t} u(t) - \frac{1}{8} e^{3t} u(-t)$ <p>case ii Given that ROC is right of the line passing through $s = 3$, hence $x(t)$ will be causal signal. (6M)</p>

	$x(t) = \frac{-1}{8} e^{-5t} u(t) - \frac{1}{8} e^{3t} u(t)$
3.	<p>Find the Fourier transform of the signal $x(t) = \cos \Omega_0 t u(t)$ (13M) [Nov 2016] -BTL3</p> <p>Answer: Page 306- Ramesh babu</p> <p>Solution</p> <p>Given that, $x(t) = \cos \Omega_0 t u(t)$</p> <p>By definition of Fourier transform,</p> $X(j\Omega) = \int_{-\infty}^{\infty} x(t) e^{-j\Omega t} dt$ $X(j\Omega) = \int_0^{\infty} \cos \Omega_0 t e^{-j\Omega t} dt$ $= \int_0^{\infty} \frac{e^{j\Omega_0 t} + e^{-j\Omega_0 t}}{2} e^{-j\Omega t} dt$ <p style="text-align: right;">note : $\cos \Omega t = \frac{e^{j\Omega t} + e^{-j\Omega t}}{2}$</p> <p>The complex exponential signal is defined as, $x(t) = e^{j\Omega_0 t}$ on taking Fourier transform,</p> $X(j\Omega) = 2\pi\delta(\Omega - \Omega_0)$ <p>Similarly,</p> $x(t) = e^{-j\Omega_0 t}$ <p>(3)</p> <p>on taking Fourier transform, $X(j\Omega) = 2\pi\delta(\Omega + \Omega_0)$</p> $= \frac{1}{2} [2\pi\delta(\Omega - \Omega_0) + 2\pi\delta(\Omega + \Omega_0)]$ $= \pi [2\pi\delta(\Omega - \Omega_0) + 2\pi\delta(\Omega + \Omega_0)]$ <p style="text-align: right;">(4M)</p>
4.	<p>State and prove the multiplication and convolution property of Fourier transform.(13M) [Nov 2016] -BTL1</p> <p>Answer: Page 320-327- Ramesh babu</p> <p>Multiplication property</p> <p>It is also called frequency convolution</p> <p>Let, fourier transform of $x_1(t) = X_1(j\Omega)$</p> <p>Let, fourier transform of $x_2(t) = X_2(j\Omega)$</p> <p>The frequency convolution property of Fourier transform says that,</p> $x_1(t) x_2(t) = \frac{1}{2\pi} \int_{\lambda=-\infty}^{\lambda=\infty} X_1(j\Omega) X_2(j(\Omega - \lambda)) d\lambda$ <p style="text-align: right;">(4M)</p> <p>Proof</p> <p>By definition of Fourier transform</p>

$$X(j\Omega) = \int_{-\infty}^{\infty} x(t)e^{-j\Omega t} dt$$

$$X_1(j\Omega) X_2(j\Omega) = \int_{t=-\infty}^{t=\infty} x_1(t)x_2(t)e^{-j\Omega t} dt$$

By definition of inverse Fourier transform,

Convolution property

The convolution theorem of Fourier transform says that, Fourier transform of convolution of two signals is given by the product of the Fourier transform of the individual signals,

Let, fourier transform of $x_1(t) = X_1(j\Omega)$ Let, fourier transform of $x_2(t) = X_2(j\Omega)$

$$x_1(t) * x_2(t) = X_1(j\Omega) X_2(j\Omega)$$

This above equation is known as convolution property of Fourier transform. By definition of convolution of CT signals,

$$x_1(t) * x_2(t) = \int_{\tau=-\infty}^{\tau=\infty} x_1(\tau)x_2(t - \tau)d\tau \quad (4M)$$

τ is a dummy variable used for integration.

Proof

By definition of Fourier transform

$$X_1(j\Omega) = \int_{-\infty}^{\infty} x_1(t)e^{-j\Omega t} dt$$

$$X_2(j\Omega) = \int_{-\infty}^{\infty} x_2(t)e^{-j\Omega t} dt$$

$$x_1(t) * x_2(t) = \int_{t=-\infty}^{t=\infty} x_1(t) * x_2(t)e^{-j\Omega t} dt$$

$$e^{-j\Omega t} = e^{j\Omega\tau} e^{-j\Omega\tau} e^{-j\Omega t} = e^{-j\Omega\tau} e^{-j\Omega(t-\tau)}$$

$$x_1(t) * x_2(t) = \int_{t=-\infty}^{t=\infty} x_1(t)e^{-j\Omega t} dt \int_{t=-\infty}^{t=\infty} x_2(t)e^{-j\Omega t} dt \quad (5M)$$

$$x_1(t) * x_2(t) = X_1(j\Omega) X_2(j\Omega)$$

5

State and prove Parseval's theorem of Fourier Transform? State and prove Rayleigh's theorem.(6M) [May 2016]R13, May 2013, May 2016]-BTL1

Answer: Page 322 - Ramesh babu

The parseval's theorem states that, $x(t) = X(j\Omega)$

	$\int_{-\infty}^{\infty} x(t) ^2 dt = \frac{1}{2\pi} \int_{-\infty}^{\infty} X(j\Omega) ^2$ $ x(t) ^2 = x(t) x^*(t)$ $ X(j\Omega) ^2 = X(j\Omega) X^*(j\Omega)$ <p>By definition of inverse Fourier transform,</p> $x(t) = \frac{1}{2\pi} \int_{-\infty}^{\infty} X(j\Omega) e^{j\Omega t} d\Omega$ <p>on taking conjugate of the above equation,</p> $x^*(t) = \frac{1}{2\pi} \int_{-\infty}^{\infty} X^*(j\Omega) e^{j\Omega t} d\Omega$ $x^*(t) = \frac{1}{2\pi} \int_{-\infty}^{\infty} X^*(j\Omega) \int_{-\infty}^{\infty} x(t) e^{-j\Omega t} dt d\Omega$ $= \frac{1}{2\pi} \int_{-\infty}^{\infty} X^*(j\Omega) X(j\Omega) d\Omega$ $\int_{-\infty}^{\infty} x(t) ^2 dt = \frac{1}{2\pi} \int_{-\infty}^{\infty} X(j\Omega) ^2$ <p>Hence it was proved.</p> <p style="text-align: right;">(3M)</p>
6	<p>If $x(t) = X(\omega)$. Then using time shifting property show the $x(t+T) + x(t-T) = 2X(\omega) \cos \omega T$ (6M)[May 2015]-BTL3</p> <p>Answer: Page 329 - Ramesh babu(Similar Type)</p> <p>Solution</p> <p>Given that, $x(t) = X(j\Omega)$</p> <p>The time shifting property of Fourier transform says that, $F\{x(t-t_0)\} = e^{-j\Omega t_0} X(j\Omega)$</p> $F\{x(t+T)\} = e^{j\Omega T} X(j\Omega)$ $F\{x(t-T)\} = e^{-j\Omega T} X(j\Omega) \quad (3M)$ $F\{x(t+T) + x(t-T)\} = e^{j\Omega T} X(j\Omega) + e^{-j\Omega T} X(j\Omega)$ $= X(j\Omega) [e^{j\Omega T} + e^{-j\Omega T}]$ $= X(j\Omega) [2 \cos \Omega T]$ $F\{x(t+T) + x(t-T)\} = 2 X(j\Omega) \cos \Omega T \quad (3M)$
7	<p>Find the Fourier transform of $x(t) = t e^{-at} u(t)$ (6M)[Nov 2015]-BTL5</p> <p>Answer: Page 332 - Ramesh babu</p> <p>Solution</p> <p>Given that, $x(t) = t e^{-at} u(t) = t e^{-at}; t \geq 0$</p> <p>By definition of Fourier transform,</p> $X(j\Omega) = \int_0^{\infty} x(t) e^{-j\Omega t} dt$

	$X(j\Omega) = \int_{-\infty}^{\infty} t e^{-at} e^{-j\Omega t} dt$ $X(j\Omega) = \int_0^{\infty} t e^{-(a+j\Omega)t} dt$ $= \frac{t e^{-(a+j\Omega)t}}{-(a+j\Omega)} - \int \left[\frac{e^{-(a+j\Omega)t}}{-(a+j\Omega)} dt \right]_0^{\infty}$ $= \left[\frac{-t e^{-(a+j\Omega)t}}{(a+j\Omega)} - \frac{e^{-(a+j\Omega)t}}{-(a+j\Omega)^2} \right]_0^{\infty}$ $X(j\Omega) = \frac{1}{(a+j\Omega)^2}$ <p style="text-align: right;">(3M)</p>
8	<p>Find the Laplace transform and its associated ROC for the signal</p> <p>$x(t) = t e^{-2 t }$ (13M)[May 2016, 2015]R13, Nov 2013, May 2016-BTL5</p> <p>Answer: Page 395 - Ramesh babu(Similar Type)</p> <p>Solution</p> <p>Given that,</p> $x(t) = t e^{-2 t } = \begin{cases} t e^{2t}; & -\infty \leq t \leq 0 \\ t e^{-2t}; & 0 \leq t \leq \infty \end{cases}$ <p>By definition of Laplace transform,</p> $X(s) = \int_{-\infty}^{\infty} x(t) e^{-st} dt$ $X(s) = \int_{-\infty}^0 t e^{2t} e^{-st} dt + \int_0^{\infty} t e^{-2t} e^{-st} dt$ $= \int_{-\infty}^0 t e^{-(s-2)t} dt + \int_0^{\infty} t e^{-(s+2)t} dt$ <p style="text-align: right;">(6M)</p>

$$\int u dv = uv - \int v du$$

$u = t \quad du = 1$	$u = t \quad du = 1$
$dv = e^{-(s-2)t} \quad v = \frac{e^{-(s-2)t}}{-(s-2)}$	$dv = e^{-(s+2)t} \quad v = \frac{e^{-(s+2)t}}{-(s+2)}$

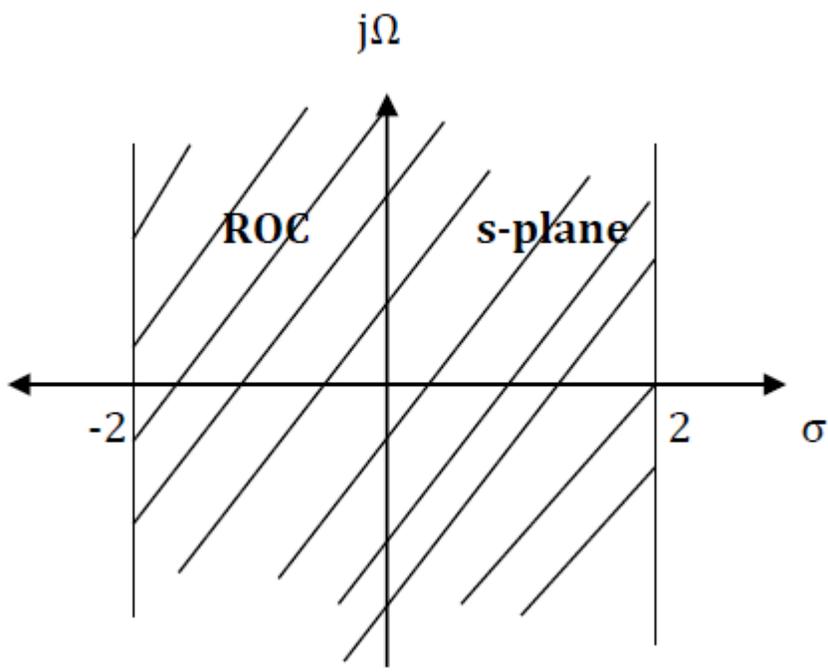
$$\begin{aligned}
 &= \left[t \frac{e^{-(s-2)t}}{-(s-2)} \right]_{-\infty}^0 - \int_{-\infty}^0 \frac{e^{-(s-2)t}}{-(s-2)} dt + \left[t \frac{e^{-(s+2)t}}{-(s+2)} \right]_0^{\infty} - \int_0^{\infty} \frac{e^{-(s+2)t}}{-(s+2)} dt \\
 &= \left[\frac{-t e^{-(s-2)t}}{(s-2)} \right]_{-\infty}^0 - \left[\frac{e^{-(s-2)t}}{(s-2)^2} \right]_{-\infty}^0 + \left[\frac{-t e^{-(s+2)t}}{(s+2)} \right]_0^{\infty} - \left[\frac{e^{-(s+2)t}}{(s+2)^2} \right]_0^{-\infty}
 \end{aligned} \tag{3M}$$

X (s) converges when σ lies between -2 and +2, the X(s) is given by,

$$\begin{aligned}
 &= \frac{1}{(s-2)^2} + \frac{1}{(s+2)^2} \\
 &= \frac{-(s+2)^2 + (s-2)^2}{(s-2)^2 (s+2)^2} \\
 &= \frac{-(s^2 + 4s + 4) - (s^2 - 4s + 4)}{[(s-2)(s+2)]^2} \\
 &= \frac{-8}{(s^2 - 4)^2}
 \end{aligned}$$

X (s) = $\frac{-8}{(s^2 - 4)^2}$ with ROC as all points in s-plane in between the lines passing through $\sigma = -2$ and $\sigma = 2$.

(4M)

	
	PART-C
Q.N 0	Questions
1	<p>From basic formula, determine the Fourier Transform of the given signals. Obtain the magnitude and phase spectra of the given signals.</p> <p>(i) $t e^{-at} u(t)$, $a > 0$</p> <p>(ii) $e^{-a t }$, $a > 0$ (15M)[May2016,2015],Nov 2013,May 2016-BTL3</p> <p>Solution</p> <p>Given that, $x(t) = t e^{-at} u(t)$, $a > 0$</p> <p>By definition of Fourier transform,</p> $X(j\Omega) = \int_{-\infty}^{\infty} x(t) e^{-j\Omega t} dt$ $X(j\Omega) = \int_0^{\infty} t e^{-at} e^{-j\Omega t} dt$ $X(j\Omega) = \int_0^{\infty} t e^{-(a+j\Omega)t} dt$

$$= \frac{te^{-(a+j\Omega)t}}{-(a+j\Omega)} - \int \left[\frac{e^{-(a+j\Omega)t}}{-(a+j\Omega)} dt \right]_0^{\infty}$$

$$= \left[\frac{-te^{-(a+j\Omega)t}}{(a+j\Omega)} - \frac{e^{-(a+j\Omega)t}}{-(a+j\Omega)^2} \right]_0^{\infty}$$

$$X(j\Omega) = \frac{1}{(a+j\Omega)^2}$$

(5)

Given that, $x(t) = e^{-at}$

$$x(t) = \begin{cases} e^{at} & ; \text{for } t = -\infty \text{ to } 0 \\ e^{-at} & ; \text{for } t = 0 \text{ to } \infty \end{cases}$$

By definition of Fourier transform,

$$X(j\Omega) = \int_{-\infty}^{\infty} x(t)e^{-j\Omega t} dt$$

$$X(j\Omega) = \int_{-\infty}^0 e^{at} e^{-j\Omega t} dt + \int_0^{\infty} e^{-at} e^{-j\Omega t} dt$$

$$= \int_{-\infty}^0 e^{(a-j\Omega)t} dt + \int_0^{\infty} e^{-(a+j\Omega)t} dt$$

$$= \left[\frac{e^{(a-j\Omega)t}}{(a-j\Omega)} \right]_{-\infty}^0 + \left[\frac{e^{-(a+j\Omega)t}}{-(a+j\Omega)} \right]_0^{\infty}$$

$$= \frac{e^0}{a-j\Omega} - \frac{e^{-\infty}}{a-j\Omega} + \frac{e^{-\infty}}{-(a+j\Omega)} - \frac{e^0}{-(a+j\Omega)}$$

$$= \frac{1}{a-j\Omega} + \frac{1}{a+j\Omega}$$

$$= \frac{(a+j\Omega) + (a-j\Omega)}{(a-j\Omega)(a+j\Omega)}$$

$$= \frac{a^2}{a^2 + \Omega^2}$$

(5)

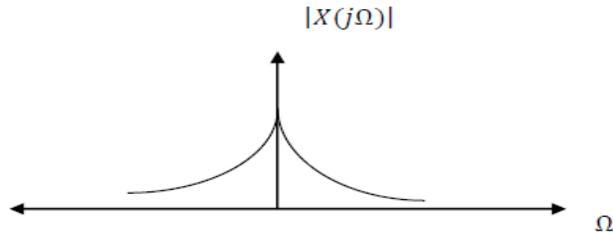
Here $X(j\Omega)$ is purely real so phase becomes zero.

Assume $a = 2$

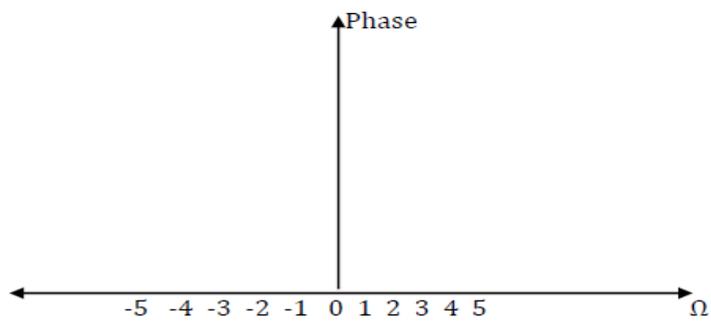
Magnitude and phase values

Ω	-4	-3	-2	-1	0	1	2	3	4
$ X(j\Omega) $	0.2	0.308	0.5	0.8	1	0.8	0.5	0.308	0.2
phase	0	0	0	0	0	0	0	0	0

Magnitude Spectrum



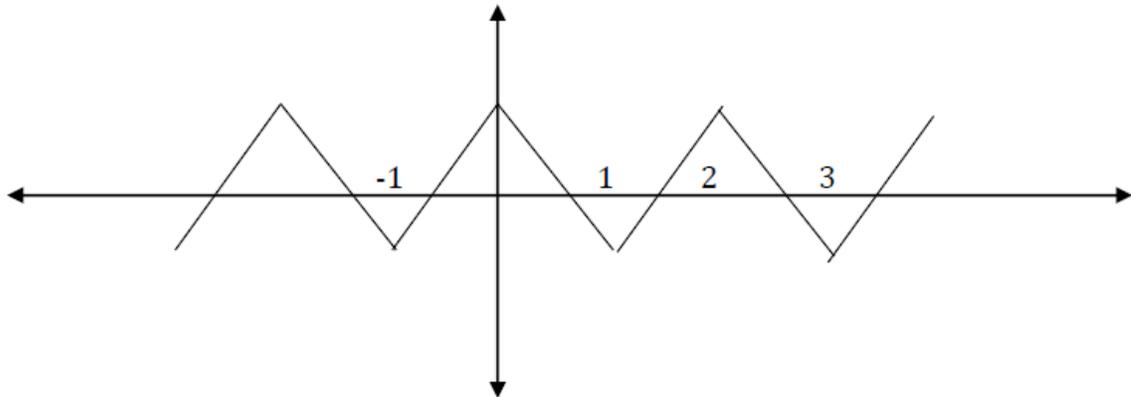
Phase Spectrum



(5)

Obtain the Fourier series co-efficient and plot the spectrum for the given Waveform.(15)
 [May 2016]R13-BTL3

2



Solution

The given waveform has even symmetry,

$$a_0 = \frac{1}{T} \int_0^{T/2} x(t) dt$$

$$a_n = \frac{4}{T} \int_0^{T/2} x(t) \cos n\Omega t dt$$

$$b_n = 0$$

from the waveform

(3)

$$x(t) = \frac{2t}{T} \text{ for } t = 0 \text{ to } T/2$$

Find a_0

$$a_0 = \frac{4}{T} \int_0^{T/2} x(t) dt$$

$$a_0 = \frac{4}{T} \int_0^{T/2} \frac{2t}{T} dt$$

$$= \frac{8}{T^2} \int_0^{T/2} t dt$$

$$= \frac{8}{T^2} \left[\frac{t^2}{2} \right]_0^{T/2} = \frac{8}{T^2} \left[\frac{T^2}{8} - 0 \right]$$

$$a_0 = 1$$

(4)

Find a_n

$$a_n = \frac{4}{T} \int_0^{T/2} x(t) \cos n\Omega t dt$$

$$a_n = \frac{4}{T} \int_0^{T/2} \frac{2t}{T} \cos n\Omega t dt$$

$$a_n = \frac{8}{T^2} \int_0^{T/2} t \cos n\Omega t dt$$

$\int u dv = uv - \int v du$
$u = t \quad du = 1$
$dv = \cos n\Omega dt \quad v = \frac{\sin n\Omega t}{n^2}$

$$= \frac{8}{T^2} \left[\frac{t \sin n\Omega t}{n\Omega} - \int \left(\frac{\sin n\Omega t}{n\Omega} \right) dt \right]_0^{T/2}$$

$$= \frac{8}{T^2} \left[\frac{t \sin n\Omega t}{n\Omega} - \left(\frac{-\cos n\Omega t}{n^2\Omega^2} \right) dt \right]_0^{T/2} \quad \Omega = \frac{2\pi}{T}$$

$$= \frac{8}{T^2} \left[\frac{t \sin n\frac{2\pi}{T}t}{n\frac{2\pi}{T}} + \left(\frac{\cos n\frac{2\pi}{T}t}{n^2\left(\frac{2\pi}{T}\right)^2} \right) dt \right]_0^{T/2}$$

(4)

for even integer values of n, $\cos n\pi = 1$ for odd integer values of n, $\cos n\pi = -1$
 $a_n = 0$; for even values of n

Fourier series equation

The trigonometric form Fourier series of x(t) is,

$$x(t) = \frac{a_0}{2} + \sum_{n=1}^{\infty} a_n \cos n\Omega t + \sum_{n=1}^{\infty} b_n \sin n\Omega t$$

here $b_n = 0$ and a_n exists only for odd values of n

$$x(t) = \frac{a_0}{2} + \sum_{n=1}^{\infty} a_n \cos n\Omega t$$

$$x(t) = \frac{1}{2} + \frac{2}{n^2\pi^2} [\cos n\pi - 1]$$

(4)

3

State and prove any four properties of Fourier Transform (15)[Nov 2015/R13

Let, Fourier transform of $x_1(t) = X_1(j\Omega)$ Let, Fourier transform of $x_2(t) = X_2(j\Omega)$

The linearity property of Fourier transform says that,

$$\text{Fourier transform of } \{a x_1(t) + b x_2(t)\} = a X_1(j\Omega) + b X_2(j\Omega)$$

Proof

By definition of Fourier transform

$$X_1(j\Omega) = \int_{-\infty}^{\infty} x_1(t) e^{-j\Omega t} dt$$

$$X_2(j\Omega) = \int_{-\infty}^{\infty} x_2(t) e^{-j\Omega t} dt$$

Consider the linear combination,

$a_1 x_1(t) + a_2 x_2(t)$. on taking Fourier transform of this signal,

$$F \{ a_1 x_1(t) + a_2 x_2(t) \} = \int_{-\infty}^{\infty} [a_1 x_1(t) + a_2 x_2(t)] e^{-j\Omega t} dt$$

$$= \int_{-\infty}^{\infty} a_1 x_1(t) e^{-j\Omega t} dt + \int_{-\infty}^{\infty} a_2 x_2(t) e^{-j\Omega t} dt$$

$$= a_1 \int_{-\infty}^{\infty} x_1(t) e^{-j\Omega t} dt + a_2 \int_{-\infty}^{\infty} x_2(t) e^{-j\Omega t} dt$$

$$F \{ a_1 x_1(t) + a_2 x_2(t) \} = a_1 X_1(j\Omega) + a_2 X_2(j\Omega) \quad (4)$$

Time shifting

The shifting property of Fourier transform says that, If $F \{ x(t) \} = X(j\Omega)$

$$F \{ x(t-t_0) \} = e^{-j\Omega t_0} X(j\Omega)$$

Proof

By definition of Fourier transform,

$$F \{ x(t) \} = X(j\Omega) = \int_{-\infty}^{\infty} x(t) e^{-j\Omega t} dt$$

$$F \{ x(t-t_0) \} = \int_{-\infty}^{\infty} x(t-t_0) e^{-j\Omega t} dt$$

(3)

$$= \int_{-\infty}^{\infty} x(\tau) e^{-j\Omega(\tau+t_0)} d\tau \quad \text{let } t-t_0 = \tau$$

$$= \int_{-\infty}^{\infty} x(\tau) e^{-j\Omega\tau} e^{-j\Omega t_0} d\tau \quad t = \tau + t_0 \text{ on}$$

differentiating

$$= e^{-j\Omega t_0} \int_{-\infty}^{\infty} x(\tau) e^{-j\Omega\tau} d\tau \quad dt = d\tau$$

$$= e^{-j\Omega t_0} \int_{-\infty}^{\infty} x(t) e^{-j\Omega t} dt$$

$$F \{ x(t-t_0) \} = e^{-j\Omega t_0} X(j\Omega) \quad (4)$$

Time scaling

The time scaling property of Fourier transform says that, If $F \{ x(t) \} = X(j\Omega)$ then

Proof

By definition of Fourier transform,

$$X(j\Omega) = \int_{-\infty}^{\infty} x(t) e^{-j\Omega t} dt$$

$$F \{ x(at) \} = \int_{-\infty}^{\infty} x(at) e^{-j\Omega t} dt$$

$$= \int_{-\infty}^{\infty} x(\tau) e^{-\frac{j\tau\Omega}{a}} \frac{d\tau}{a} \quad \text{at} = \tau$$

$$= \frac{1}{a} \int_{-\infty}^{\infty} x(\tau) e^{-\frac{j\tau\Omega}{a}} d\tau \quad t = \tau/a, dt = d\tau/a$$

$$F\{x(at)\} = \frac{1}{|a|} X\left(\frac{j\Omega}{a}\right) \text{ hence it is proved.}$$

(3)

Time reversal

The time reversal property Fourier transform says that,

$$F\{x(t)\} = X(j\Omega)$$

$$F\{x(-t)\} = X(-j\Omega)$$

Proof

Form the time scaling property,

Proof

Form the time scaling property,

$$F\{x(at)\} = \frac{1}{|a|} X\left(\frac{j\Omega}{a}\right)$$

$$\text{Let } a = -1$$

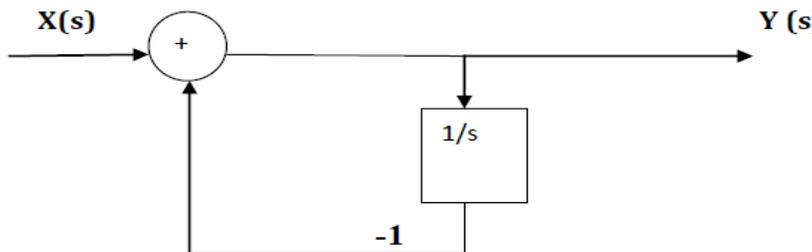
$$F\{x(-t)\} = X(-j\Omega)$$

(4)

UNIT III- LINEAR TIME INVARIANT CONTINUOUS TIME SYSTEMS	
Impulse response - convolution integrals- Differential Equation- Fourier and Laplace transforms in Analysis of CT systems - Systems connected in series / parallel.	
PART A	
Q.No	Questions
1	<p>Check whether the given system is stable and causal? (May 2019)-BTL4</p> $h(t) = e^{-4t} u(t + 10)$ <p>Solution,</p> <p>$u(t + 10) = 1$ for $t \geq -10$</p> <p>$h(t) = e^{-4t}$ for $t \geq -10$</p> <p>$h(t) \neq 0$ for $t < 0$, is is non-causal.</p> $\int_{-\infty}^{\infty} h(t) dt = \int_{-\infty}^{\infty} e^{-4t} u(t + 10) dt$ <p>$u(t + 10) = 1$ for $t \geq -10$</p> $\int_{-\infty}^{\infty} h(t) dt = \int_{-10}^{\infty} e^{-4t} dt$ <p>Integrating above equation,</p> $= \frac{1}{4} e^{-4t} < \infty, \text{ the system is stable.}$
2	<p>State Dirichlet's condition for Region of Convergence. (May 2019)-BTL1</p> <ul style="list-style-type: none"> $x(t)$ is absolutely integrable, $\int_{-\infty}^{\infty} x(t) dt < \infty$ <ul style="list-style-type: none"> $x(t)$ has finite number of maxima and minima within any finite interval. $x(t)$ has finite number of discontinuities within any finite interval, and each of the discontinuities must be finite.
3	<p>Find the impulse response $h(t)$. (NOV 2018)-BTL2</p> $H(s) = 4 - \frac{3}{s+2}; \text{Re}(s) > -2,$

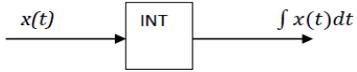
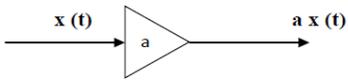
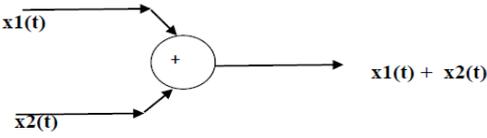
	<p>Solution,</p> <p>Given that,</p> $H(s) = 4 - \frac{3}{s+2}$ <p>Take inverse Laplace transform,</p> $h(t) = 4 \delta(t) - 3 e^{-2t} u(t)$
4	<p>Two systems with impulse response $h_1(t)$ and $h_2(t)$ are connected in series. What is the overall impulse response $h(t)$ of the system?(Nov 2018)-BTL2</p> <p>$h_1(t) = e^{-2t} u(t)$</p> <p>$h_2(t) = \delta(t - 1)$</p> <p>The diagram shows two block diagrams. The first block diagram shows an input signal $x(t)$ entering a block labeled $h_1(t) = e^{-2t} u(t)$. The output of this block enters a second block labeled $h_2(t) = \delta(t - 1)$. The output of the second block is the overall response. The second block diagram shows an input signal $x(t)$ entering a single block labeled $h_1(t) * h_2(t)$, with the output labeled $y(t)$.</p>
5	<p>Will there be two different signals having same Laplace Transform? Give an examples. How do you differentiate these two signals?(Nov 2017) –BTL4</p> <p>Yes, two different signals have the same Laplace transform,</p> <p>Examples, $u(t)=1/s$</p> <p>$u(-t) = 1/s$</p>
6	<p>Find impulse response of a LTI system with transfer function $H(s)$ is given by,(Nov 2017)-BTL2</p> $H(s) = \frac{1}{(s+1)(s+3)}$ <p>Solution</p> <p>By partial fraction expansion technique,</p> $H(s) = \frac{1}{(s+1)(s+3)} = \frac{A}{(s+1)} + \frac{B}{(s+3)}$ <p>If $s = -1$ $A = 1/2$</p> <p>If $s = -3$ $B = -1/2$</p> <p>Taking inverse Laplace transforms,</p>

	$h(t) = \frac{1}{2} e^{-t} u(t) - \frac{1}{2} e^{-3t} u(t)$
7.	<p>Give the expression for convolution integral. [May 2017] -BTL2</p> <p>The convolution of two continuous time signals $x_1(t)$ and $x_2(t)$ is defined as,</p> $x_3(t) = \int_{-\infty}^{\infty} x_1(\lambda) x_2(t-\lambda)$ <p>Where,</p> <p>$x_3(t)$ is the signal obtained by convolving $x_1(t)$ and $x_2(t)$ λ is a dummy variable used for integration.</p> <p>Symbol * indicates convolution operation.</p>
8.	<p>Given $h(t)$, what is the step response of a CT LTI system [May 2017] -BTL1</p> <p>Input and output of an LTI system are related by,</p> $y(t) = \int_{-\infty}^{\infty} x(\tau) h(t-\tau)$ <p>It is a convolution. where,</p> <p>$x(\tau)$ is the input variable function</p> <p>$h(t-\tau)$ is the delay impulse response</p>
9	<p>Convolve the following signal $u(t-1)$ and $\delta(t-1)$ [May 2018], [Nov 2016]- BTL2</p> <p>$x_1(t) = u(t-1)$</p> <p>$x_2(t) = \delta(t-1)$ Using convolution,</p> <p>$x_1(t) * x_2(t) = u(t-1) * \delta(t-1)$</p> <p>$= u(t-1-1)$ {hint: $\delta(t-t_0) * x(t) = x(t-t_0)$}</p> <p>$= u(t-2)$</p>
10	<p>Find the differential equation representation for the signal. [Nov 2016] -BTL3</p> $H(s) = \frac{1}{s^2 + 2s + 1}$ <p>Solution</p> <p>Given that,</p> $H(S) = \frac{1}{(s)^2 + 2s + 1}$ $\frac{Y(s)}{X(s)} = \frac{1}{(s)^2 + 2s + 1}$ <p>On cross multiplying the above equation, $(s)^2 Y(s) + 2s Y(s) + Y(s) = X(s)$</p> <p>On taking inverse Laplace Transform of the above equation,</p> $\frac{d^2}{dt^2} y(t) + 2 \frac{d y(t)}{dt} + y(t) = x(t)$

11	<p>Find whether the following system whose impulse response is given Causal and stable $h(t) = e^{-2t} u(t-1)$ [May 2016] -BTL4</p> <p>Given that, $h(t) = e^{-2t} u(t)$</p> <p>The condition for causality is given by,</p> <p>$h(t) = 0$ for $t < 0$</p> <p>$h(t) = e^{-2t}$, $t \geq 0$</p> <p>$0, t < 0$</p> <p>Therefore the condition is satisfied. Hence the system is causal.</p>
12	<p>Realize the block diagram representing the system (May 2016, 2018)-BTL2</p> <p>$H(s) = \frac{s}{s+1}$</p> <p>Solution</p> 
13	<p>What is $u(t-2) * f(t-1)$? Where * represents convolution. [Nov 2015] -BTL2</p> <p>$x_1(t) = u(t-2)$</p> <p>$x_2(t) = \delta(t-1)$ Using convolution,</p> <p>$x_1(t) * x_2(t) = u(t-2) * \delta(t-1)$</p> <p>$= u(t-2-1)$ {hint: $\delta(t-t_0) * x(t) = x(t-t_0)$}</p> <p>$= u(t-3)$</p>
14	<p>Given the differential equation representation of a System $\frac{d^2 y(t)}{dt^2} + 2 \frac{dy(t)}{dt} - 3 y(t) = 2 x(t)$.</p> <p>Find the frequency response $H(j\Omega)$. [Nov 2015] -BTL2</p> <p>Given that, $\frac{d^2 y(t)}{dt^2} + 2 \frac{dy(t)}{dt} - 3 y(t) = 2 x(t)$</p> <p>Taking Fourier Transform of the above equation, $(j\Omega)^2 Y(j\Omega) + 2 j\Omega Y(j\Omega) - 3 Y(j\Omega) = 2 X(j\Omega)$</p> <p>$Y(j\Omega) [(j\Omega)^2 + 2 j\Omega - 3] = 2 X(j\Omega)$</p>

	$\frac{Y(j\Omega)}{X(j\Omega)} = \frac{2}{(j\Omega)^2 + 2j\Omega - 3}$ <p>Frequency response,</p> $H(j\Omega) = \frac{2}{(j\Omega + 3)(j\Omega - 1)}$
15	<p>Given $x(t) = \delta(t)$. Find $X(s)$ and $X(\omega)$. [May 2015] -BTL3</p> <p>Solution</p> <p>It is defined as</p> $x(t) = \delta(t) = \begin{cases} 1; & t = 0 \\ 0; & t \neq 0 \end{cases}$ <p>$X(s)$ and $X(\omega) = 1$</p>
16	<p>State convolution integral. [May 2015], May 2013, 2015-BTL1</p> <p>The convolution of two continuous time signals $x_1(t)$ and $x_2(t)$ is defined as,</p> $x_3(t) = \int_{-\infty}^{\infty} x_1(\lambda) x_2(t-\lambda)$ <p>Where,</p> <p>$x_3(t)$ is the signal obtained by convolving $x_1(t)$ and $x_2(t)$ λ is a dummy variable used for integration.</p> <p>Symbol * indicates convolution operation.</p>
17	<p>Draw the block diagram of the LTI system described By [No 2014] -BTL2</p> <p>$\frac{dy(t)}{dt} + y(t) = 0.1x(t)$.</p> <p>Solution</p> <p>$sY(s) + Y(s) = 0.1X(s)$</p>
18	<p>Find $y(n) = x(n-1) * \delta(n-2)$. [Nov 2014] -BTL3</p> <p>Solution</p> <p>Given that, $y(n) = x(n-1) * \delta(n-2)$</p> $= \sum_{-\infty}^{\infty} x(m-1) \delta(n-m+2)$

	$= x(m - 1\delta(n - m + 2))$ $= x(n+2-1)$ $= x(n+1)$
19	<p>State the necessary and sufficient condition for an LTI CT system to be causal. [May 2014, 2015] -BTL1</p> <p>A system said to be causal if the output of the system at any time 't' depends only on the present input, past inputs and past outputs but does not depend on the future inputs and outputs. If the system output at any time t depends on future inputs or outputs then the system is called a non-causal.</p>
20	<p>List the properties of convolution integral. [Nov 2014]- BTL1</p> <p>The convolution of continuous time signals will satisfy the following properties,</p> <p>Commutative property: $x_1(t) * x_2(t) = x_2(t) * x_1(t)$</p> <p>Associative property: $[x_1(t) * x_2(t)] * x_3(t) = x_1(t) * [x_2(t) * x_3(t)]$</p> <p>Distributive property: $x_1(t) * [x_2(t) + x_3(t)] = [x_1(t) * x_2(t)] + [x_1(t) * x_3(t)]$</p>
21	<p>State the significance of impulse response. [Nov 2014]- BTL1</p> <p>let, $x(t)$ = input of a LTI CT system $y(t)$ = output of the LTI CT system for the input $x(t)$ $h(t)$ = Impulse response now, the response $y(t)$ of the CT system is given by convolution of input and impulse response.</p> $y(t) = x(t) * h(t) = \int_{-\infty}^{\infty} x(\lambda)h(t - \lambda)d\lambda$ <p>When the input to a continuous time system is a unit impulse signal $\delta(t)$ then the output is called an impulse response of the system and it is denoted by $h(t)$.</p> <p>Impulse response, $h(t) = \delta(t)$</p> <div style="text-align: center;"> <p>Impulse input $\delta(t)$ impulse response $h(t)$</p> </div>
22	<p>Find the differential equation relating the input and output a CT System represented by [May 2014] -BTL3</p> $H(j\Omega) = \frac{4}{(j\Omega)^2 + 8j\Omega + 4}$ <p>Given that, $H(j\Omega) = \frac{4}{(j\Omega)^2 + 8j\Omega + 4}$</p> $\frac{Y(j\Omega)}{X(j\Omega)} = \frac{4}{(j\Omega)^2 + 8j\Omega + 4}$

	<p>On cross multiplying the above equation, $(j\Omega)^2 Y(j\Omega) + 8 j\Omega Y(j\Omega) + 4 Y(j\Omega) = 4 X(j\Omega)$ On taking inverse Fourier Transform of the above equation,</p> $\frac{d^2}{dt^2} y(t) + 8 \frac{d y(t)}{dt} + 4 y(t) = 4 x(t)$
<p>23</p>	<p>List and draw the basic elements for the block diagram Representation of the CT system. [Nov 2012, 2013] -BTL1</p> <p>Integrator</p>  <p>Constant Multiplier</p>  <p>Signal Adder</p> 
<p>24</p>	<p>What is the condition for a LTI system to be stable? [May 2013,2015]-BTL1</p> <p>For an LTI system, the condition for BIBO stability can be transformed to a condition on impulse response, h (t). For BIBO stability of an LTI continuous time system, the integral of impulse response should be finite.</p> $\int_{-\infty}^{\infty} h(t) dt < \infty$
<p>25</p>	<p>What is the relationship between input and output of an LTI system?(or) What are the conditions for a system to be LTI system? -BTL1</p> <p>Input and output of an LTI system are related by,</p> $y(t) = \int_{-\infty}^{\infty} x(\tau) h(t - \tau)$ <p>It is a convolution.</p>
	<p>PART-B</p>
<p>Q.N o</p>	<p>Questions</p>

1.	<p>A causal LTI system having a frequency response $H(j\Omega) = 1/(j\Omega+3)$ is producing an output $y(t) = e^{-3t} u(t) - e^{-4t} u(t)$ for a particular input $x(t)$. Determine $x(t)$. (13M) [May 2017] -BTL3</p> <p>Solution Given that,</p> $H(j\Omega) = \frac{1}{j\Omega+3}$ <p>$y(t) = e^{-3t} u(t) - e^{-4t} u(t)$ Determine $x(t)$ $y(t) = e^{-3t} u(t) - e^{-4t} u(t)$ Taking Fourier transform of above equation,</p> $Y(j\Omega) = \frac{1}{j\Omega+3} - \frac{1}{j\Omega+4}$ $x(t) = \frac{y(t)}{h(t)}$ $X(j\Omega) = \frac{Y(j\Omega)}{H(j\Omega)}$ <p style="text-align: right;">(5M)</p> $X(j\Omega) = \frac{\frac{1}{j\Omega+3} - \frac{1}{j\Omega+4}}{\frac{1}{j\Omega+3}}$ $X(j\Omega) = \frac{j\Omega+4 - j\Omega-3}{(j\Omega+3)(j\Omega+4)} \cdot \frac{1}{j\Omega+3}$ $X(j\Omega) = \frac{1}{(j\Omega+4)}$ <p style="text-align: right;">(5M)</p> <p>Taking inverse Fourier transform $x(t) = e^{-4t} u(t)$ (3M)</p>
2	<p>Realize the given system in parallel form (13M) [May 2017] -BTL3</p> $H(s) = \frac{s(s+2)}{s^3+8s^2+19s+12}$ <p>Solution</p>

Given that,

$$H(s) = \frac{s(s+2)}{s^3+8s^2+19s+12}$$

Factorize the above equation

$$H(s) = \frac{s(s+2)}{(s+1)(s+3)(s+4)}$$

By partial fraction expansion technique,

$$H(s) = \frac{s(s+2)}{(s+1)(s+3)(s+4)} = \frac{A}{(s+1)} + \frac{B}{(s+3)} + \frac{C}{(s+4)}$$

$$\text{if } s = -1 \quad A = -1/6$$

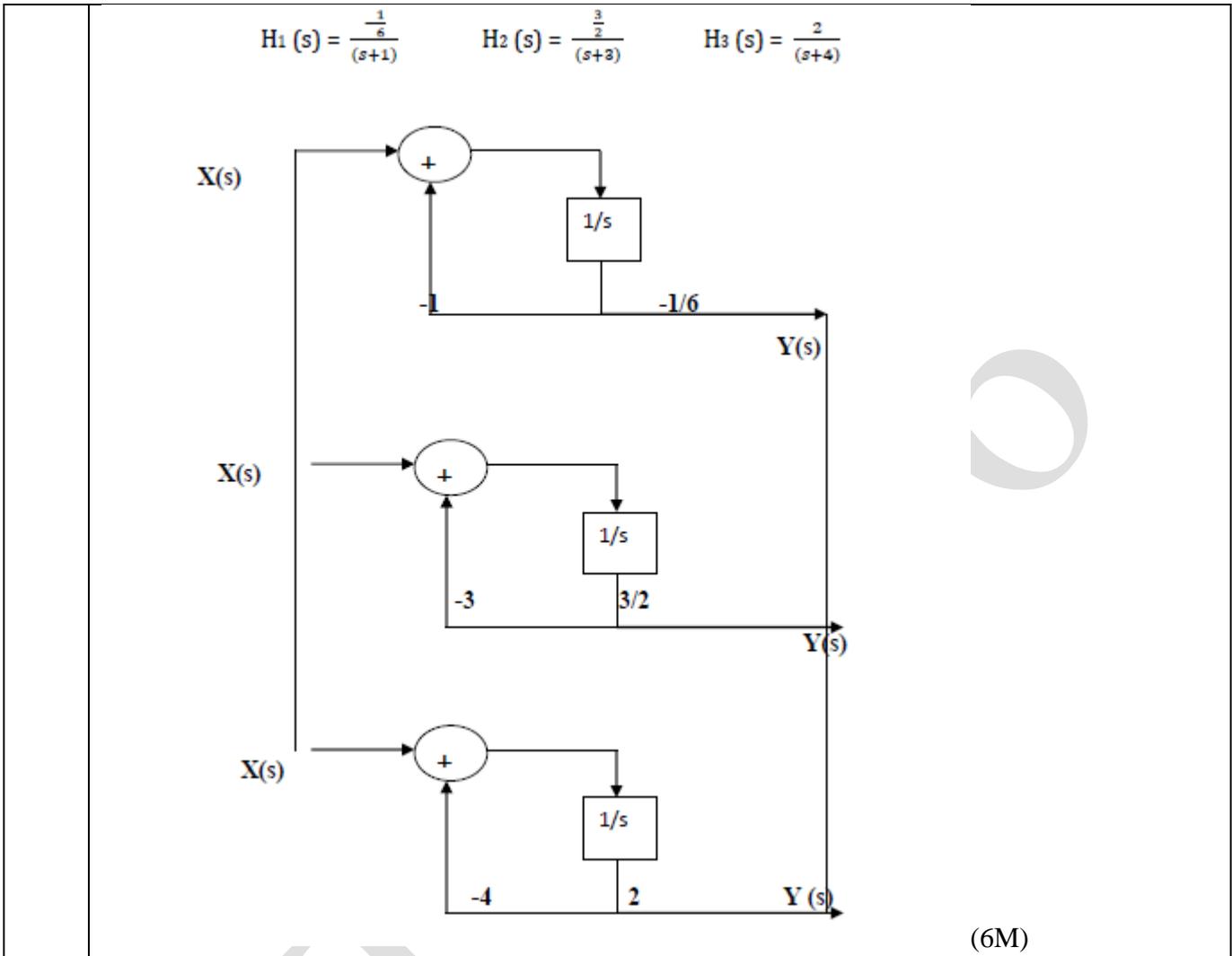
$$\text{if } s = -3 \quad B = -3/2$$

$$\text{if } s = -4 \quad C = 2$$

(7M)

$$H(s) = \frac{-\frac{1}{6}}{(s+1)} - \frac{\frac{3}{2}}{(s+3)} + \frac{2}{(s+4)}$$

Parallel form



Convolution of the following two signals:

$x(t) = e^{-3t} u(t)$ and $h(t) = u(t+3)$

(16M)[Nov 2016] -BTL3

Solution

Given that, $x(t) = e^{-3t} u(t)$ and $h(t) = u(t+3)$

3

Let, $y(t) = x(t) * h(t)$

(4M)

By definition of convolution,

$$y(t) = \int_{\lambda=-3}^{\lambda=t} x(\lambda) h(t-\lambda) d\lambda$$

	$y(t) = \int_{\lambda=-3}^{\lambda=t} e^{-3\lambda} e^{-3(t-\lambda)} d\lambda$ $y(t) = \int_{\lambda=-3}^{\lambda=t} e^{-3\lambda} e^{-3t} e^{3\lambda} d\lambda$ $y(t) = e^{-3t} \int_{\lambda=-3}^{\lambda=t} e^{-3\lambda} e^{3\lambda} d\lambda \quad (6M)$ $= e^{-3t} \int_{\lambda=-3}^{\lambda=t} e^{-3\lambda+3\lambda} d\lambda$ $= e^{-3t} \int_{\lambda=-3}^{\lambda=t} d\lambda$ $= e^{-3t} [\lambda]_{-3}^t$ $= e^{-3t} u(t-3); t \geq -3$ $y(t) = e^{-3t} u(t+3) u(t+3)$
4	<p>A system is described by the differential equation</p> $\frac{d^2}{dt^2} y(t) + 6 \frac{dy(t)}{dt} + 8 y(t) = \frac{dx(t)}{dt} + x(t).$ <p>Find the transfer function and the Output signal $y(t)$ for $x(t) = \delta(t)$. (16M)[Nov 2016]-BTL3</p> <p>Solution on taking the Laplace transform of the above equation</p> $s^2 Y(s) + 6s Y(s) + 8 Y(s) = s X(s) + X(s)$ $Y(s) [s^2 + 6s + 8] = X(s) [s + 1]$

$$H(s) = \frac{Y(s)}{X(s)}$$

$$H(s) = \frac{s+1}{s^2+6s+8}$$

$$H(s) = \frac{s+1}{(s+2)(s+4)}$$

(6M)

By partial fraction expansion technique,

$$H(s) = \frac{s+1}{(s+2)(s+4)} = \frac{A}{s+2} + \frac{B}{s+4}$$

$$\text{If } s = -2 \quad A = -1/2$$

$$\text{If } s = -4 \quad B = 3/2$$

Taking inverse Laplace transforms,

$$h(t) = \frac{-1}{2} e^{-2t} u(t) + \frac{3}{2} e^{-4t} u(t)$$

Response of the system

$$x(t) = \delta(t)$$

$$X(s) = 1$$

$$Y(s) = X(s) H(s)$$

$$Y(s) = \frac{s+1}{(s+2)(s+4)}$$

$$Y(s) = X(s) H(s)$$

(5M)

$$Y(s) = \frac{s+1}{(s+2)(s+4)}$$

By partial fraction expansion technique,

$$H(s) = \frac{s+1}{(s+2)(s+4)} = \frac{A}{s+2} + \frac{B}{s+4}$$

$$\text{If } s = -2 \quad A = -1/2$$

$$\text{If } s = -4 \quad B = 3/2$$

$$Y(s) = \frac{-1}{2} \frac{1}{s+2} + \frac{3}{2} \frac{1}{s+4}$$

Taking inverse Laplace transforms,

$$y(t) = \frac{-1}{2} e^{-2t} u(t) + \frac{3}{2} e^{-4t} u(t)$$

(5M)

Solve the differential equation $(D^2 + 5D + 4) y(t) = D x(t)$ using the input $x(t) = e^{-2t}$ and with initial condition $y(0) = 0$ and $y'(0) = 1$ (10 marks) [May 2015] R13, Nov 2011, Nov 2014-BTL5

Solution

Given that, $(D^2 + 5D + 4) y(t) = D x(t)$

Input $x(t) = e^{-2t}$

Taking the inverse Laplace transform

$$X(s) = \frac{1}{s+2} \quad \text{At initial condition input } x(t) = 0$$

The given system equation is,

$$\frac{d^2 y(t)}{dt^2} + 5 \frac{dy(t)}{dt} + 4y(t) = \frac{d}{dt} x(t)$$

Taking Laplace transform of the above equation,

$$s^2 Y(s) - s y(0) - y'(0) + 5[s Y(s) - y(0)] + 4 Y(s) = s X(s) - x(0)$$

Substituting initial values,

$$s^2 Y(s) - s(0) - 1 + 5[s Y(s) - 0] + 4 Y(s) = s X(s) - 1$$

$$s^2 Y(s) + 5 s Y(s) + 4 Y(s) = s X(s)$$

$$(s^2 + 5s + 4) Y(s) = \frac{s}{s+2}$$

$$Y(s) = \frac{s}{(s+2)(s^2+5s+4)}$$

$$Y(s) = \frac{s}{(s+2)(s+1)(s+4)}$$

(5)

5

$$Y(s) = \frac{s}{(s+1)(s+2)(s+4)}$$

By partial fraction expansion technique,

$$Y(s) = \frac{s}{(s+1)(s+2)(s+4)} = \frac{A}{(s+1)} + \frac{B}{(s+2)} + \frac{C}{(s+4)}$$

$$\text{If } s = -1 \quad A = -1/3$$

$$\text{If } s = -2 \quad B = 1$$

$$\text{If } s = -4 \quad C = -2/3$$

$$Y(s) = \frac{-\frac{1}{3}}{(s+1)} + \frac{1}{(s+2)} - \frac{\frac{2}{3}}{(s+4)}$$

Taking inverse Laplace transforms,

$$y(t) = \frac{-1}{3} e^{-t}u(t) + e^{-2t}u(t) - \frac{2}{3} e^{-4t}u(t) \quad (5M)$$

Draw the block diagram representation for

$$H(s) = \frac{4s+28}{s^2+6s+5}$$

(6M)[May 2015]-BTL2

Solution Direct form – I

Given that,

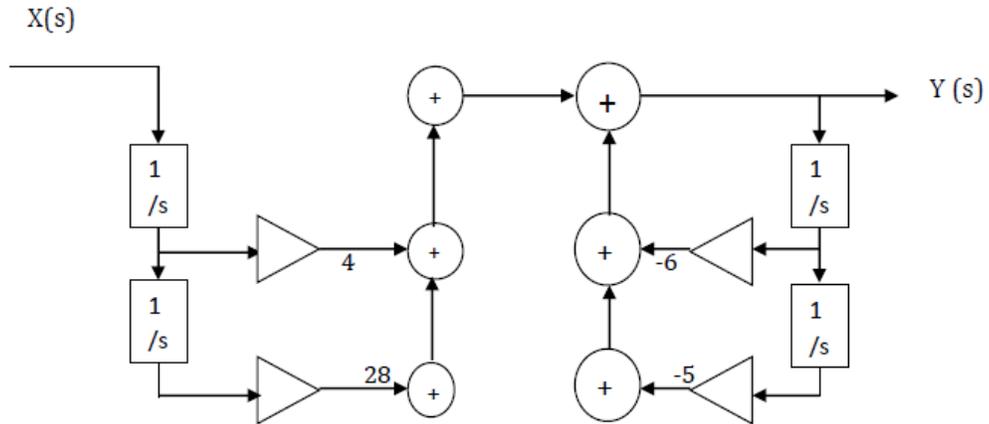
$$H(s) = \frac{Y(s)}{X(s)} = \frac{4s+28}{s^2+6s+5}$$

$$H(s) = \frac{s^2\left(\frac{4}{s} + \frac{28}{s}\right)}{s^2\left(1 + \frac{6}{s} + \frac{5}{s^2}\right)}$$

$$H(s) = \frac{\left(\frac{4}{s} + \frac{28}{s}\right)}{\left(1 + \frac{6}{s} + \frac{5}{s^2}\right)}$$

(3M)

Diagram



(3M)

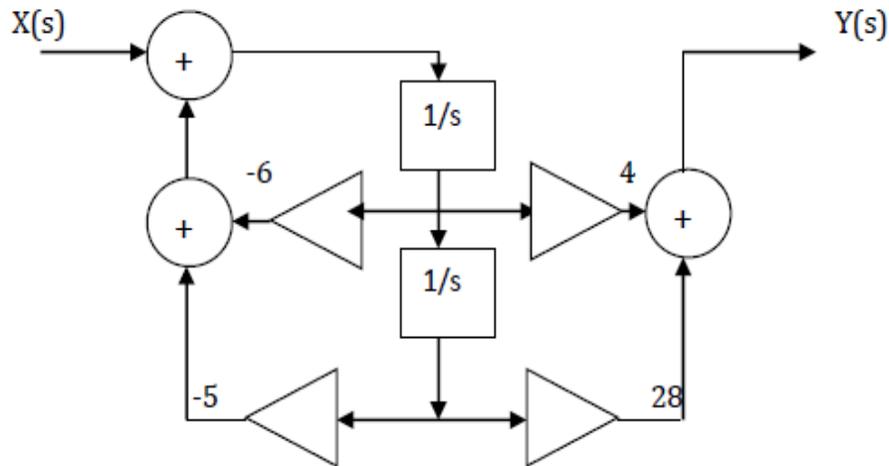
Direct form - II

Given that, $H(s) = \frac{4s+28}{s^2+6s+5}$

$$H(s) = \frac{Y(s)}{X(s)} = \frac{4s+28}{s^2+6s+5}$$

$$H(s) = \frac{s^2\left(\frac{4}{s} + \frac{28}{s}\right)}{s^2\left(1 + \frac{6}{s} + \frac{5}{s^2}\right)}$$

$$H(s) = \frac{\left(\frac{4}{s} + \frac{28}{s}\right)}{\left(1 + \frac{6}{s} + \frac{5}{s^2}\right)}$$



Using graphical representation, find the response of the system whose Impulse response is, $h(t) = e^{-2t} u(t)$ for an input, (8 Marks) [May 2016] -BTL3

Solution

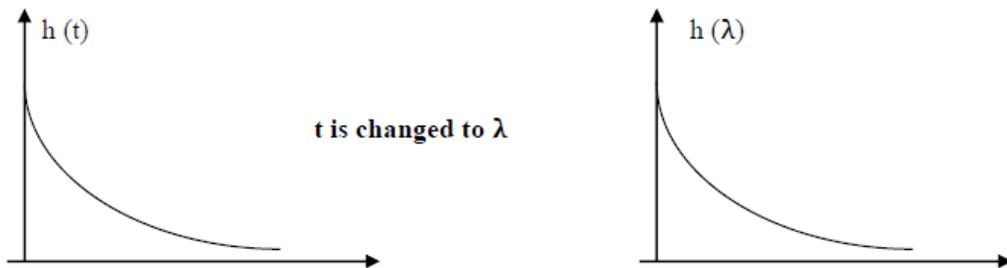
Given that, $h(t) = e^{-2t} u(t)$

$$x(t) = \begin{cases} A, & \text{for } 0 \leq t \leq 2 \\ 0, & \text{otherwise} \end{cases}$$

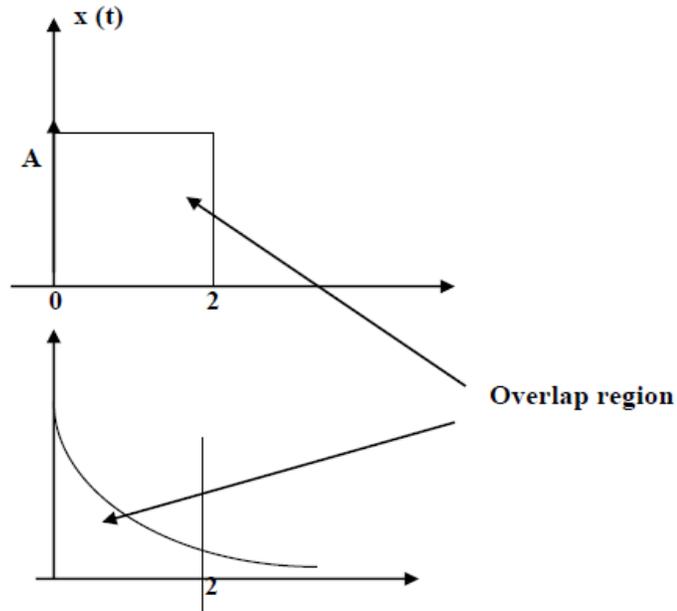
$$y(t) = x(t) * h(t)$$

$$y(t) = \int_{\lambda=-\infty}^{\lambda=\infty} x(\lambda)h(t - \lambda)d\lambda$$

(2M)



(3M)



(3M)

7

8 Realize the following is indirect form II. (8 marks) [May 2016] -BTL6

$$\frac{d^3y(t)}{dt^3} + 4\frac{d^2}{dt^2}y(t) + 7\frac{dy(t)}{dt} + 8y(t) = 5\frac{d^2x(t)}{dt^2} + 4\frac{dx(t)}{dt} + 7x(t).$$

Solution

Given that, $\frac{d^3y(t)}{dt^3} + 4\frac{d^2}{dt^2}y(t) + 7\frac{dy(t)}{dt} + 8y(t) = 5\frac{d^2x(t)}{dt^2} + 4\frac{dx(t)}{dt} + 7x(t).$

on taking Laplace transform of the above equation,

$$s^3 Y(s) + 4s^2 Y(s) + 7s Y(s) + 8Y(s) = 5s^2 X(s) + 4s X(s) + 7X(s)$$

$$Y(s) [s^3 + 4s^2 + 7s + 8] = X(s) [5s^2 + 4s + 7]$$

$$H(s) = \frac{Y(s)}{X(s)} \quad (3M)$$

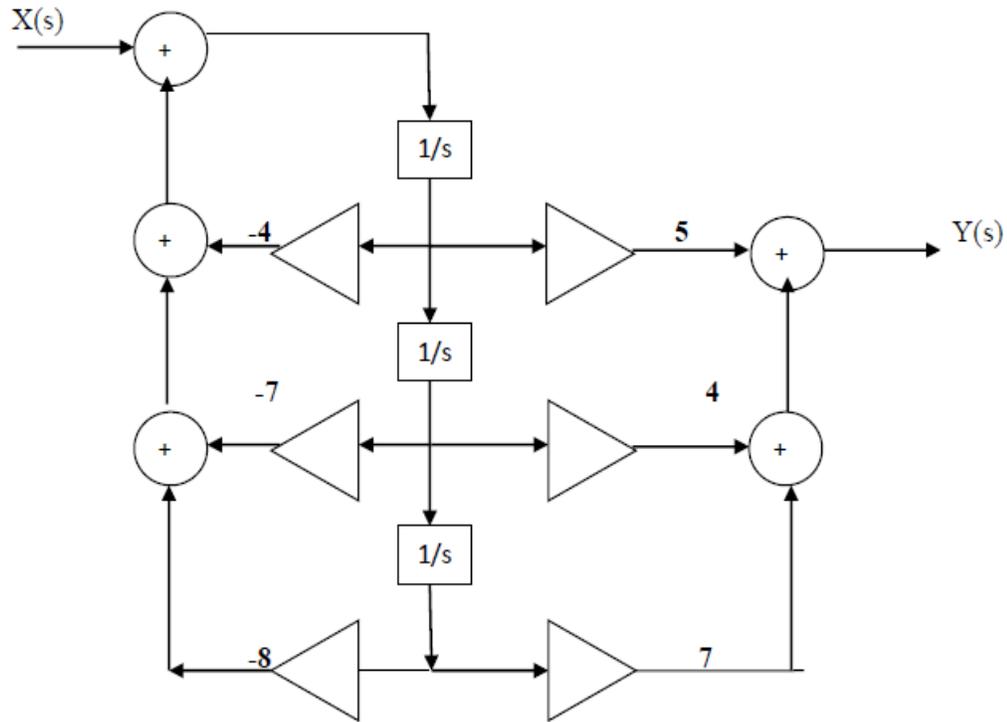
$$H(s) = \frac{5s^2 + 4s + 7}{s^3 + 4s^2 + 7s + 8}$$

on dividing both side s^3 we get

$$H(s) = \frac{\frac{5}{s} + \frac{4}{s^2} + \frac{7}{s^3}}{1 + \frac{4}{s} + \frac{7}{s^2} + \frac{8}{s^3}}$$

(2M)

Direct form – II



(3M)

Determine frequency response and impulse response for the system described by the following differential equation. Assume zero initial conditions. (6 Marks) [May 2016]-BTL3

$$\frac{dy(t)}{dt} + 3y(t) = x(t).$$

Solution

Given that, $\frac{dy(t)}{dt} + 3y(t) = x(t).$

On taking the Laplace transform for above equation,

$$s Y(s) + 3 Y(s) = X(s)$$

$$Y(s) [s + 3] = X(s)$$

$$H(s) = \frac{Y(s)}{X(s)}$$

$$H(s) = \frac{1}{s+3}$$

(3M)

	<p>Frequency response</p> $H(s) = \frac{1}{s+3}$ <p>Put $s = j\Omega$</p> $H(j\Omega) = \frac{1}{j\Omega+3}$ <p>This is called frequency response. (3M)</p> <p>Impulse response</p> $H(j\Omega) = \frac{1}{j\Omega+3}$ <p>Taking inverse Fourier transform we get,</p> $\mathbf{h(t) = e^{-3t} u(t)}$
10	<p>Convolve the following signals $x(t) = e^{-2t}u(t-2)$ and $h(t) = e^{-2t}u(t)$ (16 marks) [Nov 2015] May 2010-BTL3</p> <p>Solution</p> <p>Given that, $x(t) = e^{-2t}u(t-2)$ and $h(t) = e^{-2t}u(t)$</p> <p>Let, $y(t) = x(t) * h(t)$</p> <p>By definition of convolution,</p> $y(t) = \int_{\lambda=2}^{\lambda=t} x_1(\lambda)x_2(t-\lambda)d\lambda$ $y(t) = \int_{\lambda=2}^{\lambda=t} e^{-2\lambda}e^{-2(t-\lambda)}d\lambda$ $y(t) = \int_{\lambda=2}^{\lambda=t} e^{-2\lambda}e^{-2t}e^{2\lambda}d\lambda$ $y(t) = e^{-2t} \int_{\lambda=2}^{\lambda=t} e^{-2\lambda}e^{2\lambda}d\lambda$ $= e^{-2t} \int_{\lambda=2}^{\lambda=t} e^{-2\lambda+2\lambda}d\lambda$ <p style="text-align: right;">(6M)</p>

	$= e^{-2t} \int_{\lambda=2}^{\lambda=t} d\lambda$ $= e^{-2t} [\lambda]_2^t$ $= e^{-2t} u(t - 2); t \geq 2$ $y(t) = e^{-2t} u(t - 2) u(t - 2) \quad (4M)$
11	<p>Define convolution integral and derive its equation (8 marks) (Nov 2013)</p> <p>What is impulse response? Show that the response of an LTI system is convolution integral of its impulse response with input signal? (Nov 2012) –BTL1</p> <p>Solution</p> <p>In an LTI continuous time system, the response $y(t)$ of the system for an arbitrary input $x(t)$ is given by convolution of input $x(t)$ with impulse response $h(t)$ of the system. It is expressed as,</p> $y(t) = x(t) * h(t)$ $y(t) = \int_{-\infty}^{\infty} x(\lambda) h(t - \lambda) d\lambda$ <p>Where * represents convolution operation</p> <p>Proof (3M)</p> <p>Let $y(t)$ be the response of system H for an input $x(t)$</p> $y(t) = \int_{-\infty}^{\infty} x(\lambda) \delta(t - \lambda) d\lambda$ $y(t) = \int_{-\infty}^{\infty} H x(\lambda) \delta(t - \lambda) d\lambda$ $y(t) = \int_{-\infty}^{\infty} x(\lambda) H \{\delta(t - \lambda)\} d\lambda$ $y(t) = \int_{-\infty}^{\infty} x(\lambda) h(t - \lambda) d\lambda \quad (5M)$ <p>The above equation represents the convolution of input $x(t)$ with the impulse response $h(t)$ to yield the output $y(t)$.</p> <p>Hence it is proved that the response $y(t)$ of LTI continuous time system for an arbitrary input $x(t)$ is given by convolution of input $x(t)$ with impulse response $h(t)$ of the system.</p>

	PART-C
Q.No	Questions
1	<p>Using Laplace transform determine the response of the system described by the equation with initial conditions $y(0) = 0$; $dy(t)/dt = 1$ for the input $x(t) = e^{-2t} u(t)$. (15M)[May 2017] -BTL3</p> $\frac{d^2}{dt^2}y(t) + 5\frac{dy(t)}{dt} + 4y(t) = dx(t)/dt$ <p>Solution Taking the Laplace transform</p> $X(s) = \frac{1}{s+2}$ <p>At initial condition input $x(t) = 0$ The given system equation is,</p> $\frac{d^2y(t)}{dt^2} + 5\frac{dy(t)}{dt} + 4y(t) = \frac{d}{dt}x(t)$ $s^2 Y(s) - s y(0) - y'(0) + 5[s Y(s) - y(0)] + 4 Y(s) = s X(s) - x(0)$ <p>Substituting initial values,</p> $s^2 Y(s) - s(0) - 1 + 5[s Y(s) - 0] + 4 Y(s) = s X(s) - 1 \quad (4)$ $s^2 Y(s) + 5s Y(s) + 4 Y(s) = s X(s)$ $(s^2 + 5s + 4) Y(s) = \frac{s}{s+2}$ $Y(s) = \frac{s}{(s+2)(s^2+5s+4)}$ $Y(s) = \frac{s}{(s+2)(s+1)(s+4)}$ $Y(s) = \frac{s}{(s+1)(s+2)(s+4)}$ <p>By partial fraction expansion technique,</p> $Y(s) = \frac{s}{(s+1)(s+2)(s+4)} = \frac{A}{(s+1)} + \frac{B}{(s+2)} + \frac{C}{(s+4)}$ <p>If $s = -1$ $A = -1/3$ If $s = -2$ $B = 1$ If $s = -4$ $C = -2/3$ (8)</p> <p>Taking inverse Laplace transforms,</p> $Y(s) = \frac{-\frac{1}{3}}{(s+1)} + \frac{1}{(s+2)} - \frac{\frac{2}{3}}{(s+4)}$

$$y(t) = \frac{-1}{3}e^{-t}u(t) + e^{-2t}u(t) - \frac{2}{3}e^{-4t}u(t) \quad (3)$$

The input-output of a causal LTI system are related by the differential equation

$$\frac{d^2y(t)}{dt^2} + 6\frac{dy(t)}{dt} + 8y(t) = 2x(t)$$

- i. Find the impulse response $h(t)$
- ii. Find the response $y(t)$ of the system if $x(t) = u(t)$

Use Fourier transform(15 marks) [Nov 2015,] Nov 2012-BTL3

Solution

Given that,

$$\frac{d^2y(t)}{dt^2} + 6\frac{dy(t)}{dt} + 8y(t) = 2x(t)$$

Impulse response of the system

$$\frac{d^2y(t)}{dt^2} + 6\frac{dy(t)}{dt} + 8y(t) = 2x(t)$$

On taking Fourier transform of above equation we get,

$$(j\Omega)^2 Y(j\Omega) + 6(j\Omega) Y(j\Omega) + 8 Y(j\Omega) = 2 X(j\Omega)$$

$$Y(j\Omega) [(j\Omega)^2 + 6j\Omega + 8] = 2 X(j\Omega)$$

$$\frac{Y(j\Omega)}{X(j\Omega)} = \frac{2}{(j\Omega)^2 + 6j\Omega + 8}$$

Factorize the above form we get,

$$\frac{Y(j\Omega)}{X(j\Omega)} = \frac{2}{(j\Omega+2)(j\Omega+4)}$$

By partial fraction expansion technique,

$$H(j\Omega) = \frac{2}{(j\Omega+2)(j\Omega+4)} = \frac{A}{(j\Omega+2)} + \frac{B}{(j\Omega+4)}$$

$$\text{If } j\Omega = -2$$

$$A = 1$$

$$\text{If } j\Omega = -4$$

$$B = -1$$

(6M)

$$H(j\Omega) = \frac{1}{(j\Omega+2)} - \frac{1}{(j\Omega+4)}$$

On taking inverse Fourier transform,

$$h(t) = e^{-2t}u(t) - e^{-4t}u(t)$$

Response of the system

Given that, $x(t) = u(t)$

Taking inverse Fourier transform

$$X(j\Omega) = \frac{1}{j\Omega}$$

$$Y(j\Omega) = X(j\Omega) H(j\Omega)$$

$$Y(j\Omega) = X(j\Omega) \frac{2}{(j\Omega+2)(j\Omega+4)} = \frac{1}{j\Omega} \frac{2}{(j\Omega+2)(j\Omega+4)}$$

By partial fraction expansion technique,

$$Y(j\Omega) = \frac{A}{j\Omega} + \frac{B}{(j\Omega+2)} + \frac{C}{(j\Omega+4)}$$

$$\text{If } j\Omega = 0$$

$$A = 0.25$$

$$\text{If } j\Omega = -2$$

$$B = -0.5$$

$$\text{If } j\Omega = -4$$

$$C = 0.25$$

(4M)

$$Y(j\Omega) = \frac{0.25}{j\Omega} - \frac{0.5}{(j\Omega+2)} + \frac{0.25}{(j\Omega+4)}$$

By taking inverse Fourier transform

$$y(t) = 0.5 u(t) - 0.5 e^{-2t}u(t) + 0.25 e^{-4t}u(t) \quad (5M)$$

Find the response $y(t)$ of a continuous time system using Laplace transform with transfer function

$$H(s) = \frac{1}{(s+2)(s+3)}$$

3

for an input $x(t) = e^{-t} u(t)$. (15M)[Nov 2016] -BTL3

Solution

Response of the system

$$y(t) = x(t) h(t)$$

$$Y(s) = X(s) H(s)$$

$$x(t) = e^{-t} u(t)$$

Taking Laplace transform of the above equation

$$X(s) = \frac{1}{(s+1)}$$

$$Y(s) = \frac{1}{(s+1)} \frac{1}{(s+2)(s+3)}$$

$$Y(s) = \frac{1}{(s+1)(s+2)(s+3)}$$

(3M)

By partial fraction expansion technique

$$Y(s) = \frac{1}{(s+1)(s+2)(s+3)} = \frac{A}{(s+1)} + \frac{B}{(s+2)} + \frac{1}{(s+3)}$$

$$\text{If } s = -1 \quad A = \frac{1}{2}$$

$$\text{If } s = -2 \quad B = -1$$

$$\text{If } s = -3 \quad C = \frac{1}{2}$$

(5M)

$$Y(s) = \frac{\frac{1}{2}}{(s+1)} - \frac{1}{(s+2)} + \frac{\frac{1}{2}}{(s+3)}$$

Taking inverse Laplace transforms,

$$y(t) = \frac{1}{2} e^{-t} u(t) - e^{-2t} u(t) + \frac{1}{2} e^{-3t} u(t)$$

(7M)

UNIT IV- ANALYSIS OF DISCRETE TIME SIGNALS

Baseband signal Sampling – Fourier Transform of discrete time signals (DTFT) – Properties of DTFT - Z Transform & Properties

PART A

Q.N

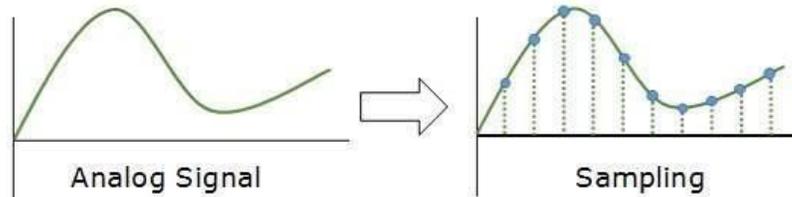
Questions

0

Define sampling theorem. (May 2019)-BTL1

- Sampling is a process in which a continuous signal is converted into a sequence of discrete samples, with each sample representing the amplitude of the signal at a particular instant of time.

$$F_s > 2 F_m$$



1

- In this process, it is necessary to choose the sampling rate properly. So, the sampling theorem stated that,
- A bandwidth signal which has no spectral components above the frequency f_m Hz is uniquely determined by its values at uniform intervals less than $\frac{1}{2} f_m$ seconds apart.

Write the relationship between DTFT and Z transform. (May 2019)-BTL2

Solution

$$H(z) = \sum_{n=-\infty}^{\infty} h(n) z^{-n}$$

$$H(re^{j\omega}) = \sum_{n=-\infty}^{\infty} h(n) r e^{j\omega n}$$

$$z = r e^{j\omega} \quad r = 1$$

$$H(e^{j\omega}) = \sum_{n=-\infty}^{\infty} h(n) e^{-j\omega n}$$

$$H(e^{j\omega}) = H(z)$$

ROC must include the unit circle.

2

3

The DTFT of a discrete time signal $x(n)$ is given as $X(e^{j\omega}) = 2e^{j2\omega} + 3 + 4e^{-j\omega} - 2e^{-j2\omega}$. Find the time domain signal $x(n)$. (Nov 2018)-BTL3

Solution

	$x(n) = \{2, 3, 4, -1\}$
4	<p>List the ROC properties of Laplace Transform (Nov 2017)-BTL1</p> <p>ROC doesn't have any pole because it cannot include a pole. ROC is a strip parallel to the $j\omega$ axis. If the ROC includes the axis $\sigma = 0$, Fourier transform exists. For right-handed signals, ROC is given by $\text{Re}(s) > \sigma$.</p>
5	<p>Find the z-transform of a sequence $x(n) = \cos(n\omega T) u(n)$ (Nov 2017)-BTL3</p> <p>Solution</p> <p>Given that, $x(n) = \cos(n\omega T) u(n)$</p> <p>By the definition of z-transform</p> $X(z) = \sum_{n=-\infty}^{\infty} x(n)z^{-n}$ $X(z) = \sum_{n=0}^{\infty} \cos(n\omega T) z^{-n}$ <div style="border: 1px solid black; padding: 5px; width: fit-content; margin: 10px auto;"> $\text{Euler form, } \cos \theta = \frac{e^{j\theta} + e^{-j\theta}}{2}$ </div> $X(z) = \sum_{n=0}^{\infty} \frac{e^{j\omega n T} + e^{-j\omega n T}}{2} z^{-n}$ $X(z) = \frac{1}{2} \sum_{n=0}^{\infty} e^{j\omega n T} z^{-n} + \frac{1}{2} \sum_{n=0}^{\infty} e^{-j\omega n T} z^{-n}$ $X(z) = \frac{1}{2} \sum_{n=0}^{\infty} (e^{j\omega T} z^{-1})^n + \frac{1}{2} \sum_{n=0}^{\infty} (e^{-j\omega T} z^{-1})^n$ <p>Using infinite geometric series sum formula</p> $\sum_{n=0}^{\infty} C^n = \frac{1}{1-C}$ $X(z) = \frac{1}{2} \frac{1}{1 - e^{j\omega T} z^{-1}} + \frac{1}{2} \frac{1}{1 - e^{-j\omega T} z^{-1}}$ $X(z) = \frac{1}{2} \frac{1 - e^{-j\omega T} z^{-1} + 1 - e^{j\omega T} z^{-1}}{(1 - e^{j\omega T} z^{-1})(1 - e^{-j\omega T} z^{-1})}$ $X(z) = \frac{1}{2} \frac{2 - z^{-1}(e^{j\omega T} + e^{-j\omega T})}{(1 - e^{-j\omega T} z^{-1}) - e^{j\omega T} z^{-1} + z^{-2}}$ $X(z) = \frac{1}{2} \frac{2 - z^{-1} 2 \cos \omega T}{(1 - e^{-j\omega T} z^{-1}) - e^{j\omega T} z^{-1} + z^{-2}}$

	$X(z) = \frac{1 - z^{-1} \cos \omega T}{(1 - e^{-j\omega T} z^{-1}) - e^{j\omega T} z^{-1} + z^{-2}}$
6	<p>What is the z transform of a unit step sequence? [May 2017]R13-BTL1</p> <p>Solution Given that, unit step sequence $x(n) = u(n)$</p> $X(z) = \sum_{n=-\infty}^{\infty} x(n)z^{-n}$ $X(z) = \sum_{n=0}^{\infty} z^{-n}$ $X(z) = \frac{z}{z-1}$
7	<p>Find $x(\infty)$ of the signal for with the z-transform is given by [May 2017]-BTL3</p> $X(z) = \frac{z+1}{3(z-1)(z+0.9)}$ <p>$x(\infty)=0$</p>
8	<p>Find the nyquist rate of the signal $x(t) = \sin 200 \pi t - \cos 100 \pi t$ (May 2018, Nov 2016)-BTL3</p> <p>Solution Given that, $x(t) = \sin 200 \pi t - \cos 100 \pi t$ $2\pi F_1 = 200 \pi \quad F_1 = 100$ $2\pi F_2 = 100 \quad F_2 = 50$ Nyquist sampling rate $F_s = 2 F_{\max}$ $F_s = 2 * 100 \quad F_s = 200 \text{ Hz.}$</p>
9	<p>Find the z transform of the signal and associated ROC.BTL3 $x(n) = [2, -1, 3, 0, 2]$ (Nov 2016)-BTL3</p> <p>Solution</p> <p>From the given sequence, $x(-2) = 2, x(-1) = -1, x(0) = 3, x(1) = 0, x(2) = 2$ Definition of z – Transform,</p>

	$X(z) = \sum_{n=-\infty}^{\infty} x(n)z^{-n}$ $X(z) = \sum_{n=-2}^2 x(n)z^{-n}$ $X(z) = 2z^2 - z + 3 + 2z^{-2}$ <p>The ROC is entire z - plane except z = 0 and z = ∞</p>
10	<p>Write the condition for existence of DTFT. [May 2016] -BTL1</p> <p>DTFT The Fourier transform of discrete signal is called Discrete time Fourier Transform</p> $X(e^{j\omega}) = \sum_{n=-\infty}^{\infty} x(n)e^{-j\omega n}$ <p>Inverse DTFT</p> $x(n) = \frac{1}{2\pi} \int_{-\pi}^{\pi} X(e^{j\omega})e^{j\omega n} \text{ for } n = -\infty \text{ to } \infty$
11	<p>Find the final value of the given signal, [May 2016]-BTL3</p> $X(z) = \frac{1}{1+2z^{-1}+3z^{-2}}$ <p>Solution</p> <p>Given that, $X(z) = \frac{1}{1+2z^{-1}+3z^{-2}}$</p> $x(\infty) = \lim_{z \rightarrow 1} (1 - z^{-1})X(z)$ $x(\infty) = \lim_{z \rightarrow 1} (1 - z^{-1}) \frac{1}{1+2z^{-1}+3z^{-2}}$ $x(\infty) = \lim_{z \rightarrow 1} (1 - z^{-1}) \frac{z^2}{z^2+2z+3}$ $x(\infty) = \lim_{z \rightarrow 1} \frac{z^2 - z}{z^2+2z+3}$ $x(\infty) = 0$
12	<p>State the need for sampling. [Nov 2015] -BTL1</p> <p>The sampling is needed for processing of continuous time signal using its sampled version of digital systems.</p> <p>When sampling frequency F_s is equal to $2F_{\max}$, the sampling rate is called nyquist rate.</p>

13	<p>Find the z – Transform and its associated ROC for, $x(n) = \{1, -1, 2, 3, 4\}$ [Nov 2015] -BTL3</p> <p>Solution</p> <p>Given that, $x(n) = \{1, -1, 2, 3, 4\}$</p> <p>From the given sequence, $x(-3) = 1, x(-2) = -1, x(-1) = 2, x(0) = 3, x(1) = 4$</p> <p>Definition of z – Transform,</p> $X(z) = \sum_{n=-\infty}^{\infty} x(n)z^{-n}$ $X(z) = \sum_{n=-3}^1 x(n)z^{-n}$ $X(z) = z^3 - z^2 + 3z + 3 + 4z^{-1}$ <p>The ROC is entire z – plane except $z = 0$ and $z = \infty$</p>
14	<p>Determine the nyquist sampling rate for, $x(t) = \sin(200\pi t) + 3\sin^2(120\pi t)$ [May 2015] -BTL3</p> <p>Solution</p> <p>Given that, $x(t) = \sin(200\pi t) + 3\sin^2(120\pi t)$</p> $x_1(t) = \sin(200\pi t)$ $2\pi F_1 = 200\pi \quad F_1 = 100$ $x_2(t) = 3\sin^2(120\pi t)$ $2\pi F_2 = 120\pi \quad F_2 = 60$ <p>Nyquist sampling rate $F_s = 2 F_{\max}$</p> $F_s = 2 * 100$ $F_s = 200 \text{ Hz.}$
15	<p>List out the methods for finding the inverse z – Transform. [May 2015] -BTL1</p> <p>They are three methods for finding inverse z – transform</p> <p>Long division method</p> <p>Partial fraction method</p> <p>Residue method</p>
16	<p>Find the DTFT of $x(n) = \delta(n) + \delta(n-1)$ [Nov 2014] -BTL3</p> <p>Solution</p>

	<p>By definition of Fourier transform,</p> $X(e^{j\omega}) = \sum_{n=-\infty}^{\infty} x(n)e^{-j\omega n}$ $X(e^{j\omega}) = \sum_{n=-\infty}^{\infty} \{\delta(n) + \delta(n-1)\}e^{-j\omega n}$ $= \sum_{n=-\infty}^{\infty} \delta(n)e^{-j\omega n} + \sum_{n=-\infty}^{\infty} \delta(n-1)e^{-j\omega n}$ $= 1 * e^0 + 1 * e^{-j\omega}$ $X(e^{j\omega}) = \frac{e^{j\omega} + 1}{e^{j\omega}}$
17	<p>State and prove the time folding property of z- Transform. [Nov 2014]= BTL1</p> <p>Time reversal property If z transform of $x(n) = X(z)$ $x(-n) = X(z^{-1})$ Proof By definition of z – transform</p> $X(z) = \sum_{n=-\infty}^{\infty} x(n)z^{-n}$ $= \sum_{n=-\infty}^{\infty} x(-n)z^{-n} = \sum_{p=-\infty}^{\infty} x(p)z^p$ $= \sum_{p=-\infty}^{\infty} x(p)(z^{-1})^{-p}$ $X(z) = X(z^{-1})$
18	<p>State sampling theorem. [May 2015,2010] -BTL1</p> <p>A band limited continuous time signal with maximum frequency F_m can be fully recovered from its samples provided that the sampling frequency F_s is greater than or equal to twice the maximum frequency F_m.</p> <p>$F_s > 2 F_m$</p>
19	<p>What is meant by ROC of z – Transform? [May 2015]-BTL1</p>

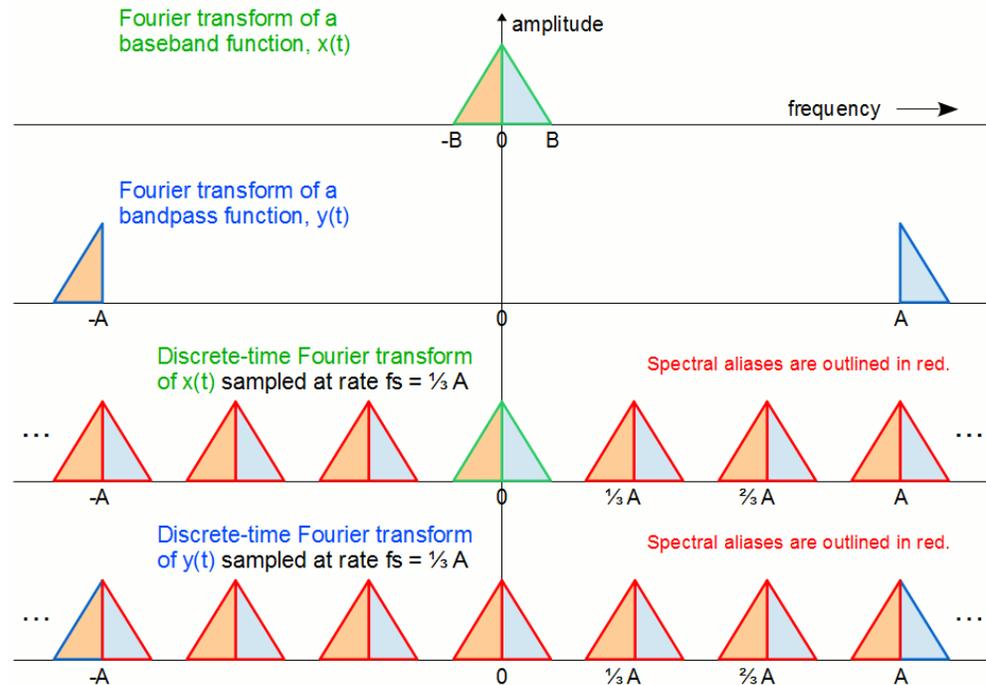
	<p>Write a note on ROC. <i>[Nov 2014]</i></p> <p>The z – Transform is an infinite power series, it exists only for those values of z for which the series converges. The region of convergence of X (z) is the set of all values of z, for which X (z) attains a finite value.</p> <p>Every X (z) there will be a set of values of z for which X (z) can be computed. Such a set of values will lie in a particular region of z – plane and this region is called Region of Convergence (ROC) of X (z).</p>
20	<p>What is aliasing? <i>[May 2013,2016,Nov 2013,2014]</i> -BTL1</p> <p>The phenomenon of high frequency component getting the identity of low frequency component during sampling is called aliasing.</p> <p>Due to overlap of frequency spectrum, the high frequency components get the identity of low frequency components. This phenomenon is called aliasing.</p>
21	<p>What is an anti – aliasing filter? <i>[May 2014]</i> -BTL1</p> <p>A continuous time signal with large bandwidth can be band limited by passing through a filter before sampling. When the frequency range of the output signal of the filter is chosen to prevent aliasing due to sampling, the filter is called anti-aliasing filter.</p> <p>in order to avoid aliasing the sampling frequency F_s should be greater than twice the maximum frequency F_m of continuous time signal.</p>
22	<p>State the multiplication property of DTFT. <i>[May 2014]</i> -BTL1</p> <p>Multiplication property of DTFT</p> <p>Z transform of $x_1(n) = X_1(e^{j\omega})$</p> <p>Z transform of $x_2(n) = X_2(e^{j\omega})$</p> <p>The complex convolution theorem state that</p> $x_1(n) x_2(n) = \frac{1}{2\pi j} \oint X_1(v) X_2\left(\frac{z}{v}\right) v^{-1} dv$ <p>v is the dummy variable used for contour integration.</p>
23	<p>Define unilateral and bilateral z – Transform. <i>[Nov 2013,May 2016]</i> -BTL1</p>

	<p>Bilateral z Transform</p> $X(z) = \sum_{n=-\infty}^{\infty} x(n)z^{-n}$ <p>Z is a complex variable</p> <p>Unilateral z Transform</p> $X(z) = \sum_{n=0}^{\infty} x(n)z^{-n}$
24	<p>Find the z – Transform and its associated ROC for $x(n) = \{1, -1, 2, 3, 4\}$ [Nov 2015, 2016] -BTL3</p> <p>From the given sequence, $x(-3) = 1, x(-2) = -1, x(-1) = 2, x(0) = 3, x(1) = 4$</p> <p>Definition of z – Transform,</p> $X(z) = \sum_{n=-\infty}^{\infty} x(n)z^{-n}$ $X(z) = \sum_{n=-3}^1 x(n)z^{-n}$ $X(z) = z^3 - z^2 + 2z + 3 + 4z^{-1}$ <p>The ROC is entire z – plane except $z = 0$ and $z = \infty$</p>
25	<p>Define circularly folded sequences. BTL1</p> <p>A circularly folded sequence is represented as $x((-n))_N$. It is obtained by plotting $x(n)$ in clockwise direction along the circle.</p>
	PART-B
Q.No	Questions
1	<p>State and explain sampling theorem both in time domain and frequency domain with necessary quantitative analysis and illustrations. (10 marks & 16 marks) (or) State and prove sampling theorem for a band limited signal. (16 marks) <i>[May 2017]R13, [May 2016] R13, [Nov 2015] R13 [Nov 2014]R13</i> <i>[Nov 2012, Nov 2015, 2014, 2012, 2011]R08-BTL2</i></p> <p>Base band sampling</p> <p>The term base band signal is used to indicate the unmodulated signal which has the original frequency components. Therefore a signal in its original form is called base band sampling. The sampling of unmodulated or original signal is called base band sampling.</p> <p>Sampling</p>

The sampling is the process of conversion of a continuous time signal into a discrete time signal. The sampling is performed by taking samples of continuous time signal at definite intervals of time.

Periodic or uniform sampling

The time interval between two successive samples will be same and such type of sampling is called periodic or uniform sampling.



(5)

Sampling time

The time interval between two successive samples is called sampling time (or sampling period or sampling interval), denoted as T .

Sampling frequency

The inverse of sampling period is called sampling frequency (or sampling rate), and it is denoted by F_s .

Let $x(t)$ is the continuous time signal $x(n)$ is the discrete time signal

The relation between $x(n)$ and $x_a(t)$ can be expressed as,

$$x(n) = x_a(t) \quad \text{at } t = nT$$

$$x(nT) = x_a(n/F_s)$$

T is the sampling period

F_s is the sampling or sampling frequency

The relation between frequency of analog and discrete time signal is,

$$f = \frac{F}{F_s}$$

The range of frequency of discrete time signal is,

$$-1/2 \leq f \leq 1/2$$

$$-\frac{F_s}{2} \leq \frac{F}{F_s} \leq \frac{F_s}{2}$$

(3)

Alias

Infinite number of higher frequency continuous time signals will be represented by a single discrete time signal. Such signals are called alias

Aliasing

The phenomenon of high frequency component getting the identity of low frequency component during sampling is called aliasing

Folding frequency

Sampling an analog signal with frequency F by choosing a sampling frequency F_s such that $F_s/2 > F$ will not result in alias. But sampling frequency is selected such that $F_s/2 < F$ that the frequency above $F_s/2$ will have alias with frequency below $F_s/2$. Hence the point of reflection is $F_s/2$, and the frequency $F_s/2$ is called folding frequency.

For unique representation of analog signal with maximum frequency F_{max} , the sampling frequency should be greater than $2F_{max}$.

To avoid aliasing $F_s \geq 2F_{max}$.

(4)

When the sampling frequency F_s is equal to $2F_{max}$, the sampling rate is called Nyquist rate.

Sampling theorem

A band limited continuous time signal with maximum frequency F_m can be fully recovered from its samples provided that the sampling frequency F_s is greater than or equal to twice the maximum frequency F_m .

$F_s > 2F_m$

Frequency spectrum of Discrete Time Signal

For Fourier transform $X(e^{j\omega})$ of a signal $x(n)$ represents the frequency content of $x(n)$. the signal decomposed into its frequency components. Hence $X(e^{j\omega})$ is called frequency spectrum of discrete time signal or signal spectrum.

$X(e^{j\omega})$ is a complex function of ω the frequency spectrum can be divided into two components, Magnitude spectrum

Phase spectrum

Aliasing in frequency spectrum due to sampling

Let $x(t)$ be an analog signal and $X(j\Omega)$ be Fourier transform of $x(t)$. The definition of continuous time inverse Fourier transform,

$$x(t) = \frac{1}{2\pi} \int_{-\infty}^{\infty} X(j\Omega) e^{j\Omega t} d\Omega$$

Let $x(nT)$ be a discrete time signal obtained by sampling $x(t)$ with sampling period T , therefore

$$x(nT) = \frac{1}{2\pi} \int_{-\infty}^{\infty} X(j\Omega) e^{j\Omega t} d\Omega \quad \text{at } t = nT$$

The frequency spectrum of a discrete time signal obtained by sampling continuous time signal will be sum of frequency shifted and amplitude scaled spectrum continuous time signal.

In order to avoid aliasing the sampling frequency F_s should be greater than twice the maximum frequency F_m of continuous time signal.

$$F_s > 2 F_m$$

Anti-aliasing filter

(4)

A continuous time signal with large bandwidth can be band limited by passing through a filter before sampling. When the frequency range of the output signal of the filter is chosen to prevent aliasing due to sampling, the filter is called anti-aliasing filter.

Signal Reconstruction

If the sampling frequency $F_s > 2 F_m$, then the spectrum $X(e^{j\omega})$ of the sampled continuous time signal will have aliased components of the spectrum $X(j\Omega)$ of original continuous time signal.

The aliasing of spectral components prevents the recovery of original signal $x(t)$ from the sampled signal $x(nT)$.

2.

State and prove the following properties of DTFT

i. Differentiation in frequency

ii. Convolution in frequency domain

(13M)[May 2017] -BTL1

Differentiation in frequency

If DTFT of $x(n) = X(e^{j\omega})$

Then $n x(n) = j \frac{d}{d\omega} X(e^{j\omega})$

Proof

By the definition of Fourier transform,

$$X(e^{j\omega}) = \sum_{n=-\infty}^{\infty} x(n) e^{-j\omega n}$$

$$= \sum_{n=-\infty}^{\infty} n x(n) j X(-j) e^{-j\omega n}$$

$$= j \sum_{n=-\infty}^{\infty} x(n) [-j n e^{-j\omega n}]$$

note : $-jn = \frac{d}{d\omega}$

$$= j \sum_{n=-\infty}^{\infty} x(n) \left[\frac{d}{d\omega} e^{-j\omega n} \right]$$

$$= j \frac{d}{d\omega} \sum_{n=-\infty}^{\infty} x(n) [e^{-j\omega n}]$$

$$n x(n) = j \frac{d}{d\omega} X(e^{j\omega})$$

Convolution in frequency domain

By using the Fourier transform in discrete signal

If DTFT of $x(n) = X(e^{j\omega})$

If DTFT of $x_1(n) = X_1(e^{j\omega})$

DTFT of $x_2(n) = X_2(e^{j\omega})$

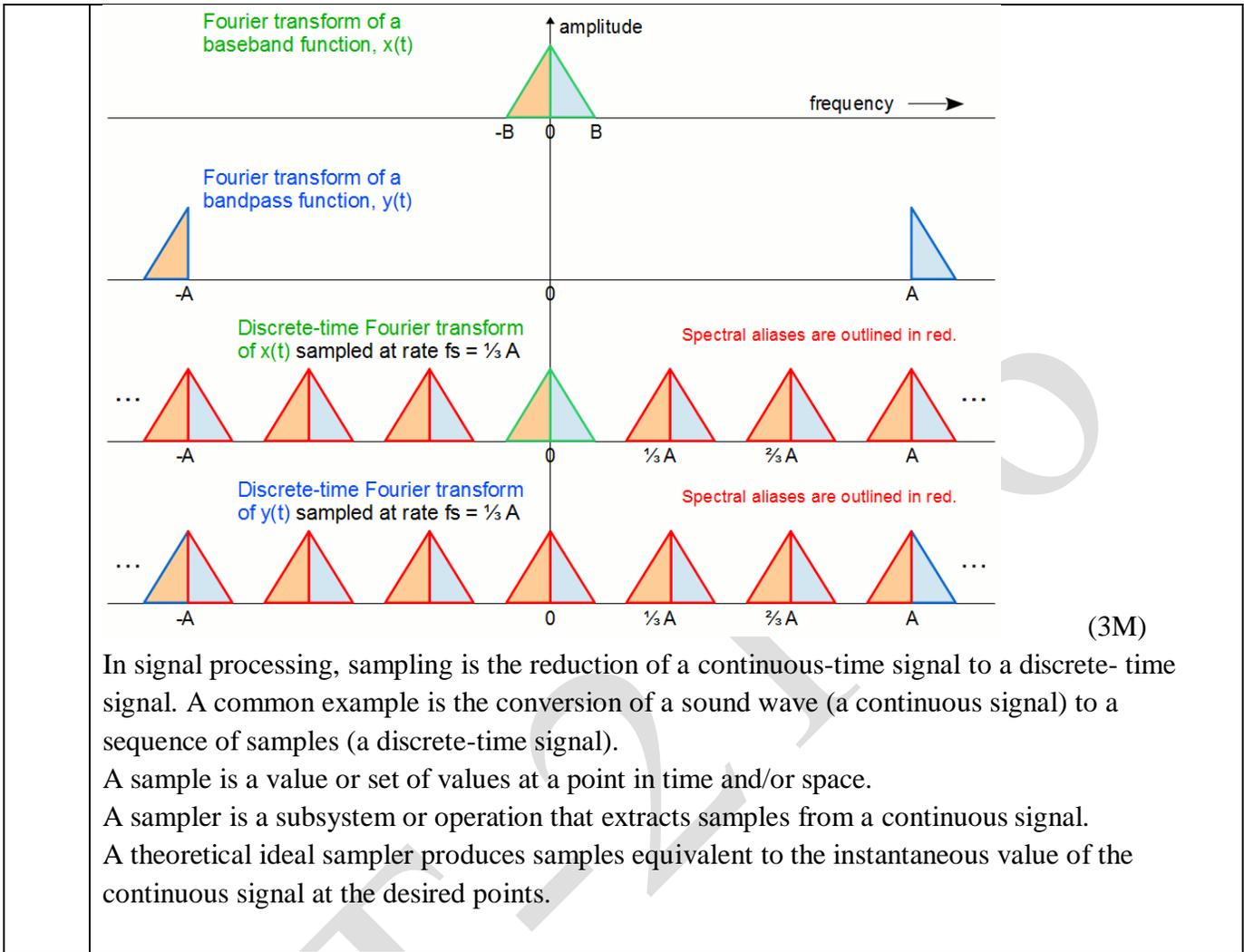
$$x_1(n) * x_2(n) = X_1(e^{j\omega}) X_2(e^{j\omega})$$

$$x_1(n) * x_2(n) = \sum_{m=-\infty}^{\infty} x_1(m) x_2(n-m)$$

(7M)

The Fourier transform of the convolution of $x_1(n)$ and $x_2(n)$ is equal to the product of

	<p>$X_1(e^{j\omega})$ and $X_2(e^{j\omega})$. it means that if we convolve two signals in time domain, it is equivalent to multiplying their spectra in frequency domain.</p> <p>Proof</p> <p>By the definition of Fourier transform,</p> $X(e^{j\omega}) = \sum_{n=-\infty}^{\infty} x(n)e^{-j\omega n}$ $X_1(e^{j\omega}) = \sum_{n=-\infty}^{\infty} x_1(n)e^{-j\omega n}$ $X_2(e^{j\omega}) = \sum_{n=-\infty}^{\infty} x_2(n)e^{-j\omega n}$ $x_1(n) * x_1(n) = \sum_{n=-\infty}^{\infty} [x_1(n) * x_1(n)]e^{-j\omega n}$ $x_1(n) * x_1(n) = \sum_{n=-\infty}^{\infty} \sum_{m=-\infty}^{\infty} [x_1(m) * x_1(n-m)]e^{-j\omega n} e^{-j\omega m} e^{j\omega m}$ $x_1(n) * x_1(n) = \sum_{n=-\infty}^{\infty} x_1(m)e^{-j\omega m} \sum_{n=-\infty}^{\infty} [x_1(n-m)]e^{-j\omega(n-m)}$ $x_1(n) * x_1(n) = \sum_{m=-\infty}^{\infty} x_1(m)e^{-j\omega m} \sum_{p=-\infty}^{\infty} [x_1(p)]e^{-j\omega p}$ $x_1(n) * x_1(n) = X_1(e^{j\omega}) X_1(e^{j\omega})$ <p style="text-align: right;">(6M)</p>
3	<p>Discuss the effect of under sampling a signal using necessary diagrams. (5 marks) [Nov 2016] -BTL2</p> <p>In signal processing, under sampling or band pass sampling is a technique where one samples a band pass-filtered signal at a sample rate below its Nyquist rate (twice the upper cutoff frequency), but is still able to reconstruct the signal. (2M)</p> <p>When one under samples a band pass signal, the samples are indistinguishable from the samples of a low-frequency alias of the high-frequency signal. Such sampling is also known as band pass sampling, harmonic sampling, IF sampling, and direct IF-to-digital conversion.</p>



In signal processing, sampling is the reduction of a continuous-time signal to a discrete-time signal. A common example is the conversion of a sound wave (a continuous signal) to a sequence of samples (a discrete-time signal).

A sample is a value or set of values at a point in time and/or space.

A sampler is a subsystem or operation that extracts samples from a continuous signal.

A theoretical ideal sampler produces samples equivalent to the instantaneous value of the continuous signal at the desired points.

Find the z-transform of $x(n) = a^n u(n) - b^n u(-n-1)$ and specify its ROC. (8 marks)
 [Nov 2016]- BTL3

By the definition of z – transform,

$$X(z) = \sum_{n=-\infty}^{\infty} x(n)z^{-n}$$

$$x(n) = a^n u(n) - b^n u(-n-1) \tag{3M}$$

4.

$$X(z) = \sum_{n=-\infty}^{\infty} \{a^n u(n) - b^n u(-n-1)\}z^{-n}$$

Taking z transform of the signal,

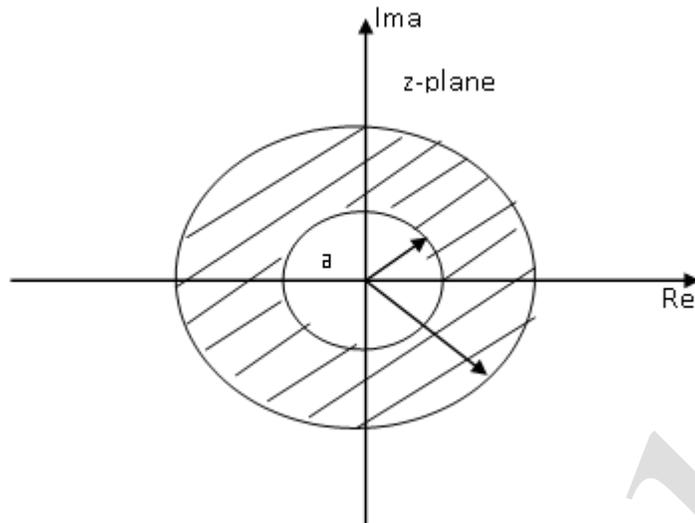
$$X(z) = \frac{z}{z-a} - \frac{z}{z-b} \tag{2M}$$

Hence the condition for convergence of $a^n u(n)$ is $0 < az^{-1} < 1$ i.e., $z > a$

Hence the condition for convergence of $b^n u(-n-1)$ is $0 < az^{-1} < 1$ i.e., $z < b$

(3M)

ROC



The term $z = b$ represents a circle of radius b in z -plane and term $z = a$ represents a circle of radius a in z -plane.

Give the relation between DTFT and z - Transform. (5 marks)[Nov 2016]-BTL2

Solution

The z – transform of a discrete time signal $x(n)$ is defined as,

By the definition of z – transform,

$$X(z) = \sum_{n=-\infty}^{\infty} x(n)z^{-n}$$

The Fourier transform of a discrete time signal $x(n)$ is defined as,

By the definition of DTFT,

$$X(e^{j\omega}) = \sum_{n=-\infty}^{\infty} x(n)e^{-j\omega n}$$

(3M)

The $X(z)$ can be viewed as a unique representation of the signal $x(n)$ in the complex z – plane. in z -plane, the point $z = e^{j\omega}$, represents a point with unit magnitude and having a phase of ω . the range of frequency of discrete time signal ω is 0 to 2π .

5

	<p>Hence, the points on unit circle in z-plane are given by, $z = e^{j\omega}$. When ω is varies from 0 to 2π. (2M)</p> <p>It is important to note that $X(z)$ exists for $z = e^{j\omega}$ if unit circle is included in ROC of $X(z)$. Therefore the Fourier transform can be obtained from z-transform by evaluating $X(z)$ at $z = e^{j\omega}$, if and only if ROC of $X(z)$ includes the unit circle.</p>
6	<p>State and prove the time shifting property and time reversal property of Z-transform. (8 marks)[Nov 2016] -BTL1</p> <p>Time shifting property (4M)</p> <p>Let DTFT of $x(n) = X(e^{j\omega})$</p> $x(n - m) = e^{-j\omega m} X(e^{j\omega})$ $x(n + m) = e^{j\omega m} X(e^{j\omega})$ <p>This relation means that if a signal shifted in time domain by m samples, its magnitude spectrum remains unchanged.</p> <p>Proof</p> <p>By definition of Fourier transform,</p> $X(e^{j\omega}) = \sum_{n=-\infty}^{\infty} x(n) e^{-j\omega n}$ $x(n - m) = \sum_{n=-\infty}^{\infty} x(n - m) e^{-j\omega n}$ $= \sum_{p=-\infty}^{\infty} x(p) e^{-j\omega(m+p)}$ $= \sum_{p=-\infty}^{\infty} x(p) e^{-j\omega m} e^{-j\omega p}$ $= e^{-j\omega m} \sum_{p=-\infty}^{\infty} x(p) e^{-j\omega p}$ $= e^{-j\omega m} \sum_{n=-\infty}^{\infty} x(n) e^{-j\omega n}$ $\mathbf{x(n - m) = e^{-j\omega m} X(e^{j\omega})}$ <p>Time reversal property (4M)</p> <p>If z transform of $x(n) = X(z)$</p> $x(-n) = X(z^{-1})$ <p>Proof</p> <p>By definition of z - transform</p>

$$\begin{aligned}
 X(z) &= \sum_{n=-\infty}^{\infty} x(n)z^{-n} \\
 &= \sum_{n=-\infty}^{\infty} x(-n)z^{-n} = \sum_{p=-\infty}^{\infty} x(p)z^p \\
 &= \sum_{p=-\infty}^{\infty} x(p)(z^{-1})^{-p} \\
 \mathbf{X(z)} &= \mathbf{X(z^{-1})}
 \end{aligned}$$

What is aliasing? Explain the steps to be taken to avoid aliasing.
(6 marks)[May 2016]R13, Nov 2012-BTL2

Aliasing (3M)

- The phenomenon of high frequency component getting the identity of low frequency component during sampling is called aliasing.
- Due to overlap of frequency spectrum, the high frequency components get the identity of low frequency components. This phenomenon is called aliasing.

Folding frequency

Sampling an analog signal with frequency F by choosing a sampling frequency F_s such that $F_s/2 > F$ will not result in alias. But sampling frequency is selected such that $F_s/2 < F$ that the frequency above $F_s/2$ will have alias with frequency below $F_s/2$. Hence the point of reflection is $F_s/2$, and the frequency $F_s/2$ is called folding frequency.

7.

For unique representation of analog signal with maximum frequency F_{max} , the sampling frequency should be greater than $2F_{max}$.

To avoid aliasing $F_s \geq 2F_{max}$.

When the sampling frequency F_s is equal to $2F_{max}$, the sampling rate is called Nyquist rate.

Sampling theorem (3M)

A band limited continuous time signal with maximum frequency F_m can be fully recovered from its samples provided that the sampling frequency F_s is greater than or equal to twice the maximum frequency F_m .

$$F_s > 2 F_m$$

Anti-aliasing filter

A continuous time signal with large bandwidth can be band limited by passing through a filter before sampling. When the frequency range of the output signal of the

	<p>filter is chosen to prevent aliasing due to sampling, the filter is called anti-aliasing filter.</p>
8	<p>State and prove the following theorems:</p> <p>(i) Convolution theorem of DTFT(8 marks)</p> <p>(ii) Initial value theorem of z – Transform. (8 marks)</p> <p><i>[May 2013] -BTL1</i></p> <p>Convolution theorem of DTFT (8M)</p> <p>If DTFT of $x_1(n) = X_1(e^{j\omega})$ DTFT of $x_2(n) = X_2(e^{j\omega})$</p> $x_1(n) * x_2(n) = X_1(e^{j\omega}) X_2(e^{j\omega})$ $x_1(n) * x_1(n) = \sum_{m=-\infty}^{\infty} x_1(m) x_1(n-m)$ <p>The Fourier transform of the convolution of $x_1(n)$ and $x_2(n)$ is equal to the product of $X_1(e^{j\omega})$ and $X_2(e^{j\omega})$. It means that if we convolve two signals in time domain, it is equivalent to multiplying their spectra in frequency domain.</p> <p>Proof</p> <p>By the definition of Fourier transform,</p> $X_1(e^{j\omega}) = \sum_{n=-\infty}^{\infty} x_1(n) e^{-j\omega n}$ $X_2(e^{j\omega}) = \sum_{n=-\infty}^{\infty} x_2(n) e^{-j\omega n}$ $x_1(n) * x_2(n) = \sum_{n=-\infty}^{\infty} [x_1(n) * x_2(n)] e^{-j\omega n}$ $x_1(n) * x_2(n) = \sum_{n=-\infty}^{\infty} \sum_{m=-\infty}^{\infty} [x_1(m) * x_2(n-m)] e^{-j\omega n} e^{-j\omega m} e^{j\omega m}$ $x_1(n) * x_2(n) = \sum_{n=-\infty}^{\infty} x_1(m) e^{-j\omega m} \sum_{n=-\infty}^{\infty} [x_2(n-m)] e^{-j\omega(n-m)}$ $x_1(n) * x_2(n) = \sum_{m=-\infty}^{\infty} x_1(m) e^{-j\omega m} \sum_{p=-\infty}^{\infty} [x_2(p)] e^{-j\omega p}$ $x_1(n) * x_2(n) = X_1(e^{j\omega}) X_2(e^{j\omega})$

	<p>Initial value theorem of z – Transform (8M)</p> <p>Let $x(n)$ be a one sided signal defined in the range $0 \leq n \leq \infty$.</p> <p>If z – transform $x(n) = X(z)$</p> <p>Then the initial value of an $x(n)$ [i.e., $x(0)$],</p> $x(0) = \lim_{z \rightarrow \infty} X(z)$ <p>Proof</p> <p>By the definition of z - transform,</p> $X(z) = \sum_{n=0}^{\infty} x(n)z^{-n}$ <p>On expanding the above equation</p> $X(z) = x(0) + \frac{x(1)}{z} + \frac{x(2)}{z^2} + \dots$ <p>Taking the limit $z = \infty$</p> $X(0) = x(0) + 0 + 0 \dots$ <p>Therefore,</p> $x(0) = \lim_{z \rightarrow \infty} X(z). \text{ Hence it is proved.}$
9	<p>Find the DTFT of $x(n)$ (5 marks) [May 2015]R13-BTL5</p> $x(n) = \left(\frac{1}{2}\right)^{n-1} u(n-1) = \left(\frac{1}{2}\right)^n ; n \geq 1$ <p>Solution</p> <p>Given that, $x(n) = \left(\frac{1}{2}\right)^{n-1} u(n-1) = \left(\frac{1}{2}\right)^n ; n \geq 1$</p> <p>By definition of Fourier transform,</p> $X(e^{j\omega}) = \sum_{n=-\infty}^{\infty} x(n)e^{-j\omega n}$ $X(e^{j\omega}) = \sum_{n=1}^{\infty} \left(\frac{1}{2}\right)^n e^{-j\omega n}$ <p>(3M)</p>

	<p>Using infinite geometric series sum formula $\sum_{n=0}^{\infty} C^n = \frac{1}{1-C}$</p> $X(e^{j\omega}) = \frac{1}{1 - \frac{1}{2}e^{-j\omega}} - 1$ $X(e^{j\omega}) = \frac{-1 + 1 + \frac{1}{2}e^{-j\omega}}{1 - \frac{1}{2}e^{-j\omega}}$ $X(e^{j\omega}) = \frac{\frac{1}{2}e^{-j\omega}}{1 - \frac{1}{2}e^{-j\omega}}$ $X(e^{j\omega}) = \frac{e^{-j\omega}}{2 - e^{-j\omega}}$ <p style="text-align: right;">(2M)</p>
10	<p>Using suitable z – Transform properties find X(z) (6 marks)[May 2015] –BTL3</p> $x(n) = (n-2) \left(\frac{1}{3}\right)^{n-2} u(n-2)$ <p>Solution Given that,</p> <p>Let $x(n) = \left(\frac{1}{3}\right)^n u(n)$; $n \geq 0$</p> <p>By definition of z - transform,</p> $X(z) = \sum_{n=-\infty}^{\infty} x(n)z^{-n}$ $X(z) = \sum_{n=0}^{\infty} \left(\frac{1}{3}\right)^n z^{-n}$ $X(z) = \sum_{n=0}^{\infty} \left(\frac{1}{3} z^{-1}\right)^n$ <p>(3)</p> <p>Using infinite geometric series sum formula $\sum_{n=0}^{\infty} C^n = \frac{1}{1-C}$</p> $X(z) = \frac{1}{1 - \frac{1}{3}z^{-1}}$ $X(z) = \frac{z}{z - \frac{1}{3}}$ <p style="text-align: right;">(3M)</p>

By differentiation in z - domain property of z - transform

$$n x(n) = -z \frac{d}{dz} X(z)$$

$$n x(n) = -z \frac{d}{dz} \left\{ \frac{z}{z - \frac{1}{3}} \right\}$$

$$n x(n) = -z \left\{ \frac{\left\{ \frac{z - \frac{1}{3}}{z} \right\} - z}{\left(z - \frac{1}{3} \right)^2} \right\}$$

$$n x(n) = \left\{ \frac{\frac{1}{3} z}{\left(z - \frac{1}{3} \right)^2} \right\}$$

By shifting in z - domain property of z - transform

$$(n-2) \left(\frac{1}{3} \right)^{n-2} u(n-2) = \left\{ \frac{\frac{1}{3}}{z \left(z - \frac{1}{3} \right)^2} \right\}$$

PART-C**Q.N
o****Questions****Determine the z-transform of the following signal and plot the ROC.**

i. $x(n) = a^n u(n)$

ii. $x(n) = -a^n u(-n-1)$ (15 marks) *[May 2015]-BTL3*

Solution

Given that, $x(n) = a^n u(n)$ (5M)

By the definition of z - transform

$$u(n) = 1 ; \text{ for } n \geq 0$$

$$0 ; n < 0$$

$$X(z) = \sum_{n=-\infty}^{\infty} x(n) z^{-n}$$

$$X(z) = \sum_{n=0}^{\infty} a^n z^{-n}$$

$$X(z) = \sum_{n=0}^{\infty} (a z^{-1})^n$$

Using infinite geometric series sum formula

$$\sum_{n=0}^{\infty} C^n = \frac{1}{1-C}$$

$$X(z) = \frac{z}{z-a}$$

Poles are at $z = a$ (2M)

ROC:

The term $x(n) = a^n u(n)$ converges if $z > a$ (5M)

Given that, $x(n) = -a^n u(-n-1)$

By the definition of z – transform

$u(n) = 1 ; \text{ for } n \geq 0$

$0 ; n < 0$

$$X(z) = \sum_{n=-\infty}^{\infty} x(n)z^{-n}$$

$$X(z) = \sum_{n=0}^{\infty} -a^n z^{-n}$$

$$X(z) = - \sum_{n=0}^{\infty} (az^{-1})^n$$

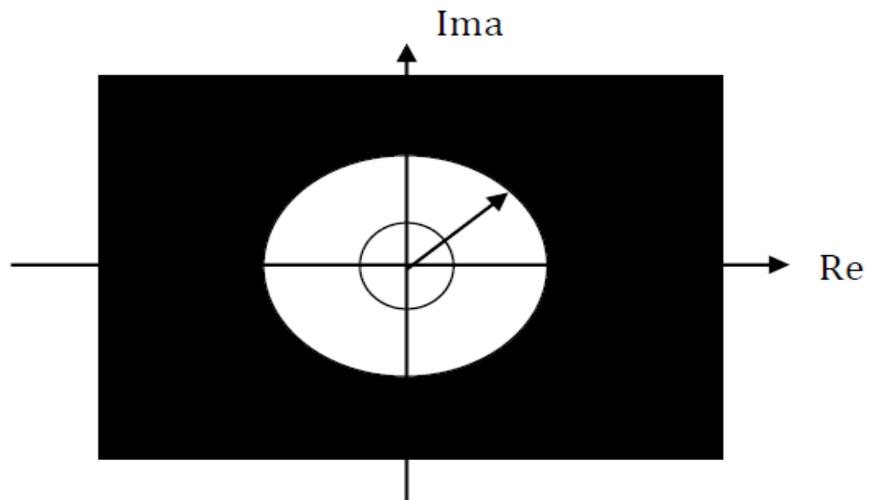
Using infinite geometric series sum formula $\sum_{n=0}^{\infty} c^n = \frac{1}{1-c}$

$$X(z) = - \frac{z}{z-a}$$

Poles are at $z = a$

ROC:

The term $x(n) = -a^n u(-n-1)$ converges if $z > a$ (3)



2. Explain in detail properties of DTFT.(15 marks)[May 2015] -BTL1

Properties of DTFT

Linearity

(2M)

The linearity property of Fourier transform states that the Fourier transform of a linear weighted combination of two or more signals is equal to the similar linear weighted combination of the Fourier transform of the individual signals.

$$\text{DTFT of } x(n) = X(e^{j\omega})$$

$$\text{DTFT of } x_1(n) = X_1(e^{j\omega})$$

$$\text{DTFT of } x_2(n) = X_2(e^{j\omega})$$

$$a x_1(n) + b x_2(n) = a X_1(e^{j\omega}) + b X_2(e^{j\omega})$$

Time shifting property

(4M)

$$\text{Let DTFT of } x(n) = X(e^{j\omega})$$

$$x(n - m) = e^{-j\omega m} X(e^{j\omega})$$

$$x(n + m) = e^{j\omega m} X(e^{j\omega})$$

This relation means that if a signal shifted in time domain by m samples, its magnitude spectrum remains unchanged.

Proof

By definition of Fourier transform

$$X(e^{j\omega}) = \sum_{n=-\infty}^{\infty} x(n) e^{-j\omega n}$$

$$x(n - m) = \sum_{n=-\infty}^{\infty} x(n - m) e^{-j\omega n}$$

$$= \sum_{p=-\infty}^{\infty} x(p) e^{-j\omega(m+p)}$$

$$= \sum_{p=-\infty}^{\infty} x(p) e^{-j\omega m} e^{-j\omega p}$$

$$= e^{-j\omega m} \sum_{p=-\infty}^{\infty} x(p) e^{-j\omega p}$$

$$= e^{-j\omega m} \sum_{n=-\infty}^{\infty} x(n) e^{-j\omega n}$$

$$x(n - m) = e^{-j\omega m} X(e^{j\omega})$$

Convolution theorem of DTFT

(4M)

$$\text{If DTFT of } x_1(n) = X_1(e^{j\omega})$$

$$\text{DTFT of } x_2(n) = X_2(e^{j\omega})$$

$$x_1(n) * x_1(n) = X_1(e^{j\omega}) X_1(e^{j\omega})$$

$$x_1(n) * x_1(n) = \sum_{m=-\infty}^{\infty} x_1(m) x_1(n-m)$$

The Fourier transform of the convolution of $x_1(n)$ and $x_2(n)$ is equal to the product of $X_1(e^{j\omega})$ and $X_2(e^{j\omega})$. It means that if we convolve two signals in time domain, it is equivalent to multiplying their spectra in frequency domain.

Proof

By the definition of Fourier transform,

$$X_1(e^{j\omega}) = \sum_{n=-\infty}^{\infty} x_1(n) e^{-j\omega n}$$

$$X_2(e^{j\omega}) = \sum_{n=-\infty}^{\infty} x_2(n) e^{-j\omega n}$$

$$x_1(n) * x_1(n) = \sum_{n=-\infty}^{\infty} [x_1(n) * x_1(n)] e^{-j\omega n}$$

$$x_1(n) * x_1(n) = \sum_{n=-\infty}^{\infty} \sum_{m=-\infty}^{\infty} [x_1(m) * x_1(n-m)] e^{-j\omega n} e^{-j\omega m} e^{j\omega m}$$

$$x_1(n) * x_1(n) = \sum_{n=-\infty}^{\infty} x_1(m) e^{-j\omega m} \sum_{n=-\infty}^{\infty} [x_1(n-m)] e^{-j\omega(n-m)}$$

$$x_1(n) * x_1(n) = \sum_{m=-\infty}^{\infty} x_1(m) e^{-j\omega m} \sum_{p=-\infty}^{\infty} [x_1(p)] e^{-j\omega p}$$

$$x_1(n) * x_1(n) = X_1(e^{j\omega}) X_1(e^{j\omega})$$

Differentiation in frequency

(5M)

If DTFT of $x(n) = X(e^{j\omega})$, then

$$n x(n) = j \frac{d}{d\omega} X(e^{j\omega})$$

Proof

By the definition of Fourier transform,

$$X(e^{j\omega}) = \sum_{n=-\infty}^{\infty} x(n) e^{-j\omega n}$$

$$= \sum_{n=-\infty}^{\infty} x(n) j \frac{d}{d\omega} e^{-j\omega n}$$

$$= j \sum_{n=-\infty}^{\infty} x(n) [-j n e^{-j\omega n}] \quad \text{note : } -jn = \frac{d}{d\omega}$$

$$= j \sum_{n=-\infty}^{\infty} x(n) \left[\frac{d}{d\omega} e^{-j\omega n} \right]$$

$$= j \frac{d}{d\omega} \sum_{n=-\infty}^{\infty} x(n) [e^{-j\omega n}]$$

$$n x(n) = j \frac{d}{d\omega} X(e^{j\omega})$$

Time reversal property

If DTFT transform of $x(n) = X(e^{j\omega})$

$$x(-n) = X(e^{-j\omega})$$

Proof

By definition of z - transform

$$X(z) = \sum_{n=-\infty}^{\infty} x(n) z^{-n}$$

$$= \sum_{n=-\infty}^{\infty} x(-n) z^{-n} = \sum_{p=-\infty}^{\infty} x(p) z^{-p}$$

$$= \sum_{p=-\infty}^{\infty} x(p) (z^{-1})^{-p}$$

$$X(z) = X(z^{-1})$$

Find inverse z - Transform of X(z)

$$X(z) = \frac{z^{-1}}{1 - 0.25z^{-1} - 0.375z^{-2}}$$

For (i) ROC: $z > 0.75$ and $z < 0.5$

(15 marks) [Nov 2014] -BTL3

Solution

Given that,

$$X(z) = \frac{z^{-1}}{1 - 0.25z^{-1} - 0.375z^{-2}}$$

Multiplying both side on z^2 we get,

3.

$$X(z) = \frac{z}{z^2 - 0.25z - 0.375}$$

Factorize the above equation

$$X(z) = \frac{z}{(z-0.75)(z+0.5)}$$

$$\frac{X(z)}{z} = \frac{1}{(z-0.75)(z+0.5)}$$

By partial fraction expansion technique,

$$\frac{X(z)}{z} = \frac{1}{(z-0.75)(z+0.5)} = \frac{A}{(z-0.75)} + \frac{B}{(z+0.5)} \quad (4)$$

$$\text{if } z = 0.75 \quad A = 0.8$$

$$\text{if } z = -0.5 \quad B = -0.8$$

The poles of $X(z)$ are at, $z = 0.75$ and $z = -0.5$ (3M)

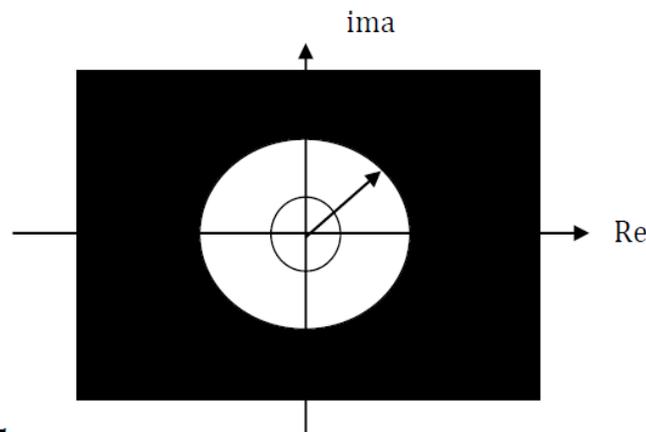
Condition

ROC $z > 0.75$

(4M)

The specified ROC is exterior of the circle whose radius corresponds to the largest pole, hence $x(n)$ will be a causal signal (right sided).

Let take the inverse z -transform of $X(z)$ to get $x(n)$ as causal. $x(n) = 0.8(0.75)^n u(n) - 0.8(-0.5)^n u(n)$



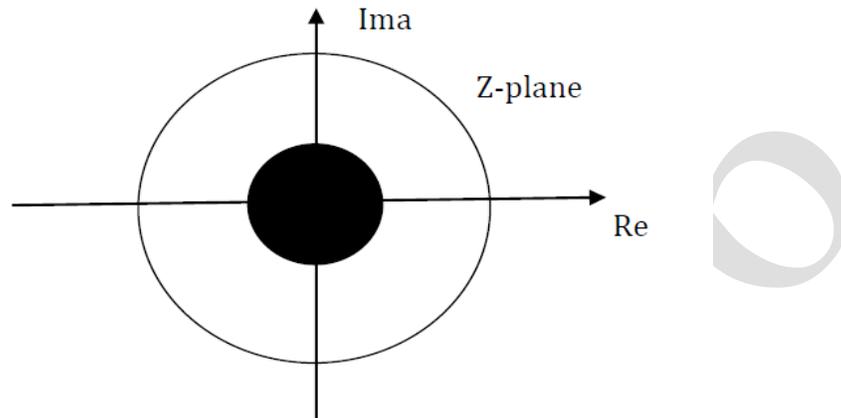
ROC $z < 0.5$

The specified ROC is interior of the circle whose radius corresponds to the smallest pole, hence $x(n)$ will be an anti-causal signal (left sided).

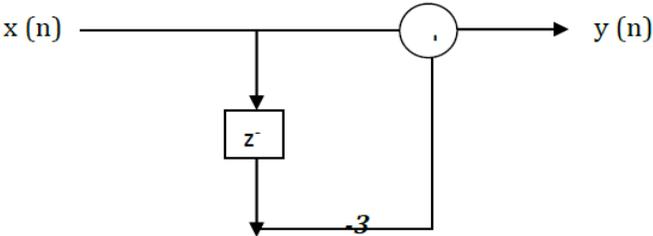
Let take the inverse z – transform of X (z) to get x (n) as causal. $x (n) = - 0.8 (0.75)^n u (-n-1) + 0.8 (-0.5)^n u (-n-1)$ (4M)

Let take the inverse z – transform of X (z) to get x (n) as causal.

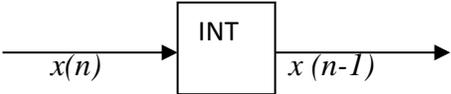
$$x (n) = - 0.8 (0.75)^n u (-n-1) + 0.8 (-0.5)^n u (-n-1)$$

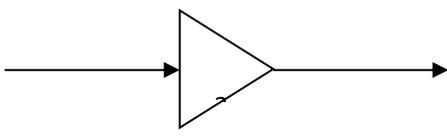
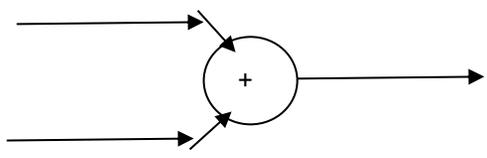


UNIT V- LINEAR TIME INVARIANT-DISCRETE TIME SYSTEMS	
Impulse response – Difference equations-Convolution sum- Discrete Fourier Transform and Z Transform Analysis of Recursive & Non-Recursive systems-DT systems connected in series and parallel.	
PART A	
Q.No	Questions
1.	<p>Determine the Z-Transform of the following two signals. Note that the Z-Transform for both have the same algebraic expression and differ only in the ROC. (May 2019)-BTL3</p> <p>i. $x(n) = \left(\frac{1}{2}\right)^n u(n)$</p> <p>ii. $x(n) = -\left(\frac{1}{2}\right)^n u(-n-1)$</p> <p>Solution</p> $X(Z) = \sum_{n=-\infty}^{\infty} x(n)z^{-n}$ $X(Z) = \sum_{n=0}^{\infty} \left(\frac{1}{2}z^{-1}\right)^n$ $X(Z) = \frac{z}{z-\frac{1}{2}} ; Z > \frac{1}{2}$ $X(Z) = \frac{z}{z-\frac{1}{2}} ; Z < \frac{1}{2}$
2.	<p>Find the initial and final value of the function, (May 2019)-BTL1</p> $X(z) = \frac{1+z^{-1}}{1-0.25z^{-2}}$ <p>Solution</p> <p>Initial value</p> $x(0) = \lim_{z \rightarrow \infty} X(z)$ $x(0) = \lim_{z \rightarrow \infty} \frac{1+z^{-1}}{1-0.25z^{-2}}$ $x(0) = 1$ <p>Final value theorem</p> $x(\infty) = \lim_{z \rightarrow \infty} (1+z^{-1})X(z)$ $x(\infty) = 0$

3	<p>The input $x(n]$ and output $y(n]$ of a discrete time LTI system is given as $x(n) = \{1, 2, 3, 4\}$ and $y(n) = \{0, 1, 2, 3, 4\}$. Find the impulse response $h(n)$. (Nov 2018)-BTL3</p> $h(n) = \frac{y(n)}{x(n)}$ $X(z) = 1 + 2z^{-1} + 3z^{-2} + 4z^{-3}$ $Y(z) = z^{-1} + 2z^{-2} + 3z^{-3} + 4z^{-4}$
4.	<p>Find the difference equation representation of the system. (Nov 2018)-BTL3</p> $H(z) = \frac{z^{-1}}{z^{-2} + 2z^{-1} + 4}$ <p>Solution Difference equation, $y(n-2) + 2y(n-1) + 4y(n) = x(n-1)$</p>
5	<p>Write the condition for stability of a DT-LTI system with respect to the Position of poles. (Nov 2017)-BTL1</p> <p>Solution LTI system is stable, $\sum_{n=-\infty}^{\infty} h(n) < \infty$ Absolutely integral. ROC of $H(s)$ An LTI system is stable if and only if ROC of the system function $H(s)$ include $j\omega$ axis.</p>
6	<p>Realize the difference equation $y(n) = x(n) - 3x(n-1]$ in direct form – 1 (Nov 2017)-BTL6</p> $y(n) = x(n) - 3x(n-1]$ 
7	<p>What is the necessary and sufficient condition on impulse response for Stability of a causal LTI system? [May 2017] -BTL1 (or) In terms of ROC, state the condition for an LTIDT system to be Causal and stable. [Nov 2014]R13 Define stability in LTI system. [May 2015] A stable discrete time system the ROC of impulse response should include the unit circle.</p>

	<p>Condition for stability</p> <p>On combining the condition for location of poles and the ROC, for a stable LTI discrete time system the poles should lie inside the unit circle and the unit circle should be included in ROC of impulse response of the system.</p>																
8	<p>What is the difference between recursive and non-recursive systems?[May 2017] Distinguish between recursive and non – recursive systems.[Nov 2015]-BTL2</p> <table border="1"> <thead> <tr> <th>Recursive systems</th> <th>Non – Recursive systems</th> </tr> </thead> <tbody> <tr> <td>A system whose output $y(n)$ at time n depends on any number of past output values as well as present and past inputs is called recursive system.</td> <td>A system whose output does not depend on past output but depends only on the present and past input is called non-recursive system.</td> </tr> <tr> <td>IIR system are called recursive system</td> <td>FIR system are called non-recursive system</td> </tr> <tr> <td>$y(n) = y(n-1), y(n-2), \dots, x(n), x(n-1), \dots$</td> <td>$y(n) = x(n), x(n-1), \dots$</td> </tr> </tbody> </table>	Recursive systems	Non – Recursive systems	A system whose output $y(n)$ at time n depends on any number of past output values as well as present and past inputs is called recursive system.	A system whose output does not depend on past output but depends only on the present and past input is called non-recursive system.	IIR system are called recursive system	FIR system are called non-recursive system	$y(n) = y(n-1), y(n-2), \dots, x(n), x(n-1), \dots$	$y(n) = x(n), x(n-1), \dots$								
Recursive systems	Non – Recursive systems																
A system whose output $y(n)$ at time n depends on any number of past output values as well as present and past inputs is called recursive system.	A system whose output does not depend on past output but depends only on the present and past input is called non-recursive system.																
IIR system are called recursive system	FIR system are called non-recursive system																
$y(n) = y(n-1), y(n-2), \dots, x(n), x(n-1), \dots$	$y(n) = x(n), x(n-1), \dots$																
9	<p>Define the non-recursive system. May 2016/R13-BTL1</p> <p>Non recursive system. A system whose output does not depend on past output but depends only on the present and past input is called non-recursive system. FIR system are called non-recursive system Examples $y(n) = x(n), x(n-1), \dots$</p>																
10	<p>Convolve following sequence $x(n) = \{1, 2, 3\}$ $h(n) = \{1, 1, 2\}$ May 2018, Nov 2016-BTL3</p> <p>Solution Given that, $x(n) = \{1, 2, 3\}$ & $h(n) = \{1, 1, 2\}$</p> <table border="1"> <tr> <td>$x(n)/$ $h(n)$</td> <td>1</td> <td>1</td> <td>2</td> </tr> <tr> <td>1</td> <td>1</td> <td>1</td> <td>2</td> </tr> <tr> <td>2</td> <td>2</td> <td>2</td> <td>4</td> </tr> <tr> <td>3</td> <td>3</td> <td>3</td> <td>6</td> </tr> </table> <p>$y(n) = \{1, 3, 7, 7, 6\}$</p>	$x(n)/$ $h(n)$	1	1	2	1	1	1	2	2	2	2	4	3	3	3	6
$x(n)/$ $h(n)$	1	1	2														
1	1	1	2														
2	2	2	4														
3	3	3	6														

<p>11</p>	<p>Given the system function $H(z) = 2 + 3z^{-1} + 4z^{-3} - 5z^{-4}$. Determine impulse Response $h(n)$. [Nov 2016]R13-BTL2 Solution Given that, $H(z) = 2 + 3z^{-1} + 4z^{-3} - 5z^{-4}$ Impulse response $h(n)$ $H(z) = 2 + 3z^{-1} + 4z^{-3} - 5z^{-4}$ Take the inverse z transform $h(n) = \{2, 3, 4, -5\}$</p>																
<p>12</p>	<p>From discrete convolution sum, find the step response in terms of $h(n)$. [May 2016]R13-BTL3 Solution The Discrete or linear convolution sum can be defined as, $X(z) = \sum_{m=-\infty}^{\infty} x_1(n) x_2(n - m)$ In terms of $h(n)$? $H(z) = \sum_{m=-\infty}^{\infty} h_1(n) h_2(n - m)$</p>																
<p>13</p>	<p>Convolve the following signals, $x(n) = \{1, 1, 3\}$ and $h(n) = \{1, 4, -1\}$ [Nov 2015] -BTL3 Solution Given that, $x(n) = \{1, 1, 3\}$ and $h(n) = \{1, 4, -1\}$</p> <table border="1" data-bbox="764 1144 1294 1472"> <tr> <td>x (n)/ h (n)</td> <td>1</td> <td>4</td> <td>-1</td> </tr> <tr> <td>1</td> <td>1</td> <td>4</td> <td>-1</td> </tr> <tr> <td>1</td> <td>1</td> <td>4</td> <td>-1</td> </tr> <tr> <td>3</td> <td>3</td> <td>12</td> <td>-3</td> </tr> </table> <p>$y(n) = \{1, 5, 6, 11, -3\}$</p>	x (n)/ h (n)	1	4	-1	1	1	4	-1	1	1	4	-1	3	3	12	-3
x (n)/ h (n)	1	4	-1														
1	1	4	-1														
1	1	4	-1														
3	3	12	-3														
<p>14</p>	<p>Name the basic building blocks used in LTIDT system block diagram.[May 2015] -BTL1 unit delay</p> 																

	<p>Constant Multiplier $x(n) \rightarrow a x(n)$</p>  <p>Signal Adder $x_1(n)$ $x_1(n) + x_2(n)$ $x_2(n)$</p> 
15	<p>Write the n^{th} order difference equation. [May 2015], [Nov 2014] -BTL1</p> <p>In general, the time domain representation of an N^{th} order IIR system is,</p> $y(n) = -\sum_{m=1}^N a_m y(n-m) + \sum_{m=1}^N b_m x(n-m)$ <p>The z domain representation of an N^{th} order IIR system is,</p> $H(z) = \frac{Y(z)}{X(z)} = \frac{b_0 + b_1 z^{-1} + b_2 z^{-2} + \dots + b_M z^{-M}}{1 + a_1 z^{-1} + a_2 z^{-2} + \dots + a_N z^{-N}}$
16	<p>A causal LTI system has impulse response $h(n)$, for which the z-Transform is $H(z) = \frac{1+z^{-1}}{(1-0.5z^{-1})(1+0.25z^{-1})}$ is the system stable? Explain</p> <p style="text-align: right;">[Nov 2012, May 2016] -BTL2</p> <p>Solution</p> <p>Given that, $H(z) = \frac{1+z^{-1}}{(1-0.5z^{-1})(1+0.25z^{-1})}$</p> <p>Multiplying both Nr and Dr by z^2 we get,</p> $H(z) = \frac{z^2+z}{(z-0.5)(z+0.25)}$ <p>The poles of $H(z)$ lie at $z = 0.5$ and $z = -0.25$</p> <p>When ROC is $z > 0.5$, the impulse response $h(n)$ is right sided signal.</p> <p>The ROC includes the unit circle. Hence the system is stable.</p> <p>The impulse response is right sided signal. Hence the system is causal.</p>
17	<p>Using z-Transform, check whether the following system is stable,</p> $H(z) = \frac{z}{z-1/2} + \frac{2z}{z-3}$ <p style="text-align: right;">[May 2014] -BTL4</p> <p>Solution</p> <p>Given that, $H(z) = \frac{z}{z-1/2} + \frac{2z}{z-3}$</p> <p>ROC: $0.5 < z < 3$</p>

	<p>The impulse response $h(n)$ is two sided signal. Since $z > 0.5$, the term with pole $z = 0.5$ corresponds to right sided signal. Since $z < 3$, term with pole $z = 3$ corresponds to left sided signal.</p> $H(z) = \frac{z}{z-1/2} + \frac{2z}{z-3}$ <p>Take inverse z transform,</p> $h(n) = (0.5)^n u(n) - 2(3)^n u(-n-1)$ <p>Here the ROC includes the unit circle but one of the pole lie outside the unit circle and hence the system is unstable.</p>
18	<p>Define convolution sum with its equation. [Nov 2013] -BTL1</p> <p>Convolution sum</p> <p>The Discrete or linear convolution sum can be defined as,</p> $x_3(n) = \sum_{m=-\infty}^{\infty} x_1(n) x_2(n-m) \quad (\text{or})$ $x_3(n) = \sum_{m=-\infty}^{\infty} x_2(n) x_1(n-m)$ <p>Where,</p> <p>$x_3(n)$ is the sequence obtained by convolving $x_1(n)$ and $x_2(n)$</p> <p>m is a dummy variable</p> <p>The convolution relation can be expressed as,</p> $x_3(n) = x_1(n) * x_2(n) = x_2(n) * x_1(n)$ <p>Where, * indicates convolution operation.</p>
19	<p>If $X(\omega)$ is the DTFT of $x(n)$, what is the DTFT of $x^*(-n)$ [May 2013] -BTL1</p> <p>Solution</p> <p>By time reversal property,</p> $x(n) = X(e^{j\omega}), \text{ then}$ $x(-n) = X(e^{-j\omega})$ <p>By conjugation property,</p> $x(n) = X(e^{j\omega}), \text{ then}$ $x^*(n) = X^*(e^{-j\omega})$ $x^*(-n) = X^*(e^{j\omega})$
20	<p>Give the impulse response of a linear time invariant as $h(n) = \sin \pi n$. Check whether the system is stable or not. [Nov 2014] -BTL2</p> <p>Solution</p> <p>Given that, $h(n) = \sin \pi n$</p> <p>The condition for the stability of a system is,</p>

	$\sum_{n=-\infty}^{\infty} h(n) < \infty$ $\sum_{n=-\infty}^{\infty} h(n) = \sum_{n=-\infty}^{\infty} \sin \pi n $ <p>Sin θ lies between -1 and 1 for all θ. The output is bounded for any value of input and therefore the given system is stable.</p>															
<p>21</p>	<p>Convolve the following two sequences: $x(n) = \{1,1,1,1\}$ $h(n) = \{3,2\}$ [Nov 2012, May 2016] – BTL3</p> <p>Solution</p> <p>Given that, $x(n) = \{1, 1, 1, 1\}$ and $h(n) = \{3, 2\}$</p> <table border="1" data-bbox="592 751 1122 1094"> <tr> <td>x (n)/ h (n)</td> <td>1</td> <td>1</td> <td>1</td> <td>1</td> </tr> <tr> <td>3</td> <td>3</td> <td>3</td> <td>3</td> <td>3</td> </tr> <tr> <td>2</td> <td>2</td> <td>2</td> <td>2</td> <td>2</td> </tr> </table> <p>$y(n) = \{3, 5, 5, 5, 2\}$</p>	x (n)/ h (n)	1	1	1	1	3	3	3	3	3	2	2	2	2	2
x (n)/ h (n)	1	1	1	1												
3	3	3	3	3												
2	2	2	2	2												
<p>22</p>	<p>List the steps involved in linear convolution. <i>[May 2015]R08-BTL1</i></p> <ul style="list-style-type: none"> • Procedure • change of index • folding • shifting • multiplication • summation 															
<p>23</p>	<p>Find the overall impulse response $h(n)$ when two systems $h_1(n) = u(n)$ $h_2(n) = \delta(n) + 2\delta(n-1)$ are in series. <i>[May 2014]R08-BTL3</i></p> <p>Solution</p> <p>Given that, $h_1(n) = u(n)$ and $h_2(n) = \delta(n) + 2\delta(n-1)$</p> <p>Let $h(n)$ be the impulse response of the cascade system. Now $h(n)$ is given by convolution of $h_1(n)$ and $h_2(n)$.</p> $h(n) = h_1(n) * h_2(n)$															

	$= u(n) * \{\delta(n) + 2\delta(n-1)\}$ <div style="border: 1px solid black; padding: 5px; margin: 5px auto; width: fit-content;"> <p>Note : $x(n) * \delta(n) = x(n)$ $x(n) * \delta(n-1) = x(n-1)$</p> </div> $= u(n) * \delta(n) + 2 u(n) \delta(n-1)$ $h(n) = u(n) + 2 u(n-1)$				
24	<p>What is the relationship between Fourier Transform and DFT? –BTL2</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 50%; text-align: center;">Fourier Transform</th> <th style="width: 50%; text-align: center;">DFT</th> </tr> </thead> <tbody> <tr> <td style="vertical-align: top;"> <ul style="list-style-type: none"> Gives the frequency information for an aperiodic signal Continuous frequency spectrum </td> <td style="vertical-align: top;"> <ul style="list-style-type: none"> Obtained by performing sampling operation in both the time and frequency spectrum Discrete frequency spectrum </td> </tr> </tbody> </table>	Fourier Transform	DFT	<ul style="list-style-type: none"> Gives the frequency information for an aperiodic signal Continuous frequency spectrum 	<ul style="list-style-type: none"> Obtained by performing sampling operation in both the time and frequency spectrum Discrete frequency spectrum
Fourier Transform	DFT				
<ul style="list-style-type: none"> Gives the frequency information for an aperiodic signal Continuous frequency spectrum 	<ul style="list-style-type: none"> Obtained by performing sampling operation in both the time and frequency spectrum Discrete frequency spectrum 				
25	<p>State the properties of DFT? –BTL1</p> <ul style="list-style-type: none"> Periodicity Linearity and symmetry Multiplication of two DFTs Circular convolution Time reversal Circular time shift and frequency shift Complex conjugate Circular correlation 				
	PART B				
Q,N o	Questions				
1	<p>Perform convolution to find the response of the system $h_1(n)$ and $h_2(n)$ for the input sequences $x_1(n)$ and $x_2(n)$ respectively.</p> <p>$x_1(n) = \{1, -1, 2, 3\}$ $h_1(n) = \{1, -2, 3, -1\}$ $x_2(n) = \{1, 2, 3, 2\}$ $h_2(n) = \{1, 2, 2\}$ [May 2017] -BTL3 (13M)</p> <p>Solution Given that, $x_1(n) = \{1, -1, 2, 3\}$ $h_1(n) = \{1, -2, 3, -1\}$ $y(n) = x(n) * h(n)$ Where $y(n)$ is the response of the system</p>				

$x(n)$ is the input of the system
 $h(n)$ is the impulse response of the system
 Using linear or tabular convolution (6M)

$x_1(n)/$ $h_1(n)$	1	-1	2	3
1	1	-1	2	3
-2	-2	2	-4	-6
3	3	-3	6	9
-1	-1	1	-2	-3

The response of the system is,
 $y_1(n) = \{1, -3, 7, -5, 1, 7, -3\}$

Given that, $x_2(n) = \{1, 2, 3, 2\}$

$h_1(n) = \{1, 2, 2\}$

(6M)

$x_1(n)/$ $h_1(n)$	1	2	3	2
1	1	2	3	2
2	2	4	6	4
2	2	4	6	4

The response of the system is,
 $y(n) = \{1, 4, 9, 12, 10, 4\}$

2

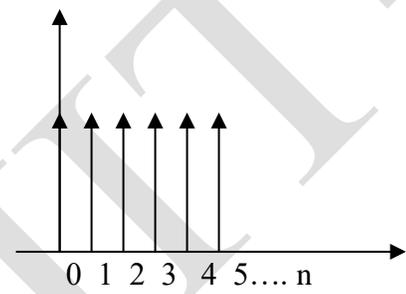
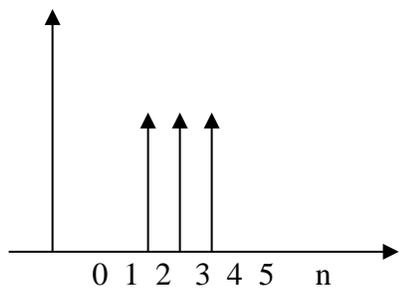
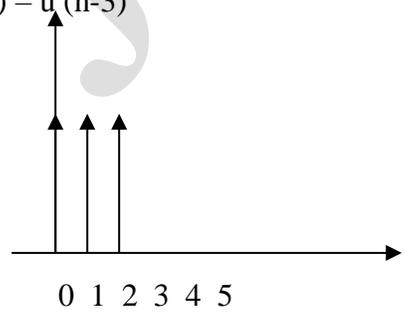
For a causal LTI system the input $x(n)$ and output $y(n)$ are related through a difference equation $y(n) - 1/6 y(n-1) - 1/6 y(n-2) = x(n)$. Determine the frequency response $H(e^{j\omega})$ and the impulse response $h(n)$ of the system.(13) [May 2017] -BTL3

Solution

Given that, $y(n) - 1/6 y(n-1) - 1/6 y(n-2) = x(n)$

Taking the z -transform of the above equation,

$$Y(z) - \frac{1}{6} Y(z)z^{-1} - \frac{1}{6} Y(z)z^{-2} = X(z)$$

	<p> $Y(z) \left\{ -\frac{1}{6}z^{-1} - \frac{1}{6}z^{-2} \right\} = X(z)$ $H(z) = \frac{Y(z)}{X(z)}$ $H(z) = \frac{1}{-\frac{1}{6}z^{-1} - \frac{1}{6}z^{-2}} \quad (4M)$ <p>Multiplying both Nr and Dr by z^2 we get,</p> $H(z) = \frac{z^2}{-\frac{1}{6}z - \frac{1}{6}}$ $H(z) = \frac{z^2}{-\frac{1}{6}(z+1)}$ <p>Frequency response (5M)</p> <p>put $z = e^{j\omega}$</p> $H(e^{j\omega}) = \frac{e^{j2\omega}}{-\frac{1}{6}(e^{j\omega} + 1)}$ $H(e^{j\omega}) = \frac{-6 e^{j2\omega}}{(e^{j\omega} + 1)}$ <p>h(n) calculation (4M)</p> </p>
<p>3</p>	<p>Convolve the following signals,</p> <p>$x(n) = u(n) - u(n-3)$</p> <p>$h(n) = 0.5^n u(n)$ (13M)[Nov 2016] -BTL-3</p> <p>Solution</p> <p>Given that, $x(n) = u(n) - u(n-3)$</p> <p>$h(n) = 0.5^n u(n)$ (7M)</p> <p>Solve $x(n) = u(n) - u(n-3)$</p> <div style="display: flex; justify-content: space-around;"> <div style="text-align: center;"> <p>u(n)</p>  </div> <div style="text-align: center;"> <p>u(n-3)</p>  </div> </div> <div style="text-align: center; margin-top: 20px;"> <p>u(n) - u(n-3)</p>  </div>

$$x(n) = u(n) - u(n - 3)$$

$$x(n) = 1 ; \text{ for } 0, 0 < n < 2$$

The Discrete or linear convolution sum can be defined as, (6M)

$$y(n) = \sum_{m=-\infty}^{\infty} x(m) \delta(n - m)$$

$$y(n) = \sum_{m=-\infty}^{\infty} \left(\frac{1}{2}\right)^2 u(n - m + 2)$$

$$y(n) = \sum_{m=2}^n \left(\frac{1}{2}\right)^2$$

Determine whether the given system is stable by finding H (z) and plotting the pole zero diagrams. $y(n) = 2y(n-1)-0.8y(n-2)+x(n)+0.8x(n-1)$ (13M)[Nov 2016] -BTL3

Solution

Given that, $y(n) = 2y(n-1)-0.8y(n-2)+x(n)+0.8x(n-1)$

Transfer function H (z)

Taking the z – transform of the above equation we get,

$$Y(z) = 2 Y(z) z^{-1} - 0.8 Y(z) z^{-2} + X(z) + 0.8 X(z) z^{-1}$$

$$Y(z) - 2 Y(z) z^{-1} + 0.8 Y(z) z^{-2} = X(z) + 0.8 X(z) z^{-1}$$

$$Y(z) [1 - 2 z^{-1} + 0.8 z^{-2}] = X(z) [1 + 0.8 z^{-1}]$$

$$H(z) = \frac{1+0.8z^{-1}}{1-2z^{-1}+0.8z^{-2}} \tag{5M}$$

Multiplying both Nr and Dr by z^2 , then we get

$$H(z) = \frac{z^2+0.8z}{z^2-2z+0.8}$$

Hence, H (z) is called transfer function

Poles and zero

$$H(z) = \frac{z^2+0.8z}{z^2-2z+0.8}$$

4.

Factorize the above term we get,

$$H(z) = \frac{z(z+0.8)}{(z-1.447)(z-0.552)}$$

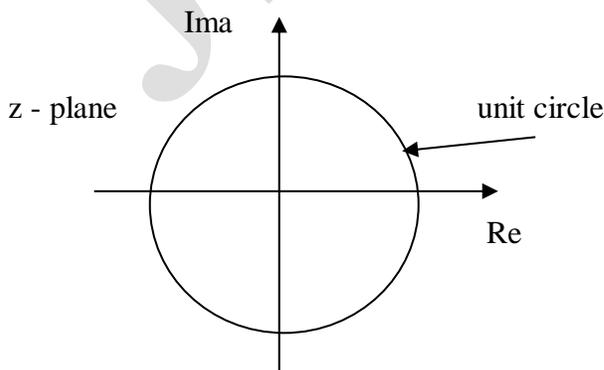
The poles of the denominator term are, (5M)

$$p1 = 1.447, p2 = 0.552$$

The zero of the numerator term,

$$z_1 = 0 \text{ and } z_2 = -0.8$$

Pole zero diagrams (3M)



Realize the following system in cascade form,

$$H(z) = \frac{1 + \frac{1}{5}z^{-1}}{\left(1 - \frac{1}{2}z^{-1} + \frac{1}{3}z^{-2}\right)\left(1 + \frac{1}{4}z^{-1}\right)} \quad (10 \text{ marks}) \quad [\text{May 2016}] - \text{BTL3}$$

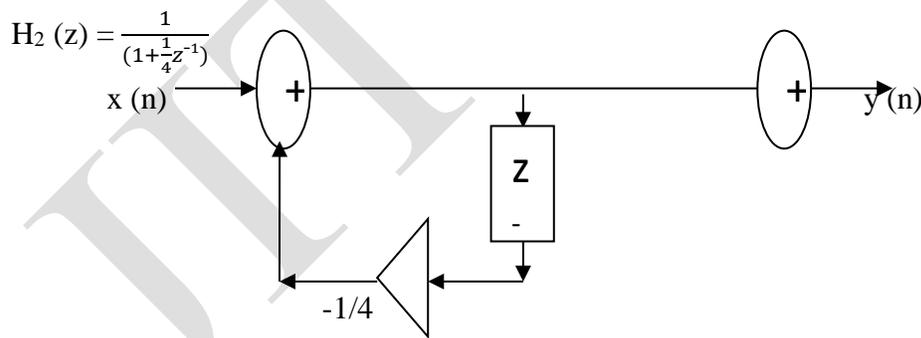
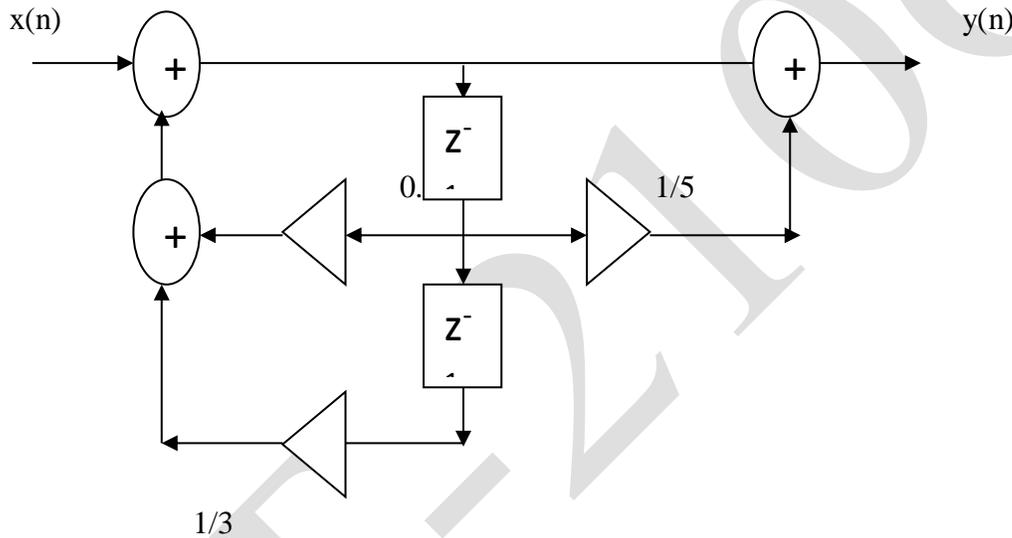
Solution

Given that,
$$H(z) = \frac{1 + \frac{1}{5}z^{-1}}{\left(1 - \frac{1}{2}z^{-1} + \frac{1}{3}z^{-2}\right)\left(1 + \frac{1}{4}z^{-1}\right)}$$

$$H_1(z) = \frac{1 + \frac{1}{5}z^{-1}}{\left(1 - \frac{1}{2}z^{-1} + \frac{1}{3}z^{-2}\right)}$$

Using Direct form – II

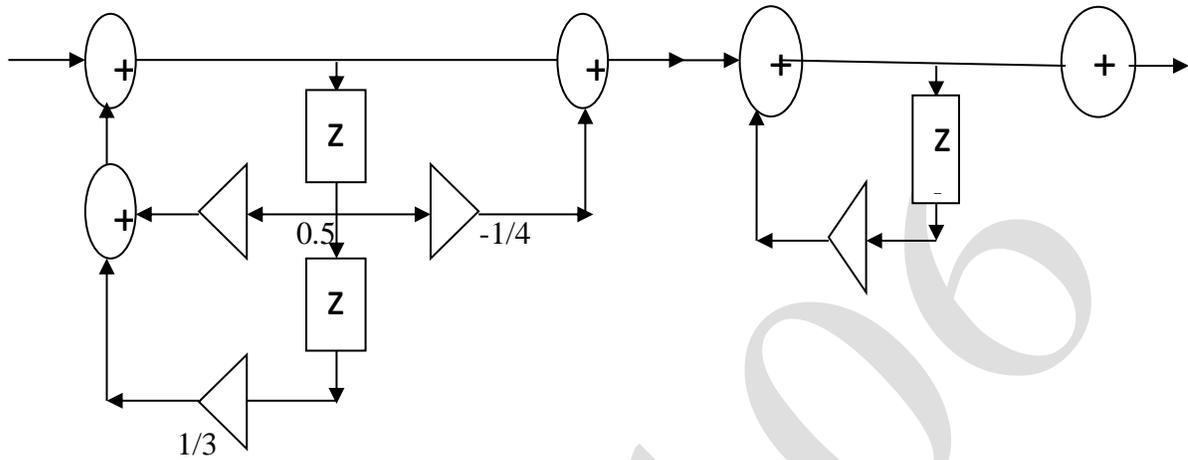
(5M)



5

Cascade form

(5M)



Convolve $x(n) = \{1, 1, 0, 1, 1\}$ and $h(n) = \{1, -2, -3, 4\}$ (6M)[May 2016] -BTL3

Solution

Given that,

$x(n) = \{1, 1, 0, 1, 1\}$ and

$h(n) = \{1, -2, -3, 4\}$

(6M)

6

$x_1(n)/h_1(n)$	-3	-2	-1	0	1	2
		1	1	0	1	1
-3	1	1	1	0	1	1
-2	-2	-2	-2	0	-2	-2
-1	-3	-3	-3	0	-3	-3
0	4	4	4	0	4	4

The response of the system is

$$y(n) = \{1, -1, -5, 2, 3, -5, 1, 4\}$$

7	<p>A system is governed by a linear constant coefficient difference Equation, $y(n) = 0.7 y(n-1) - 0.1 y(n-2) + 2 x(n) - x(n-2)$ find the Output response of the system $y(n)$ for an $x(n) = u(n)$ (16 marks) [May 2016] -BTL3</p> <p>Solution</p> <p>Given that, $y(n) = 0.7 y(n-1) - 0.1 y(n-2) + 2 x(n) - x(n-2)$ $x(n) = u(n)$ $y(n) = 0.7 y(n-1) - 0.1 y(n-2) + 2 x(n) - x(n-2)$ Taking z – transform of the above equation $Y(z) = 0.7 Y(z) z^{-1} - 0.1 Y(z) z^{-2} + 2 X(z) - X(z) z^{-2}$ $Y(z) - 0.7 Y(z) z^{-1} + 0.1 Y(z) z^{-2} = 2 X(z) - X(z) z^{-2}$ $Y(z) [1 - 0.7 z^{-1} + 0.1 z^{-2}] = X(z) [2 - z^{-2}]$ $H(z) = \frac{Y(z)}{X(z)} \quad (4M)$</p> $H(z) = \frac{2 - z^{-2}}{1 - 0.7z^{-1} + 0.1z^{-2}}$ <p>Multiplying both Nr and Dr by z^2</p> $H(z) = \frac{2z^2 - 1}{z^2 - 0.7z + 0.1}$ <p>Factorize the above equation</p> $H(z) = \frac{2z^2 - 1}{(z - 0.2)(z - 0.5)}$ <p>Hence above $H(z)$ is called transfer function.</p> <p>Response of the system</p> $y(n) = x(n) h(n) \quad (7M)$ <p>Given input signal, $x(n) = u(n)$ Taking the z transform of the equation $X(z) = \frac{z}{z-1}$</p> $Y(z) = X(z) H(z)$ $Y(z) = \frac{z}{z-1} \frac{2z^2 - 1}{(z - 0.2)(z - 0.5)}$ $\frac{Y(z)}{z} = \frac{2z^2 - 1}{(z - 0.2)(z - 0.5)(z - 1)}$ <p>By the partial fraction expansion technique</p> $\frac{Y(z)}{z} = \frac{2z^2 - 1}{(z - 0.2)(z - 0.5)(z - 1)} = \frac{A}{(z - 0.2)} + \frac{B}{(z - 0.5)} + \frac{C}{(z - 1)}$ <p>If $z = 0.2$ $A = -3.833$ If $z = 0.5$ $B = 3.33$ If $z = 1$ $C = 6.666$</p> $\frac{Y(z)}{z} = \frac{-3.833}{(z - 0.2)} + \frac{3.33}{(z - 0.5)} + \frac{6.666}{(z - 1)} \quad (5M)$
---	--

	$Y(z) = \frac{-3.833z}{(z-0.2)} + \frac{3.33z}{(z-0.5)} + \frac{6.66z}{(z-1)}$ <p>Taking the inverse z –transform</p> $y(n) = -3.833 (0.2)^n u(n) + 3.33 (0.5)^n u(n) + 6.66 (1)^n u(n)$
8	<p>Determine the impulse response and step response $y(n) + y(n-1) - 2y(n-2) = x(n-1) + 2x(n-2)$ (10 marks) [May 2015] -BTL-3</p> <p>Solution</p> <p>Given that, $y(n) + y(n-1) - 2y(n-2) = x(n-1) + 2x(n-2)$</p> <p>Impulse response</p> <p>The difference equation system is,</p> $y(n) + y(n-1) - 2y(n-2) = x(n-1) + 2x(n-2)$ <p>Taking z transform of the above equation</p> $(z) + Y(z)z^{-1} - 2Y(z)z^{-2} = X(z)z^{-1} + 2X(z)z^{-2}$ $Y(z)[1 + z^{-1} - 2z^{-2}] = X(z)[z^{-1} + 2z^{-2}]$ $H(z) = \frac{Y(z)}{X(z)}$ $H(z) = \frac{z^{-1} + 2z^{-2}}{1 + z^{-1} - 2z^{-2}} \quad (5M)$ <p>Multiplying both Nr and Dr by z^2</p> $H(z) = \frac{z + 2}{z^2 + z - 2}$ <p>Factorize the above term we get</p> $H(z) = \frac{z + 2}{(z-1)(z+2)}$ $H(z) = \frac{1}{(z-1)}$ <p>Hence H(z) is called transfer function</p> <p>Taking the inverse z transform</p> $h(t) = u(n)$ <p>Step response</p> <p>Input, $x(n) = u(n)$ (5M)</p> $X(z) = \frac{z}{(z-1)}$ <p>Output response,</p> $Y(z) = X(z)H(z)$ $Y(z) = \frac{z}{(z-1)} \frac{1}{(z-1)}$ $Y(z) = \frac{z}{(z-1)^2}$ <p>Taking the inverse z transform we get</p> $y(n) = n u(n)$

A causal system has $x(n) = \delta(n) = \frac{1}{4}\delta(n-1) - \frac{1}{8}\delta(n-2)$ and $y(n) = \delta(n) - \frac{3}{4}\delta(n-1)$. find impulse response and output if $x(n) = (1/2)^n u(n)$ (12M)[May 2015] -BTL3

Solution

Given that, $x(n) = \delta(n) = \frac{1}{4}\delta(n-1) - \frac{1}{8}\delta(n-2)$ and $y(n) = \delta(n) - \frac{3}{4}\delta(n-1)$

$$x(n) = (1/2)^n u(n)$$

Impulse response of the system

$$x(n) = \delta(n) = \frac{1}{4}\delta(n-1) - \frac{1}{8}\delta(n-2)$$

Taking the z transform of the above equation

$$X(z) = 1 + \frac{1}{4}z^{-1} - \frac{1}{8}z^{-2}$$

$$y(n) = \delta(n) - \frac{3}{4}\delta(n-1)$$

Taking the z transform of the above equation

$$Y(z) = 1 - \frac{3}{4}z^{-1} \quad (4M)$$

Transfer function,

$$H(z) = \frac{Y(z)}{X(z)}$$

$$H(z) = \frac{1 - \frac{3}{4}z^{-1}}{1 + \frac{1}{4}z^{-1} - \frac{1}{8}z^{-2}}$$

Multiplying Nr and Dr by z^2 we get,

$$H(z) = \frac{z^2 - \frac{3}{4}z}{z^2 + \frac{1}{4}z - \frac{1}{8}}$$

Factorize the above term,

$$H(z) = \frac{z(z - \frac{3}{4})}{(z - \frac{1}{4})(z + \frac{1}{2})} \quad (4M)$$

$$\frac{H(z)}{z} = \frac{(z - \frac{3}{4})}{(z - \frac{1}{4})(z + \frac{1}{2})}$$

By using partial fraction expansion technique,

$$\frac{H(z)}{z} = \frac{(z - \frac{3}{4})}{(z - \frac{1}{4})(z + \frac{1}{2})} = \frac{A}{(z - \frac{1}{4})} + \frac{B}{(z + \frac{1}{2})}$$

$$\text{if } z = \frac{1}{4} \quad A = \frac{-2}{3}$$

$$\text{if } z = -\frac{1}{2} \quad B = \frac{5}{3}$$

$$\frac{H(z)}{z} = \frac{-\frac{2}{3}}{(z - \frac{1}{4})} + \frac{\frac{5}{3}}{(z + \frac{1}{2})}$$

$$H(z) = \frac{-\frac{2}{3}z}{(z - \frac{1}{4})} + \frac{\frac{5}{3}z}{(z + \frac{1}{2})}$$

Taking inverse z transform

$$h(n) = \frac{-2}{3} \left(\frac{1}{4}\right)^n u(n) + \frac{5}{3} \left(\frac{-1}{2}\right)^n u(n) \quad (4M)$$

Output response

$$x(n) = (1/2)^n u(n)$$

Solution

Given that, $H(z) = \frac{3-4z^{-1}}{1-3.5z^{-1}+1.5z^{-2}}$

Multiply the z^2 both Nr and Dr

$$H(z) = \frac{3z^2-4z}{z^2-3.5z+1.5}$$

Factorize the above equation

$$H(z) = \frac{z(3z-4)}{(z-3)(z-0.5)}$$

$$\frac{H(z)}{z} = \frac{(3z-4)}{(z-3)(z-0.5)}$$

By using partial fraction expansion technique

$$\frac{H(z)}{z} = \frac{(3z-4)}{(z-3)(z-0.5)} = \frac{A}{(z-3)} + \frac{B}{(z-0.5)}$$

if $z = 3$ $A = 2$

if $z = 0.5$ $B = 1$

$$\frac{H(z)}{z} = \frac{2}{(z-3)} + \frac{1}{(z-0.5)}$$

$$H(z) = \frac{2z}{(z-3)} + \frac{z}{(z-0.5)}$$

The poles of $H(z)$ are at $z = 3$ and $z = 0.5$

(5M)

system is stable

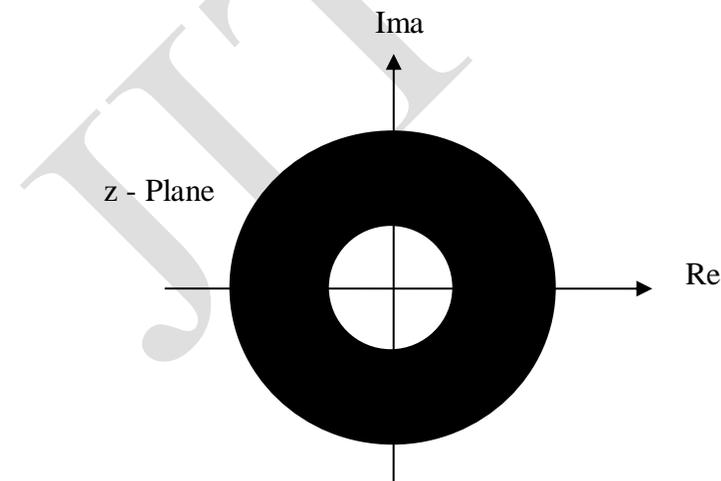
The ROC is stable system should include the unit circle. Therefore ROC is

$$0.5 < z < 3$$

$$H(z) = \frac{2z}{(z-3)} + \frac{z}{(z-0.5)}$$

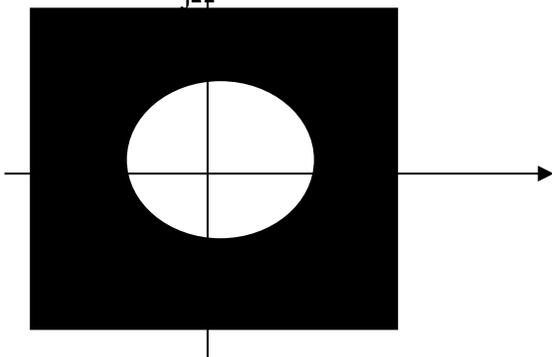
Taking inverse z transform

$$h(n) = -2(3)^n u(-n-1) + 0.5^n u(n)$$



The system is causal

For a causal system the ROC should be exterior of a circle, whose radius is equal to the magnitude of outermost pole.

	<p style="text-align: center;">$h(n) = 2(3)^n u(n) + 0.5^n u(n)$</p>  <p>The system is anti causal For an anti causal system, the ROC should be interior of a circle, whose radius is equal to magnitude of innermost pole. $h(n) = -2(3)^n u(-n-1) - 0.5^n u(-n-1)$</p>
	PART-C
Q.No	Questions
1	<p>LTI discrete time system $y(n) = 3/2 y(n-1) - 1/2 y(n-2) + x(n) + x(n-1)$ Given an input $x(n) = u(n)$ Find the transfer function of the system. Find the impulse response of the system. (15 marks) [Nov 2014] -BTL5</p> <p>Solution Given that, $y(n) = 3/2 y(n-1) - 1/2 y(n-2) + x(n) + x(n-1)$</p> <p>Transfer function The difference equation system is, $y(n) = 3/2 y(n-1) - 1/2 y(n-2) + x(n) + x(n-1)$</p> <p>Taking z transform of the above equation $Y(z) = 3/2 Y(z) z^{-1} - 1/2 Y(z) z^{-2} + X(z) + X(z) z^{-1}$ $Y(z) - 3/2 Y(z) z^{-1} + 1/2 Y(z) z^{-2} = X(z) + X(z) z^{-1}$ $Y(z) [1 - 3/2 z^{-1} + 1/2 z^{-2}] = X(z) [1 + z^{-1}]$</p> $H(z) = \frac{Y(z)}{X(z)}$ $H(z) = \frac{1+z^{-1}}{1-\frac{3}{2}z^{-1}+\frac{1}{2}z^{-2}}$ <p>Multiplying both Nr and Dr by z^2</p> $H(z) = \frac{z^2+z}{z^2-\frac{3}{2}z+\frac{1}{2}}$

	$H(z) = \frac{z^2+z}{z^2-1.5z+0.5}$ <p>Factorize the above term we get</p> $H(z) = \frac{z(z+1)}{(z-1)(z-0.5)} \quad (7)$ <p>Hence H(z) is called transfer function</p> <p>By using partial fraction expansion technique,</p> $\frac{H(z)}{z} = \frac{(z+1)}{(z-1)(z-0.5)} = \frac{A}{(z-1)} + \frac{B}{(z-0.5)}$ <p>If z=1 $A = 4$</p> <p>If z = 1/2 $B = -3$</p> $\frac{H(z)}{z} = \frac{4}{(z-1)} - \frac{3}{(z-0.5)} \quad (5)$ $H(z) = \frac{4z}{(z-1)} - \frac{3z}{(z-0.5)}$ <p>Taking the inverse z transform</p> $h(n) = 4 u(n) - 3 (0.5)^n u(n) \quad (3)$
2.	<p>Convolve the following signals: $x(n) = (1/2)^{n-2} u(n-2)$ and $h(n) = u(n+2)$ (15 marks) [Nov 2015/R13 BTL3]</p> <p>Solution</p> <p>Given that, : $x(n) = (1/2)^{n-2} u(n-2)$ and $h(n) = u(n+2)$</p> $x(n) = \left(\frac{1}{2}\right)^{n-2} u(n-2)$ $x(n) = \left(\frac{1}{2}\right)^{n-2}; n \geq 2$ $x(m) = \left(\frac{1}{2}\right)^{m-2} u(n-2)$ $x(m) = \left(\frac{1}{2}\right)^{m-2}; m \geq 2$ $h(n) = u(n+2) = 1; n \geq -2$ $= 0; n < -2$ $h(m) = u(m+2) = 1; m \geq -2$ $= 0; m < -2 \quad (5M)$ <p>The Discrete or linear convolution sum can be defined as,</p> $x(n) * h(n) = \sum_{m=-\infty}^{\infty} x(m) h(n-m)$ $x(n) * h(n) = \sum_{m=-\infty}^{\infty} \left(\frac{1}{2}\right)^{m-2} u(n-m+2)$ $= \sum_{m=2}^n \left(\frac{1}{2}\right)^m \left(\frac{1}{2}\right)^{-2}$ $= \left(\frac{1}{2}\right)^{-2} \sum_{m=2}^n \left(\frac{1}{2}\right)^m$ $= \left(\frac{1}{2}\right)^{-2} \sum_{m=0}^n \left(\frac{1}{2}\right)^m - \left(\frac{1}{2}\right)^0 - \left(\frac{1}{2}\right)^1$ $= 2^2 \sum_{m=0}^n \left(\frac{1}{2}\right)^m - 1 - \left(\frac{1}{2}\right)^1 \quad (5M)$

finite geometric series sum formula

$$\sum_{n=0}^N c^n = \frac{1 - c^{N+1}}{1 - c}$$

$$= 4 \left[\frac{1 - \left(\frac{1}{2}\right)^{n+1}}{1 - \frac{1}{2}} - \frac{3}{2} \right]$$

$$= 4 \left[2 \left(1 - \left(\frac{1}{2}\right)^n\right) \left(\frac{1}{2}\right) - \frac{3}{2} \right]$$

$$x(n) * h(n) = 2 - \left(\frac{1}{2}\right)^{n-2}; \quad n \geq 2 \quad (5M)$$

Consider an LTI system with impulse response $h(n) = \alpha^n u(n)$ and the input to this system is $x(n) = \beta^n u(n)$ with $\alpha < 1$ and $\beta < 1$. Determine the response $y(n)$.

when $\alpha = \beta$

when $\alpha \neq \beta$ using DTFT

(15 marks) [Nov 2015] -BTL5

Solution

Given that, $h(n) = \alpha^n u(n)$

$x(n) = \beta^n u(n)$

$y(n)$ is the response of the LTI system

$Y(e^{j\omega})$ is the Fourier transform of $y(n)$

The response $y(n)$ of the system is given by the convolution of $x(n)$ and $h(n)$

$$y(n) = x(n) * h(n)$$

On taking Fourier transform of above equation

$$Y(e^{j\omega}) = X(e^{j\omega}) H(e^{j\omega})$$

By definition of Fourier transform

$$X(e^{j\omega}) = \sum_{n=-\infty}^{\infty} x(n) e^{-j\omega n}$$

$$X(e^{j\omega}) = \sum_{n=0}^{\infty} \beta^n e^{-j\omega n}$$

$$X(e^{j\omega}) = \sum_{n=0}^{\infty} (\beta e^{-j\omega})^n$$

Using infinite geometric series sum formula $\sum_{n=0}^{\infty} c^n = \frac{1}{1-c}$

$$X(e^{j\omega}) = \frac{1}{1 - \beta e^{-j\omega}} \quad (5M)$$

By definition of Fourier transform

$$H(e^{j\omega}) = \sum_{n=-\infty}^{\infty} h(n) e^{-j\omega n}$$

$$H(e^{j\omega}) = \sum_{n=0}^{\infty} \alpha^n e^{-j\omega n}$$

$$H(e^{j\omega}) = \sum_{n=0}^{\infty} (\alpha e^{-j\omega})^n$$

Using infinite geometric series sum formula $\sum_{n=0}^{\infty} c^n = \frac{1}{1-c}$

3.

$$H(e^{j\omega}) = \frac{1}{1 - \alpha e^{-j\omega}}$$

$$Y(e^{j\omega}) = \frac{1}{1 - \beta e^{-j\omega}} \frac{1}{1 - \alpha e^{-j\omega}}$$

$$Y(e^{j\omega}) = \frac{e^{j\omega} e^{j\omega}}{(e^{j\omega} - \beta)(e^{j\omega} - \alpha)}$$

Condition

$$\alpha = \beta$$

$$Y(e^{j\omega}) = \frac{e^{j\omega} e^{j\omega}}{(e^{j\omega} - \beta)^2}$$

(5M)

By partial fraction expansion technique

$$\frac{Y(e^{j\omega})}{e^{j\omega}} = \frac{e^{j\omega}}{(e^{j\omega} - \beta)^2}$$

$$\frac{Y(e^{j\omega})}{e^{j\omega}} = \frac{e^{j\omega}}{(e^{j\omega} - \beta)^2} = \frac{A}{(e^{j\omega} - \beta)^2} + \frac{B}{(e^{j\omega} - \beta)}$$

$$\text{if } e^{j\omega} = \beta \quad A = \beta$$

$$B = 1$$

$$\frac{Y(e^{j\omega})}{e^{j\omega}} = \frac{\beta}{(e^{j\omega} - \beta)^2} + \frac{1}{(e^{j\omega} - \beta)}$$

$$Y(e^{j\omega}) = \frac{\beta e^{j\omega}}{(e^{j\omega} - \beta)^2} + \frac{e^{j\omega}}{(e^{j\omega} - \beta)}$$

The response $y(n)$ is obtained by taking inverse Fourier transform,

$$y(n) = n \beta^n u(n) + \beta^n u(n)$$

(5M)

EC8392

DIGITAL ELECTRONICS

L T P C
3 0 0 3**OBJECTIVES:**

- To present the Digital fundamentals, Boolean algebra and its applications in digital systems
- To familiarize with the design of various combinational digital circuits using logic gates
- To introduce the analysis and design procedures for synchronous and asynchronous sequential circuits
- To explain the various semiconductor memories and related technology
- To introduce the electronic circuits involved in the making of logic gates

UNIT I - DIGITAL FUNDAMENTALS

9

Number Systems – Decimal, Binary, Octal, Hexadecimal, 1's and 2's complements, Codes – Binary, BCD, Excess 3, Gray, Alphanumeric codes, Boolean theorems, Logic gates, Universal gates, Sum of products and product of sums, Minterms and Maxterms, Karnaugh map Minimization and Quine-McCluskey method of minimization.

UNIT II - COMBINATIONAL CIRCUIT DESIGN

9

Design of Half and Full Adders, Half and Full Subtractors, Binary Parallel Adder – Carry look ahead Adder, BCD Adder, Multiplexer, Demultiplexer, Magnitude Comparator, Decoder, Encoder, Priority Encoder.

UNIT III - SYNCHRONOUS SEQUENTIAL CIRCUITS

9

Flip flops – SR, JK, T, D, Master/Slave FF – operation and excitation tables, Triggering of FF, Analysis and design of clocked sequential circuits – Design - Moore/Mealy models, state minimization, state assignment, circuit implementation – Design of Counters- Ripple Counters, Ring Counters, Shift registers, Universal Shift Register.

UNIT IV - ASYNCHRONOUS SEQUENTIAL CIRCUITS

9

Stable and Unstable states, output specifications, cycles and races, state reduction, race free assignments, Hazards, Essential Hazards, Pulse mode sequential circuits, Design of Hazard free circuits.

UNIT V-MEMORY DEVICES AND DIGITAL INTEGRATED CIRCUITS

9

Basic memory structure – ROM -PROM – EPROM – EEPROM –EAPROM, RAM – Static and dynamic RAM Programmable Logic Devices – Programmable Logic Array (PLA) - Programmable Array Logic (PAL) – Field Programmable Gate Arrays (FPGA) - Implementation of combinational logic circuits using PLA, PAL.Digital integrated circuits: Logic levels, propagation delay, power dissipation, fan-out and fan- in, noise margin, logic families and their characteristics-RTL, TTL, ECL, CMOS

TOTAL: 45 PERIODS**OUTCOMES:**

At the end of the course:

- Use digital electronics in the present contemporary world
- Design various combinational digital circuits using logic gates
- Do the analysis and design procedures for synchronous and asynchronous sequential circuits
- Use the semiconductor memories and related technology
- Use electronic circuits involved in the design of logic gates

TEXT BOOKS:

1. M. Morris Mano and Michael D. Ciletti, -Digital Designl, 5th Edition, Pearson, 2014.

REFERENCES

1. Charles H.Roth. -Fundamentals of Logic Designl, 6th Edition, Thomson Learning, 2013.
2. Thomas L. Floyd, -Digital Fundamentalsl, 10th Edition, Pearson Education Inc, 2011
3. S.Salivahanan and S.Arivazhagan-Digital Electronicsl, Ist Edition,Vikas Publishing House pvt Ltd, 2012.
4. Anil K.Maini -Digital Electronicsl, Wiley, 2014.
5. A.Anand Kumar -Fundamentals of Digital Circuitsl, 4th Edition, PHI Learning Private Limited, 2016.
6. Soumitra Kumar Mandal – Digital Electronicsl, McGraw Hill Education Private Limited,2016.

SUBJECT CODE: EC8392

YEAR/SEMESTER : II /03

SUBJECT NAME: DIGITAL ELECTRONICS

SUBJECTHANDLER :MS.R.ANANTHI REETA

UNIT I - DIGITAL FUNDAMENTALS

Number Systems – Decimal, Binary, Octal, Hexadecimal, 1's and 2's complements, Codes – Binary, BCD, Excess 3, Gray, Alphanumeric codes, Boolean theorems, Logic gates, Universal gates, Sum of products and product of sums, Minterms and Maxterms, Karnaugh map Minimization and Quine-McCluskey method of minimization.

PART * A

1.	<p>State Demorgan's Theorem.[April/May-2010,2011,May/June-2013, Nov/Dec- 2010](BTL1)</p> <p>De Morgan suggested two theorems that form important part of Boolean algebra.</p> <p>They are,</p> <p>1) The complement of a product is equal to the sum of the complements. $(AB)' = A' + B'$</p> <p>2) The complement of a sum term is equal to the product of the complements. $(A + B)' = A'B'$</p>
2.	<p>Why NAND and NOR gates are called Universal gates?(BTL - 1)</p> <p>NAND and NOR are the gates that can be used alone to generate remaining gates such as NOT, AND and OR. Thus, with only any of the two gates, we can implement the logic circuit. Hence, they are called universal gates.</p>
3.	<p>What are called don't care conditions?(MAY/JUNE 2013)(BTL1)</p> <p>In some logic circuits certain input conditions never occur, therefore the Corresponding output never appears. In such cases the output level is not defined, it can be either high or low. These output levels are indicated by 'X' or 'd' in the truth tables and are called don't care conditions or incompletely specified functions.</p>
4.	<p>Apply De-Morgan's theorem to $[(A+B)+C]'$.[May/June-2014] (BTL 3)</p> <p>Given $[(A+B)+C]' = (A+B)' \cdot C' = (A' \cdot B') \cdot C'$ $[(A+B)+C]' = A'B'C'$</p>
5.	<p>Convert 0.35 to equivalent hexadecimal number. [May/June-2014] (BTL 3)</p> <p>Given $(0.35)_{10} = 0.35 \times 16 = 5.60 = 0.60 \times 16 = 9.60$ $= 0.60 \times 16 = 9.60$ $(0.35)_{10} = (0.599)_{16}$</p>
6.	<p>Convert $Y = A + BC' + AB + A'BC$ into canonical form. [April/May-2015](BTL 3)</p> <p>Given</p> <p>$Y = A + BC' + AB + A'BC$ $Y = A(B+B')(C+C') + (A+A')BC' + AB(C+C') + A'BC$ $Y = ABC + ABC' + AB'C + AB'C' + ABC' + A'BC' + ABC + ABC' + A'BC$ $Y = ABC + ABC' + AB'C + AB'C' + A'BC' + A'BC$</p>
7.	<p>Name the two canonical forms for Boolean Algebra.(BTL - 1)</p> <p>Standard SOP and Standard POS forms</p>
8.	<p>Define 'min term' and 'max term'. [April/May-2015](BTL 1)</p> <p>A product term containing all the variables of the function in either complemented or uncomplemented form is called a min term.</p> <p>A sum term containing all the variables of the function in either complemented or uncomplemented form is called a max term.</p>
9.	<p>State the Associative Law of Boolean Algebra.(BTL - 1)</p> <p><u>Law 1 (The Associative Law of Addition)</u></p> <p>In the ORing of the several variables, the result is the same regardless of the grouping of the variables. For three variables, A ORed with B OR C is the same as A OR B ORed with C.</p> <p>i.e., $A + (B + C) = (A + B) + C$</p> <p><u>Law 2 (The Associative Law of Multiplication)</u></p> <p>It makes no difference in what order the variables are grouped when ANDing several variables. For three variables, A AND B ANDed with C is the same as A ANDed with B and C</p> <p>i.e., $(AB)C = A(BC)$</p>

10.	<p>Prove that the logical sum of all min terms of a Boolean function of 2 variables is 1. [Nov/Dec-2009] Consider two variables as A and B. For two variables A and B minterms are: $A'B', A'B, AB', AB$. The logical sum of these minterms are given by (BTL 1) $F = A'B' + A'B + AB' + AB$ $= A'(B'+B) + A(B'+B)(B'+B=1)$ $= A'(1) + A(1)(A'+A=1)$ $F = 1$ Hence it is to be proved.</p>																																																												
11.	<p>Show that a positive logic NAND gate is a negative logic NOR gate. [Nov/Dec- 2009] (BTL 1) Truth table of NAND gate</p> <table border="1" data-bbox="235 535 539 718"> <thead> <tr> <th>A</th> <th>B</th> <th>Y</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>1</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> </tr> <tr> <td>1</td> <td>0</td> <td>1</td> </tr> <tr> <td>1</td> <td>1</td> <td>0</td> </tr> </tbody> </table> <p>Truth table of positive logic NAND gate</p> <table border="1" data-bbox="235 751 539 976"> <thead> <tr> <th>A</th> <th>B</th> <th>Y</th> </tr> </thead> <tbody> <tr> <td>LOW</td> <td>LOW</td> <td>LOW</td> </tr> <tr> <td>LOW</td> <td>HIGH</td> <td>LOW</td> </tr> <tr> <td>HIGH</td> <td>LOW</td> <td>LOW</td> </tr> <tr> <td>HIGH</td> <td>HIGH</td> <td>HIGH</td> </tr> </tbody> </table> <p>TRUTH TABLE OF NOR GATE</p> <table border="1" data-bbox="235 1010 539 1234"> <thead> <tr> <th>A</th> <th>B</th> <th>Y</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> </tr> <tr> <td>1</td> <td>1</td> <td>1</td> </tr> </tbody> </table> <p>Truth table for positive logic NOR gate</p> <table border="1" data-bbox="235 1268 539 1486"> <thead> <tr> <th>A</th> <th>B</th> <th>Y</th> </tr> </thead> <tbody> <tr> <td>LOW</td> <td>LOW</td> <td>HIGH</td> </tr> <tr> <td>LOW</td> <td>HIGH</td> <td>HIGH</td> </tr> <tr> <td>HIGH</td> <td>LOW</td> <td>HIGH</td> </tr> <tr> <td>HIGH</td> <td>HIGH</td> <td>LOW</td> </tr> </tbody> </table>	A	B	Y	0	0	1	0	1	1	1	0	1	1	1	0	A	B	Y	LOW	LOW	LOW	LOW	HIGH	LOW	HIGH	LOW	LOW	HIGH	HIGH	HIGH	A	B	Y	0	0	0	0	1	0	1	0	0	1	1	1	A	B	Y	LOW	LOW	HIGH	LOW	HIGH	HIGH	HIGH	LOW	HIGH	HIGH	HIGH	LOW
A	B	Y																																																											
0	0	1																																																											
0	1	1																																																											
1	0	1																																																											
1	1	0																																																											
A	B	Y																																																											
LOW	LOW	LOW																																																											
LOW	HIGH	LOW																																																											
HIGH	LOW	LOW																																																											
HIGH	HIGH	HIGH																																																											
A	B	Y																																																											
0	0	0																																																											
0	1	0																																																											
1	0	0																																																											
1	1	1																																																											
A	B	Y																																																											
LOW	LOW	HIGH																																																											
LOW	HIGH	HIGH																																																											
HIGH	LOW	HIGH																																																											
HIGH	HIGH	LOW																																																											
12.	<p>What is the significance of high impedance state in tri-state gates? [Nov/Dec- 2010](BTL 1) High impedance state of a three-state gate provides a special feature not available in other gates. Because of this features a larger number of three state gate output can be connected with wires to form a common line without endangering loading effects.</p>																																																												
13.	<p>Simplify the following Boolean Expression to a minimum number of literals.(BTL 3) $(BC'+A'D)(AB'+CD')$[Nov/Dec-2011] $F = (BC'+A'D)(AB'+CD')$ $= BC'AB'+BC'CD'+A'DAB'+A'DCD' (A.A'=0)$ $= AB'B'C'+BCC'D'+AA'B'D+A'CDD'$ $F = 0$</p>																																																												
14.	<p>Explain the De Morgan's theorem in Boolean Algebra.(BTL - 1)</p>																																																												

	Its states that the complement of a product is equal to the sum of the complements. $A'B' = A' + B'$
15.	Simplify the given Boolean Expression $F = x' + xy + xz' + xy'z'$. [Nov/Dec-2012] (BTL3) $F = x' + xy + xz' + xy'z'$ $= x' + x(y + z' + y'z')$ ($A + A'B = A + B$) $= x' + y + z' + y'z'$ $= x' + y + z'(1 + y')$ ($1 + A' = 1$) $F = x' + y + z'$
16.	Implement the given function using NAND gates $F(x,y,z) = \Sigma m(0,6)$. [Nov/Dec- 2012] (BTL 3) $F(x,y,z) = x'y'z' + xyz'$
17.	State Distributive Law. [Nov/Dec-2013] (BTL 1) Distributive law of dot(.) over plus(+) is given by $a.(b+c) = a.b + a.c$ Distributive law of plus(+) over dot(.) is given by $a+b.c = (a+b).(a+c)$
18.	What is a Logic gate? (BTL 1) Logic gates are the basic elements that make up a digital system. The electronic gate is a circuit that is able to operate on a number of binary inputs in order to perform a particular logical function.
19.	What are the basic digital logic gates? (BTL 1) The three basic logic gates are AND gate OR gate NOT gate
20.	Which gates are called as the universal gates? What are its advantages? (BTL 1) The NAND and NOR gates are called as the universal gates. These gates are used to perform any type of logic application.
21.	What is a karnaugh map? State the limitations of karnaugh map. (BTL 1) A karnaugh map or k map is a pictorial form of truth table, in which the map diagram is made up of squares, with each squares representing one minterm of the function. LIMITATION: i) Generally it is limited to six variable map (i.e) more then six variable involving expression are not reduced. ii) The map method is restricted in its capability since they are useful for simplifying only Boolean expression represented in standard form.
22.	What are the methods adopted to reduce Boolean function? (BTL1) i) Karnaugh map ii) Tabular method or Quine Mc-Cluskey method iii) Variable entered map technique.
23.	Prove that $ABC + ABC' + AB'C + A'BC = AB + AC + BC$ (BTL 3) $ABC + ABC' + AB'C + A'BC = AB(C + C') + AB'C + A'BC$ $= AB + AB'C + A'BC$ $= A(B + B'C) + A'BC$ $= A(B + C) + A'BC$ $= AB + AC + A'BC$ $= B(A + C) + AC$ $= AB + BC + AC$ $= AB + AC + BC \dots \text{Proved}$
24.	Explain the principle of duality with the help of example. (BTL - 1) The duality theorem states that, starting with a Boolean relation, you can derive another Boolean relation by, Changing each OR sign to an AND sign Changing each AND sign to an OR sign Complementing any 0 to 1 appearing in the expression Ex: $A+0 = A$. Using duality theorem, we can say that, $A.1 = A$

25.	<p>What code is used to label the row headings and column heading of K – map and why? (BTL - 1) Gray Code is used to label the rows and columns of K – Map In case of Gray code, only one variable changes between two consecutive numbers. This is useful in grouping pair, quad, or octets in K – Maps and thus eliminating variables in the final expression. Hence gray code is used to label the rows and columns of K – Map.</p>																																																																							
PART*B																																																																								
1	<p>Simplify the function F using Quine Mccluskey method and verify the result using KMap $F(ABCD)=\Sigma(1,2,3,5,7,9,10,11,13,15)$ Mod- MAY 2016, 2015, 2014 (13M) (BTL1) Answer Page No:2.65 in D.Edwin Dhas STEP 1:List the minterm in binary form (2M)</p> <table border="1" data-bbox="235 556 657 903"> <thead> <tr> <th>Minterm</th> <th>Binary number</th> </tr> </thead> <tbody> <tr><td>1</td><td>0001</td></tr> <tr><td>2</td><td>0010</td></tr> <tr><td>3</td><td>0011</td></tr> <tr><td>5</td><td>0101</td></tr> <tr><td>7</td><td>0111</td></tr> <tr><td>9</td><td>1001</td></tr> <tr><td>10</td><td>1010</td></tr> <tr><td>11</td><td>1011</td></tr> <tr><td>13</td><td>1101</td></tr> <tr><td>15</td><td>1111</td></tr> </tbody> </table> <p>Step 2: Group the minterms according to number of 1's (3M)</p> <table border="1" data-bbox="235 934 885 1333"> <thead> <tr> <th>No of 1's</th> <th>Minterm</th> <th>Binary Number</th> </tr> </thead> <tbody> <tr> <td rowspan="2">1</td> <td>1</td> <td>0001</td> </tr> <tr> <td>2</td> <td>0010</td> </tr> <tr> <td rowspan="3">2</td> <td>3</td> <td>0011</td> </tr> <tr> <td>5</td> <td>0101</td> </tr> <tr> <td>9</td> <td>1001</td> </tr> <tr> <td rowspan="4">3</td> <td>10</td> <td>1010</td> </tr> <tr> <td>7</td> <td>0111</td> </tr> <tr> <td>11</td> <td>1011</td> </tr> <tr> <td>13</td> <td>1101</td> </tr> <tr> <td>4</td> <td>15</td> <td>1111</td> </tr> </tbody> </table> <p>Step 3: Compare each binary number in each group with every term in the adjacent higher group for they differ only by one position. Repeat this step for various cell combinations (4M) 2 cell combination</p> <table border="1" data-bbox="235 1417 1063 1839"> <thead> <tr> <th>Minterms</th> <th>Binary number</th> </tr> </thead> <tbody> <tr><td>1,3</td><td>00_1</td></tr> <tr><td>1,5</td><td>0_01</td></tr> <tr><td>1,9</td><td>_001</td></tr> <tr><td>2,3</td><td>001_</td></tr> <tr><td>2,10</td><td>_010</td></tr> <tr><td>3,7</td><td>0_11</td></tr> <tr><td>3,11</td><td>_011</td></tr> <tr><td>5,7</td><td>01_1</td></tr> <tr><td>5,13</td><td>_101</td></tr> <tr><td>9,11</td><td>10_1</td></tr> </tbody> </table>	Minterm	Binary number	1	0001	2	0010	3	0011	5	0101	7	0111	9	1001	10	1010	11	1011	13	1101	15	1111	No of 1's	Minterm	Binary Number	1	1	0001	2	0010	2	3	0011	5	0101	9	1001	3	10	1010	7	0111	11	1011	13	1101	4	15	1111	Minterms	Binary number	1,3	00_1	1,5	0_01	1,9	_001	2,3	001_	2,10	_010	3,7	0_11	3,11	_011	5,7	01_1	5,13	_101	9,11	10_1
Minterm	Binary number																																																																							
1	0001																																																																							
2	0010																																																																							
3	0011																																																																							
5	0101																																																																							
7	0111																																																																							
9	1001																																																																							
10	1010																																																																							
11	1011																																																																							
13	1101																																																																							
15	1111																																																																							
No of 1's	Minterm	Binary Number																																																																						
1	1	0001																																																																						
	2	0010																																																																						
2	3	0011																																																																						
	5	0101																																																																						
	9	1001																																																																						
3	10	1010																																																																						
	7	0111																																																																						
	11	1011																																																																						
	13	1101																																																																						
4	15	1111																																																																						
Minterms	Binary number																																																																							
1,3	00_1																																																																							
1,5	0_01																																																																							
1,9	_001																																																																							
2,3	001_																																																																							
2,10	_010																																																																							
3,7	0_11																																																																							
3,11	_011																																																																							
5,7	01_1																																																																							
5,13	_101																																																																							
9,11	10_1																																																																							

	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr><td>9,13</td><td>1_01</td></tr> <tr><td>10,11</td><td>101_</td></tr> <tr><td>7,15</td><td>_111</td></tr> <tr><td>11,15</td><td>1_11</td></tr> <tr><td>13,15</td><td>11_1</td></tr> </table> <p>4cell combination</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr><td>Minterms</td><td>Binary number</td></tr> <tr><td>1,3,5,7</td><td>0__1</td></tr> <tr><td>1,3,9,11</td><td>_0_1</td></tr> <tr><td>1,9,5,13</td><td>--_01</td></tr> <tr><td>2,3,10,11</td><td>_01_</td></tr> <tr><td>3,11,7,15</td><td>--_11</td></tr> <tr><td>5,7,13,15</td><td>_1_1</td></tr> <tr><td>9,11,13,15</td><td>1__1</td></tr> </table> <p>8cell combination</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr><td>Minterms</td><td>Binary number</td></tr> <tr><td>1,3,5,7,9,11,13,15</td><td>___1</td></tr> </table>	9,13	1_01	10,11	101_	7,15	_111	11,15	1_11	13,15	11_1	Minterms	Binary number	1,3,5,7	0__1	1,3,9,11	_0_1	1,9,5,13	--_01	2,3,10,11	_01_	3,11,7,15	--_11	5,7,13,15	_1_1	9,11,13,15	1__1	Minterms	Binary number	1,3,5,7,9,11,13,15	___1															
9,13	1_01																																													
10,11	101_																																													
7,15	_111																																													
11,15	1_11																																													
13,15	11_1																																													
Minterms	Binary number																																													
1,3,5,7	0__1																																													
1,3,9,11	_0_1																																													
1,9,5,13	--_01																																													
2,3,10,11	_01_																																													
3,11,7,15	--_11																																													
5,7,13,15	_1_1																																													
9,11,13,15	1__1																																													
Minterms	Binary number																																													
1,3,5,7,9,11,13,15	___1																																													
	<p>Step 4: Form the prime implication table and find the Boolean expression (2M)</p> <table border="1" style="width: 100%; border-collapse: collapse; text-align: center;"> <tr> <th></th> <th>1</th> <th>2</th> <th>3</th> <th>5</th> <th>7</th> <th>9</th> <th>10</th> <th>11</th> <th>13</th> <th>15</th> </tr> <tr> <th>1,3,5,7,9,11,13,15</th> <td>*</td> <td></td> <td>*</td> <td>*</td> <td>*</td> <td>*</td> <td></td> <td>*</td> <td>*</td> <td>*</td> </tr> <tr> <th>2,3,10,11</th> <td></td> <td>*</td> <td>*</td> <td></td> <td></td> <td></td> <td>*</td> <td>*</td> <td></td> <td></td> </tr> <tr> <td></td> <td>✓</td> <td>✓</td> <td></td> <td>✓</td> <td>✓</td> <td>✓</td> <td>✓</td> <td></td> <td>✓</td> <td>✓</td> </tr> </table>		1	2	3	5	7	9	10	11	13	15	1,3,5,7,9,11,13,15	*		*	*	*	*		*	*	*	2,3,10,11		*	*				*	*				✓	✓		✓	✓	✓	✓		✓	✓	
	1	2	3	5	7	9	10	11	13	15																																				
1,3,5,7,9,11,13,15	*		*	*	*	*		*	*	*																																				
2,3,10,11		*	*				*	*																																						
	✓	✓		✓	✓	✓	✓		✓	✓																																				
	<p>$F=D+BC$</p> <p>Step 5: Draw the K-Map and verify the Boolean expression (2M)</p> <table border="1" style="width: 100%; border-collapse: collapse; text-align: center;"> <tr> <td style="border: none;"></td> <td style="border: none;">$\overline{C}\overline{D}$</td> <td style="border: none;">$\overline{C}D$</td> <td style="border: none;">CD</td> <td style="border: none;">$C\overline{D}$</td> </tr> <tr> <td style="border: none;">$\overline{A}\overline{B}$</td> <td></td> <td>1</td> <td>1</td> <td>1</td> </tr> <tr> <td style="border: none;">$\overline{A}B$</td> <td></td> <td>1</td> <td>1</td> <td></td> </tr> <tr> <td style="border: none;">AB</td> <td></td> <td>1</td> <td>1</td> <td></td> </tr> <tr> <td style="border: none;">$A\overline{B}$</td> <td></td> <td>1</td> <td>1</td> <td>1</td> </tr> </table> <p>$F=D+BC$</p>		$\overline{C}\overline{D}$	$\overline{C}D$	CD	$C\overline{D}$	$\overline{A}\overline{B}$		1	1	1	$\overline{A}B$		1	1		AB		1	1		$A\overline{B}$		1	1	1																				
	$\overline{C}\overline{D}$	$\overline{C}D$	CD	$C\overline{D}$																																										
$\overline{A}\overline{B}$		1	1	1																																										
$\overline{A}B$		1	1																																											
AB		1	1																																											
$A\overline{B}$		1	1	1																																										
2	<p>Simplify the function F using Tabulation method, Model- NOV/DEC 2015</p> <p>$f(A,B,C,D)=\sum m(1,3,5,8,9,11,15)+d(2,13)$ (13M) (BTL 3)</p> <p>Answer Page No:2.60(MODEL) in D.Edwin Dhas</p> <p>step1</p> <p style="text-align: center;">Grouping of minterms/don't care terms according to number of 1's.</p>	(3M)																																												

Group	Minterm/ don't care term	Variables				Check for inclusion in group of 2
		A	B	C	D	
1	1	0	0	0	1	✓
	2*	0	0	1	0	✓
	8	1	0	0	0	✓
2	3	0	0	1	1	✓
	5	0	1	0	1	✓
	9	1	0	0	1	✓
3	11	1	0	1	1	✓
	13*	1	1	0	1	✓
4	15	1	1	1	1	✓

Step 2

Grouping of 2 minterms/don't care terms

(3M)

Group	Minterms/ don't care terms	Variables				Check for inclusion in group of 4
		A	B	C	D	
1	1, 3	0	0	—	1	✓
	1, 5	0	—	0	1	✓
	1, 9	—	0	0	1	✓
	2*, 3	0	0	1	—	✓
	8, 9	1	0	0	—	✓
	3, 11	—	0	1	1	✓
2	5, 13*	—	1	0	1	✓
	9, 11	1	0	—	1	✓
3	9, 13*	1	—	0	1	✓
	11, 15	1	—	1	1	✓
	13, 15	1	1	—	1	✓

Step 3

Grouping of 4 minterms/don't care terms

(3M)

Group	Minterms/ don't care terms	Variables			
		A	B	C	D
1	1, 3, 9, 11	—	0	—	1
	1, 5, 9, 13*	—	—	0	1
	1, 9, 3, 11	—	0	—	1
	1, 9, 5, 13*	—	—	0	1
2	9, 11, 13*, 15	1	—	—	1
	9, 13*, 11, 15	1	—	—	1

Step 4

Prime Implication Table and Boolean Expression

(4M)

PI terms	Decimal numbers	Minterms/don't care terms								
		1	2*	3	5	8	9	11	13*	15
$\overline{B}D$	1, 3, 9, 11	x		x			x	x		
$\overline{C}D$	1, 5, 9, 13* ✓	x			⊗		x		x	
AD	9, 11, 13*, 15 ✓						x	x	x	⊗
$\overline{A}BC$	2*, 3		x	x						
ABC	8, 9	✓				⊗	x			
					✓		✓			✓

$f(A, B, C, D) = \overline{B}D + \overline{C}D + AD + \overline{A}BC$

3. Simplify the function in SOP and POS using K-Map $f = \sum m(0,2,3,6,7) + d(8,10,11,15)$ (13M) (BTL3)
 Answer Page No:2.50(MODEL) in D.Edwin Dhas

Solution:

(i) Sum of Products (SOP)

(4M)

		CD			
		$\overline{C}\overline{D}$	$\overline{C}D$	CD	$C\overline{D}$
AB	$\overline{A}\overline{B}$	1		1	1
	$\overline{A}B$			1	1
	AB			x	
	$A\overline{B}$	x		x	x

$F = A'C + BD'$

(3M)

Product of Sum (POS)

(3M)

		$\overline{C}\overline{D}$			
		$\overline{C}\overline{D}$	$\overline{C}D$	CD	$C\overline{D}$
AB	$\overline{A}\overline{B}$		0		
	$\overline{A}B$	0	0		
	AB	0	0	x	0
	$A\overline{B}$	x	0	x	x

$F = A + BC + C'D$

(3M)

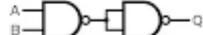
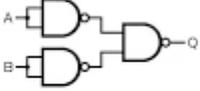
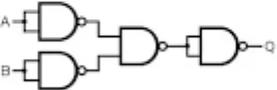
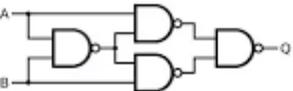
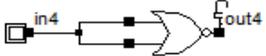
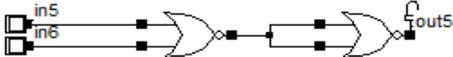
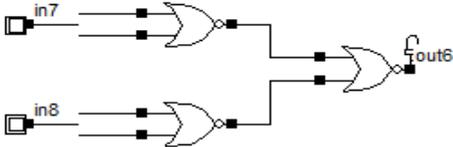
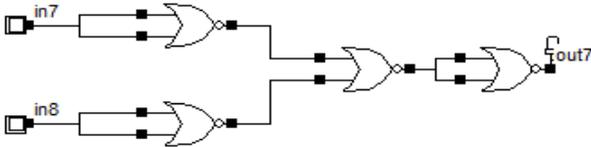
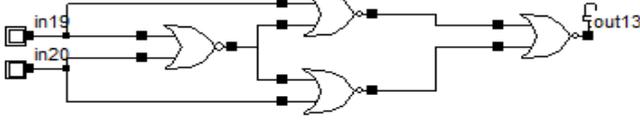
4

Implement basic logic gates using UNIVERSAL gates. NOV 2015, MAY 2015 (13M) (BTL 3)

Answer Page No:2.92 in D.Edwin Dhas

Implementation using NAND gate:

(7M)

	<p>NOT </p> <p>AND </p> <p>OR </p> <p>NOR </p> <p>XOR </p> <p>Derived Gates using NOR Gate</p> <p>NOT </p> <p>OR </p> <p>AND </p> <p>NAND </p> <p>EXNOR </p>
5	<p>Design a 4 bit BCD to EXCESS 3 code converter. Draw the logic diagram.(13M) (BTL 6) Answer Page No:2.81 in D.Edwin Dhas</p>

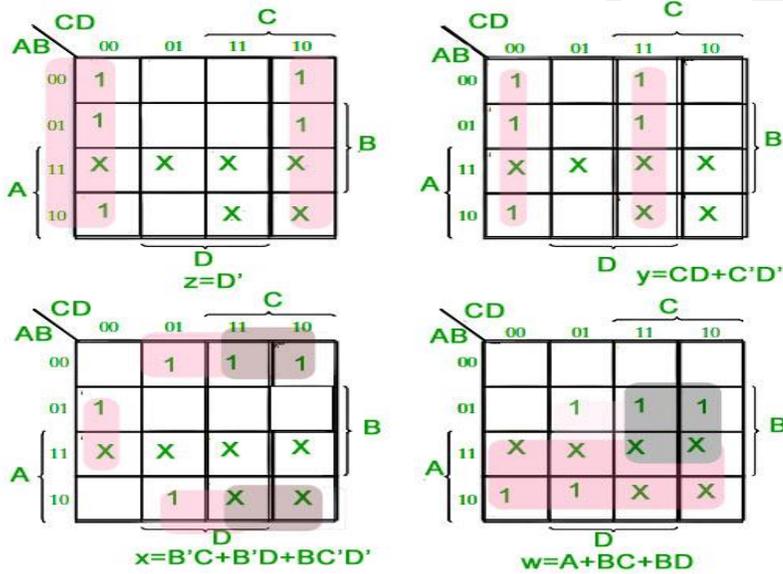


(8M)

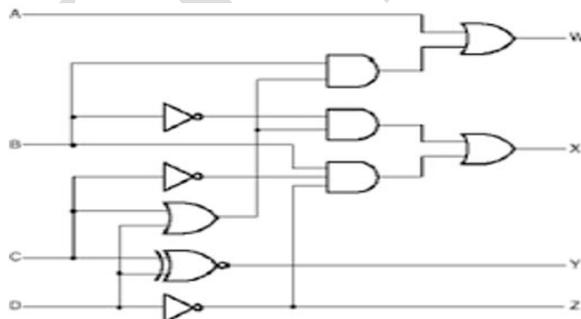
BCD(8421)				Excess-3			
A	B	C	D	w	x	y	z
0	0	0	0	0	0	1	1
0	0	0	1	0	1	0	0
0	0	1	0	0	1	0	1
0	0	1	1	0	1	1	0
0	1	0	0	0	1	1	1
0	1	0	1	1	0	0	0
0	1	1	0	1	0	0	1
0	1	1	1	1	0	1	0
1	0	0	0	1	0	1	1
1	0	0	1	1	1	0	0
1	0	1	0	X	X	X	X
1	0	1	1	X	X	X	X
1	1	0	0	X	X	X	X
1	1	0	1	X	X	X	X
1	1	1	0	X	X	X	X
1	1	1	1	X	X	X	X

06

(5M)



(5M)

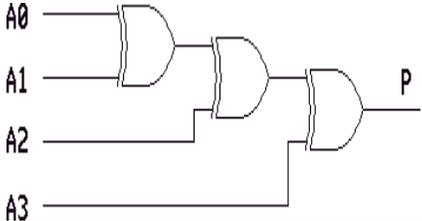
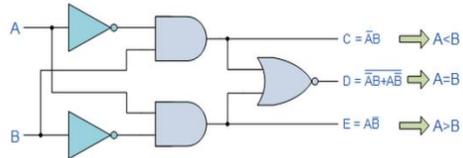


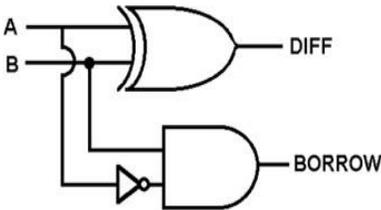
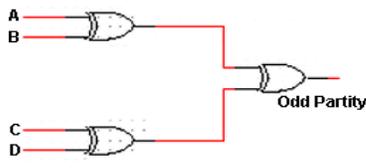
(3M)

6

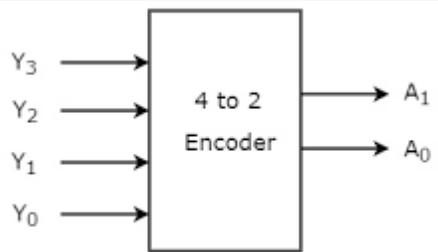
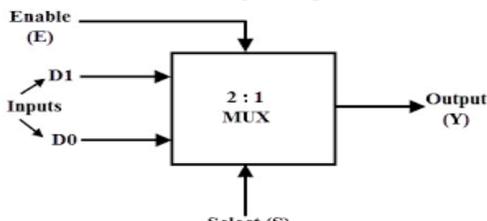
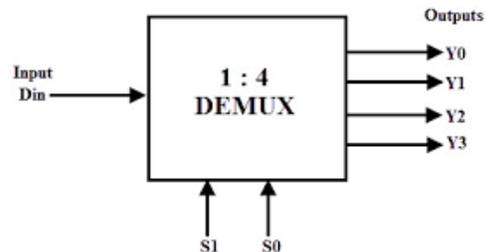
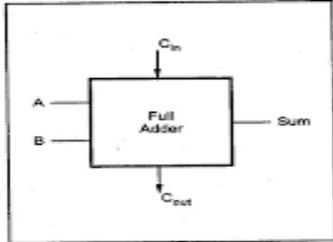
(i) Illustrate the MSOP representation for $F(A,B,C,D,E) = m(1,4,6,10,20,22,24,26) + d(0,11,16,27)$ using K-map method. Draw the circuit of the minimal expression using only NAND gates. (7)
 (ii) Write about Excess 3 and Gray Code with an example. (8M) (BTL 1)
 Answer Page No:3.74 in D.Edwin Dhas

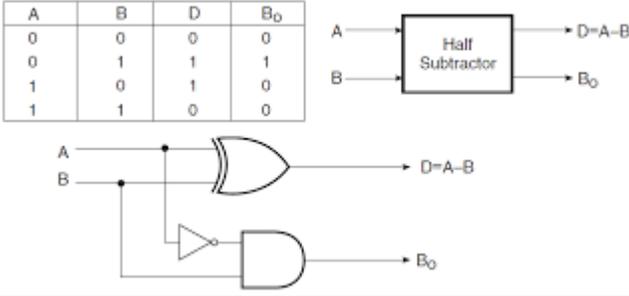
	K-MAP (3M) Logic diagram (4M)
7	Simplify the following Boolean expression $F = x''y''z'' + x''yz + xy''z'' + xyz''$. (13m) (BTL - 3) Answer Page No:2.29 in D.Edwin Dhas Key Points: Group the 1's cells (6m) Identify the Boolean Expression (7m)
8	Simplify using K-map to obtain a minimum POS expression. (7m) (BTL - 3) $(A''+B''+C+D)(A+B''+C+D)(A+B+C+D'')(A+B+C''+D'')$ (A''+B+C''+D'')(A+B+C''+D) Answer Page No:2.39 in D.Edwin Dhas Key Points: Group the 0's cells (3m) Identify the Boolean Expression (4m) State and Prove Demorgan's theorem. (8m) (BTL - 1) Answer Page No:2.4 in D.Edwin Dhas Key Points: Theorem (2m) Truth Table (2m) Proof - (4m)
9	Find a Min SOP and Min POS for $f = b''c''d + bcd + acd'' + a''b''c + a''bc''d$ (13m) (BTL - 3) Answer Page No:2.32 in D.Edwin Dhas Key Points: Group the 1's cells - (6m) Identify the Boolean Expression - (7m)
	PART*C
1	Simplify the Boolean function $F(A,B,C,D) = \Sigma m(1,3,7,11,15) + \Sigma d(0,2,5)$. if don't care conditions are not taken care, What is the simplified Boolean function .What are your comments on it? Implement both circuits. (15m) (BTL - 3) Answer Page No:2.50 in D.Edwin Dhas Key Points: Group the 0's cells - (8m) Identify the Boolean Expression. - (7m)
2	i). Implement $Y = (A+C) (A+D'') (A+B+C'')$ using NOR gates only (15m) (BTL - 3) ii) Find a network of AND and OR gate to realize $f(a,b,c,d) = \Sigma m(1,5,6,10,13,14)$ Answer Page No:2.102 in D.Edwin Dhas Key Points: Group the 1's cells - (4m) Identify the Boolean Expression - (4m) Logic Diagram - (5m)
3	Simplify the following Boolean function using Tabulation method. (15m) (BTL - 3) $F(w,x,y,z) = \Sigma(2,3,10,11,12,13,14,15)$. Answer Page No:2.76 in D.Edwin Dhas List the minterms in binary form - (2m) Arrange the minterms according to categories of 1's - (2m) Compare each binary number with every term in the next higher category - (3m) List the prime implicants - (3m) Select the minimum number of prime implicants which must cover all minterms - (3m)

UNIT II - COMBINATIONAL CIRCUIT DESIGN																										
Design of Half and Full Adders, Half and Full Subtractors, Binary Parallel Adder – Carry look ahead Adder, BCD Adder, Multiplexer, Demultiplexer, Magnitude Comparator, Decoder, Encoder, Priority Encoder.																										
PART * A																										
1	Write an expression for borrow and difference in a full subtractor circuit. [April/May-2010] (BTL 1) Difference= $A'B+AB'$, Borrow= $A'B$																									
2	Draw the circuits diagram for 4-bit odd parity generator.[April/May-2010] (BTL 6) 																									
3	Design a single bit magnitude comparator to compare two words A and B. (BTL 6) <table border="1" style="margin-left: 20px;"> <thead> <tr> <th>A</th> <th>B</th> <th>A<B</th> <th>A=B</th> <th>A>B</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> <td>1</td> <td>0</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> <td>0</td> <td>0</td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> <td>0</td> <td>1</td> </tr> <tr> <td>1</td> <td>1</td> <td>0</td> <td>1</td> <td>0</td> </tr> </tbody> </table> <p style="margin-left: 20px;"> $A>B = AB^1$ $A<B = A^1B$ $A=B = A^1B^1 + AB$ </p> 	A	B	A<B	A=B	A>B	0	0	0	1	0	0	1	1	0	0	1	0	0	0	1	1	1	0	1	0
A	B	A<B	A=B	A>B																						
0	0	0	1	0																						
0	1	1	0	0																						
1	0	0	0	1																						
1	1	0	1	0																						
4	What is an encoder?[May/June-2012] (BTL 1) An encoder has 2^n input lines and n output lines. In encoder the output lines generate the binary code corresponding to the input value.																									
5	List few applications of multiplexer.[May/June-2012, Nov/Dec-2013] (BTL 1) Data Selector. Implement combinational logic circuit. Time multiplexing systems Frequency multiplexing systems. D/A and A/D converter Data acquisition systems.																									

6	<p>Design a half subtractor using basic gates.[May/June-2013, Nov/Dec-2010] (BTL 6)</p>  <p>Difference=$A'B+AB'=A\oplus B$ Borrow=$A'B$</p>												
7	<p>What is priority Encoder?[May/June-2014] (BTL 1) A priority encoder is an encoder circuit that includes the priority function. In priority encoder, if 2 or more inputs are equal to 1 at the same time, the input having the highest priority will take precedence.</p>												
8	<p>Write down the difference between demultiplexer and decoder.[April/May-2015] (BTL 4)</p> <table border="1" data-bbox="251 661 1299 1039"> <thead> <tr> <th></th> <th>Demultiplexer</th> <th>Decoder</th> </tr> </thead> <tbody> <tr> <td>Definition</td> <td>1 data input 2^n outputs</td> <td>It has n inputs 2^n outputs It has n control inputs</td> </tr> <tr> <td>Characteristic</td> <td>Connects the data input to the data output</td> <td>Selects one of the 2^n outputs by decoding the binary value on the basis of n inputs</td> </tr> <tr> <td>Reverse of</td> <td>Multiplexer</td> <td>Encoder</td> </tr> </tbody> </table>		Demultiplexer	Decoder	Definition	1 data input 2^n outputs	It has n inputs 2^n outputs It has n control inputs	Characteristic	Connects the data input to the data output	Selects one of the 2^n outputs by decoding the binary value on the basis of n inputs	Reverse of	Multiplexer	Encoder
	Demultiplexer	Decoder											
Definition	1 data input 2^n outputs	It has n inputs 2^n outputs It has n control inputs											
Characteristic	Connects the data input to the data output	Selects one of the 2^n outputs by decoding the binary value on the basis of n inputs											
Reverse of	Multiplexer	Encoder											
9	<p>Give examples for combinational circuit.[April/May-2015, Nov/Dec-2013] (BTL 1) Adders Subtractors Multiplexers Demultiplexers Encoders</p>												
10	<p>Give the logic expression for sum and carry in full adder circuit.[April/May- 2015] (BTL 1) $Sum = (A \oplus B) \oplus C_{in}$ $Carry = AB + BC_{in} + A C_{in}$</p>												
11	<p>Decoders Suggest a solution to overcome the limitation on the speed of an adder.[Nov/Dec- 2009] (BTL 1) It is possible to increase speed of adder by eliminating inter-stage carry delay. This method utilizes logic gates to look at the lower-order bits of the augend and addend to see if a higher-order carry is to be generated.</p>												
12	<p>Design of three bit parity generator.[Nov/Dec-2012] (BTL 6) Odd parity generator</p> 												
13	<p>Construct a two-4-bit parallel adder/subtractor using Full Adders and XOR gates. [Nov/Dec-2014] (BTL 6)</p>												

<p>14</p>	<p>Define combinational logic(BTL 1)</p> <p>Output = $f(\text{input})$</p> <p>When logic gates are connected together to produce a specified output for certain specified combinations of input variables, with no storage involved, the resulting circuit is called combinational logic.</p>																				
<p>15</p>	<p>Explain the design procedure for combinational circuits (BTL 1)</p> <p>The problem definition determine the number of available input variables & required O/P variables. Assigning letter symbols to I/O variables Obtain simplified Boolean expression for each O/P. Obtain the logic diagram.</p>																				
<p>16</p>	<p>Define Half adder (BTL 1)</p> <table border="1" data-bbox="701 1094 976 1247"> <thead> <tr> <th>A</th> <th>B</th> <th>Sum</th> <th>Carry</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> <td>0</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> <td>0</td> </tr> <tr> <td>1</td> <td>0</td> <td>1</td> <td>0</td> </tr> <tr> <td>1</td> <td>1</td> <td>0</td> <td>1</td> </tr> </tbody> </table> <p>The logic circuit that performs the addition of two bits is a half adder.</p>	A	B	Sum	Carry	0	0	0	0	0	1	1	0	1	0	1	0	1	1	0	1
A	B	Sum	Carry																		
0	0	0	0																		
0	1	1	0																		
1	0	1	0																		
1	1	0	1																		
<p>17</p>	<p>Define Decoder?(BTL1)</p> <p>A decoder is a multiple - input multiple output logic circuit that converts coded inputs into coded outputs where the input and output codes are different.</p>																				
<p>18</p>	<p>What is binary decoder? (BTL 1)</p> <p>A decoder is a combinational circuit that converts binary information from n Input lines to a maximum of 2^n outputs lines.</p>																				
<p>19</p>	<p>Define Encoder?(BTL 1)</p> <p>An encoder has 2^n input lines and n output lines. In encoder the output lines Generate the binary code corresponding to the input value.</p>																				

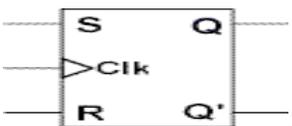
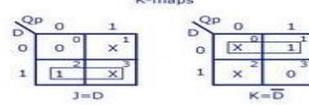
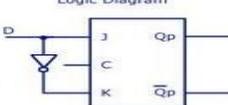
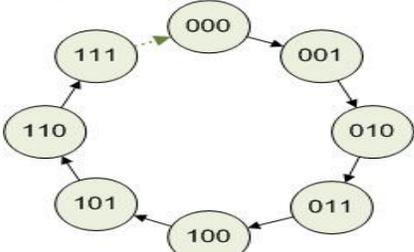
																																																			
20	<p>What is priority Encoder?(BTL1) A priority encoder is an encoder circuit that includes the priority function. In Priority encoder, if 2 or more inputs are equal to 1 at the same time, the input having the highest priority will take precedence.</p>																																																		
21	<p>Define multiplexer?(BTL 1) Multiplexer is a digital switch. It allows digital information from several sources to be routed onto a single output line.</p> 																																																		
22	<p>What do you mean by comparator?(BTL1) A comparator is a special combinational circuit designed primarily to compare the relative magnitude of two binary numbers.</p>																																																		
23	<p>Define demux(BTL1)</p>  <p>A demultiplexer (or demux) is a device that takes a single input line and routes it to one of several digital output lines. A demultiplexer of 2^n outputs has n select lines, which are used to select which output line to send the input</p>																																																		
24	<p>Define full adder(BTL1) The circuit that performs the addition of three bits is a full adder.</p> <table border="1" data-bbox="251 1459 665 1722"> <thead> <tr> <th colspan="3">Inputs</th> <th colspan="2">Outputs</th> </tr> <tr> <th>A</th> <th>B</th> <th>C_{in}</th> <th>Carry</th> <th>Sum</th> </tr> </thead> <tbody> <tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr> <tr><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td></tr> <tr><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td></tr> <tr><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td></tr> <tr><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td></tr> <tr><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td></tr> <tr><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td></tr> <tr><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td></tr> </tbody> </table> <p>Table 3.7 Truth table for full-adder</p>  <p>Fig. 3.14 Block schematic of full-adder</p>	Inputs			Outputs		A	B	C_{in}	Carry	Sum	0	0	0	0	0	0	0	1	0	1	0	1	0	0	1	0	1	1	1	0	1	0	0	0	1	1	0	1	1	0	1	1	0	1	0	1	1	1	1	1
Inputs			Outputs																																																
A	B	C_{in}	Carry	Sum																																															
0	0	0	0	0																																															
0	0	1	0	1																																															
0	1	0	0	1																																															
0	1	1	1	0																																															
1	0	0	0	1																																															
1	0	1	1	0																																															
1	1	0	1	0																																															
1	1	1	1	1																																															
25	<p>Define half subtractor(BTL1)</p>																																																		

	<p>Half subtractor is the most essential combinational logic circuit which is used in digital electronics. The subtractor circuit uses binary numbers (0,1) for the subtraction.</p> <table border="1" data-bbox="264 304 568 426"> <thead> <tr> <th>A</th> <th>B</th> <th>D</th> <th>B₀</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> <td>0</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> <td>1</td> </tr> <tr> <td>1</td> <td>0</td> <td>1</td> <td>0</td> </tr> <tr> <td>1</td> <td>1</td> <td>0</td> <td>0</td> </tr> </tbody> </table> 	A	B	D	B ₀	0	0	0	0	0	1	1	1	1	0	1	0	1	1	0	0
A	B	D	B ₀																		
0	0	0	0																		
0	1	1	1																		
1	0	1	0																		
1	1	0	0																		
PART * B																					
<p>1.</p>	<p>Consider the combinational circuit shown.(13M) (BTL - 3) Derive the Boolean expressions for T1 through T4. Evaluate the outputs F1 and F2 as a function of the four inputs. List the truth table with 16 binary combinations of the four input variables. Then list the binary values for T1 through T4 and outputs F1 and F2 in the table. Plot the Boolean function obtained in part (ii) on maps show that simplified Boolean expression are equivalent to the ones obtained in part (i) Answer Page No:3.3 in D.Edwin Dhas Key Points: Boolean expression derivation – (4m) Truth table – (4m) K – Map – (5m)</p>																				
<p>2.</p>	<p>Design half subtractor and full subtractor circuit and implement using NAND gates. (13m) (BTL - 4) (Nov – Dec 2015) Answer Page No: 3.13-3.15 in D.Edwin Dhas Key Points: Half Subtractor – (2m) Truth table for Half Subtractor – (1m) K – Map Simplification – (2m) Full Subtractor – (2m) Truth table for Full Subtractor –(2m) K – Map Simplification – (1m) Implementation using NAND gates. – (3m)</p>																				
<p>3.</p>	<p>Draw and explain the block diagram of 4 – bit parallel adder and subtractor. (13m)(BTL - 2) Answer Page No: 3.17-3.19 in D.Edwin Dhas Key Points: Block diagram of n – bit parallel adder – (7m) Block diagram of n – bit parallel subtractor – (6m)</p>																				
<p>4.</p>	<p>Draw and explain the block diagram of 4 – bit parallel adder/subtractor. (8m)(BTL - 2) Answer Page No: 3.19 in D.Edwin Dhas 4 – bit parallel adder with look ahead carry generator – (2m) Key Points: 4 – bit parallel adder/subtractor – (8m) Construct the 4 – bit adder with look ahead carry adder. (7m) (BTL - 5) (April – May 2015) Answer Page No: 3.20 - 3.22 in D.Edwin Dhas Key Points: Full adder circuit – (3m) Logic Diagram of look ahead carry generator – (2m)</p>																				

5.	<p>Design an 8 – bit BCD adder using 4 – bit binary adder. (8m) (BTL - 4) Answer Page No: 3.23-3.25 in D.Edwin Dhas Key Points: 8 – bit BCD adder using IC 7483</p> <p>With a suitable block diagram explain the operation of BCD adder.(7m) (BTL - 1) Answer Page No: 3.23-3.25 in D.Edwin Dhas Key Points: Truth Table K – Map simplification – (4m) Block Diagram of BCD adder – (3m)</p>
6.	<p>With neat diagram explain BCD subtractor using 9’s and 10’s complement method(8M). (BTL 6) Answer Page No: 3.23 in D.Edwin Dhas Key Points: subtractor using 9’s complement - 4 – bit BCD subtractor using 9’s complement method (4M) subtractor using 10’s complement 4 – bit BCD subtractor using 10’s complement method (4M)</p> <p>Design a multiple circuit to multiply the following binary number A = A0A1A2A3 and B=B0B1B2B3 using required number of binary parallel adders. (7M)(BTL - 4) Answer Page No: 3.25 - 3.26 in D.Edwin Dhas Key Points: Use two 4 – bit binary adders (7M)</p>
7	<p>With suitable block diagram explain binary multiplier. (13m) (BTL - 2) Answer Page No: 3.25-3.26 in D.Edwin Dhas Key Points: 2*2 Multiplier – 3m 4*4 Multiplier – 4m 4 – bit by 4 – bit binary multiplier – 6m</p>
8	<p>Draw the circuit for 3 to 8 decoder and explain. (8m) (BTL - 2) Answer Page No: 3.54 - 3.56 in D.Edwin Dhas Key Points: Truth Table – (4m) Logic Diagram – (4m)</p> <p>Implement the Boolean function $F = \sum m(1,2,3,7)$ using 3:8 decoder. (7m) (BTL - 2) Answer Page No: 3.54 - 3.56 in D.Edwin Dhas Key Points: Connect function variables as input to the decoder – (3m) Logically OR the outputs correspond to present minterms to obtain the output. – (4m)</p>
9	<p>Explain the working of 2:4 binary decoder(7m) (BTL - 2) Answer Page No: 3.53-3.54 in D.Edwin Dhas Key Points: Truth Table – (3m) Logic Diagram – (4m)</p> <p>Design a 4 – input priority encoder (8m) (BTL - 4) Answer Page No: 3.70-3.71 in D.Edwin Dhas Key Points: Truth Table - (2m) K – Map Simplification – (3m) Logic Diagram – (3m)</p>
	<p>Implement the following boolean function using 8 to 1 Multiplexer $F(A, B, C, D) = A'BD' + ACD + B'CD + A'C'D$. Also implement the function using 16 to 1 Multiplexer.(BTL - 5) (13m) (May – June 2014) Answer Page No: 3.38-3.39 in D.Edwin Dhas</p>

10	Key Points: Implementation table – (6m) Implementation – (7m)
11	Implement the following Boolean function with 8:1 Multiplexer (7m) (BTL - 3) $F(A,B,C,D) = \sum m(0, 2, 6, 10, 11, 12, 13) + d(3, 8, 14)$ Answer Page No: 3.40-3.41 in D.Edwin Dhas Key Points: Implementation table – (3m) Implementation – (4m)
	Realize $F(w, x, y, z) = \sum (1, 4, 6, 7, 8, 9, 10, 11, 15)$ using 4 to 1 MUX (7m) (BTL - 3) Answer Page No: 3.37-3.38 in D.Edwin Dhas Key Points: Implementation table – (3m) Implementation – (4m)
12	Implement 1:16 Demultiplexer using 1:4 Demultiplexer. (13m) (BTL - 3) Answer Page No: 3.51-3.52 in D.Edwin Dhas Key Points: Connect two least significant select lines (S1, S0) to select lines of four 4:1 DEMUX – (6m) Connect one more 4:1 Demultiplexer – (7m)
PART C	
1	Design full adder with inputs x, y, z and two outputs S and C. The circuits performs $x+y+z$, z is the input carry, C is the output carry and S is the Sum. (15m) (BTL - 4) (May – June 2016) using only Nor Gates using two half adders Answer Page No: 3.9 – 3.11 in D.Edwin Dhas Key Points: Full Adder using NOR gate implementation - (7M) Full Adder design using two half adders - (8M)
2	Design a 2 – bit Magnitude comparator using Gates (15m) (BTL - 2) (Nov – Dec 2014) Answer Page No: 3.94 – 3.96 in D.Edwin Dhas Key Points: Truth Table – (3m) K – Map Simplification – (5m) Logic Diagram – (5m)
3	Explain carry look ahead adder(15M) (BTL 1) Answer Page No: 3.20 in D.Edwin Dhas Definition –(2m) Logic diagram –(5m) Derivation –(5M) Eplanation-(3M)

UNIT III - SYNCHRONOUS SEQUENTIAL CIRCUITS																																																	
<p>Flip flops – SR, JK, T, D, Master/Slave FF – operation and excitation tables, Triggering of FF, Analysis and design of clocked sequential circuits – Design - Moore/Mealy models, state minimization, state assignment, circuit implementation – Design of Counters- Ripple Counters, Ring Counters, Shift registers, Universal Shift Register.</p>																																																	
PART * A																																																	
1	<p>Mention any two differences between the edge triggering and level triggering. [April/May 2010] (BTL1)</p> <p>Level Triggering: The input signal is sampled when the clock signal is either HIGH or LOW. It is sensitive to Glitches. Example: Latch.</p> <p>Edge Triggering: The input signal is sampled at the RISING EDGE or FALLING EDGE of the clock signal. It is not-sensitive to Glitches. Example: Flipflop.</p>																																																
2	<p>What is meant by programmable counter? Mention its application. [April/May- 2010] (BTL 1)</p> <p>A counter that divides an input frequency by a number which can be programmed into decades of synchronous down counters. Decades, with additional decoding and control logic, give the equivalent of a divide- by N counter system, where N can be made equal to any number. Appication: Microprocessor. Traffic light controller. Street light controller.</p>																																																
3	<p>Write the characteristic equation of a JK flip-flop. [April/May-2011, Nov/Dec- 2009](BTL 1)</p> <p>The characteristic equation of a JK flip-flop is given by $Q(\text{next}) = JQ' + K'Q$</p>																																																
4	<p>Realise T-FF from JK-FF. [April/May-2012](BTL 3)</p> <div style="text-align: center;"> <p>J-K Flip Flop to T Flip Flop</p> <table border="0"> <tr> <td style="text-align: center;"> <p>Conversion Table</p> <table border="1"> <thead> <tr> <th rowspan="2">T Input</th> <th colspan="2">Outputs</th> <th colspan="2">J-K Inputs</th> </tr> <tr> <th>Qp</th> <th>Qp+1</th> <th>J</th> <th>K</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>X</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> <td>X</td> <td>0</td> </tr> <tr> <td>1</td> <td>0</td> <td>1</td> <td>1</td> <td>X</td> </tr> <tr> <td>1</td> <td>1</td> <td>0</td> <td>X</td> <td>1</td> </tr> </tbody> </table> </td> <td style="text-align: center;"> <p>K-maps</p> <table border="1"> <tr> <td></td> <td>Qp</td> <td>0</td> <td>1</td> </tr> <tr> <td>T</td> <td>0</td> <td>0</td> <td>X</td> </tr> <tr> <td>1</td> <td>X</td> <td>1</td> <td>X</td> </tr> <tr> <td></td> <td></td> <td>J=T</td> <td></td> </tr> </table> </td> <td style="text-align: center;"> <p>Logic Diagram</p> </td> </tr> </table></div>	<p>Conversion Table</p> <table border="1"> <thead> <tr> <th rowspan="2">T Input</th> <th colspan="2">Outputs</th> <th colspan="2">J-K Inputs</th> </tr> <tr> <th>Qp</th> <th>Qp+1</th> <th>J</th> <th>K</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>X</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> <td>X</td> <td>0</td> </tr> <tr> <td>1</td> <td>0</td> <td>1</td> <td>1</td> <td>X</td> </tr> <tr> <td>1</td> <td>1</td> <td>0</td> <td>X</td> <td>1</td> </tr> </tbody> </table>	T Input	Outputs		J-K Inputs		Qp	Qp+1	J	K	0	0	0	0	X	0	1	1	X	0	1	0	1	1	X	1	1	0	X	1	<p>K-maps</p> <table border="1"> <tr> <td></td> <td>Qp</td> <td>0</td> <td>1</td> </tr> <tr> <td>T</td> <td>0</td> <td>0</td> <td>X</td> </tr> <tr> <td>1</td> <td>X</td> <td>1</td> <td>X</td> </tr> <tr> <td></td> <td></td> <td>J=T</td> <td></td> </tr> </table>		Qp	0	1	T	0	0	X	1	X	1	X			J=T		<p>Logic Diagram</p>
<p>Conversion Table</p> <table border="1"> <thead> <tr> <th rowspan="2">T Input</th> <th colspan="2">Outputs</th> <th colspan="2">J-K Inputs</th> </tr> <tr> <th>Qp</th> <th>Qp+1</th> <th>J</th> <th>K</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>X</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> <td>X</td> <td>0</td> </tr> <tr> <td>1</td> <td>0</td> <td>1</td> <td>1</td> <td>X</td> </tr> <tr> <td>1</td> <td>1</td> <td>0</td> <td>X</td> <td>1</td> </tr> </tbody> </table>	T Input	Outputs		J-K Inputs		Qp	Qp+1	J	K	0	0	0	0	X	0	1	1	X	0	1	0	1	1	X	1	1	0	X	1	<p>K-maps</p> <table border="1"> <tr> <td></td> <td>Qp</td> <td>0</td> <td>1</td> </tr> <tr> <td>T</td> <td>0</td> <td>0</td> <td>X</td> </tr> <tr> <td>1</td> <td>X</td> <td>1</td> <td>X</td> </tr> <tr> <td></td> <td></td> <td>J=T</td> <td></td> </tr> </table>		Qp	0	1	T	0	0	X	1	X	1	X			J=T		<p>Logic Diagram</p>		
T Input		Outputs		J-K Inputs																																													
	Qp	Qp+1	J	K																																													
0	0	0	0	X																																													
0	1	1	X	0																																													
1	0	1	1	X																																													
1	1	0	X	1																																													
	Qp	0	1																																														
T	0	0	X																																														
1	X	1	X																																														
		J=T																																															
5	<p>How many flip-flops are required to build a binary counter that counts from 0 to 1023? [April/May-2013](BTL 3)</p> <p>If the number of flip-flops required is n, then $2^n - 1 = 1023$ $n = 10$ since $2^{10} = 1024$</p>																																																
6	<p>Compare the logics of synchronous counter and ripple counter. [April/May-2014, Nov/Dec-2009](BTL 4)</p> <p>Asynchronous counter: In this type of counter flipflop are connected in such a way that output of first flip-flop drives the clock for next flip-flop. All the flip-flop are not clocked simultaneously. Logic circuit is very simple even for more number of states.</p> <p>synchronous counter: In this type there is no connection between output of first flip-flop and clock input of the next flip-flop. All the flip-flop are clocked simultaneously. Design involves complex logic circuit as number of states increases.</p>																																																
7	<p>Sketch the logic diagram of a clocked SR flip-flop. [April/May-2014](BTL 6)</p>																																																

																
8	<p>How do you eliminate the race around condition in a JK flip-flop?[Nov/Dec- 2010] (BTL 1)</p> <p>When the input to the JK flip-flop is $j=1$ and $k=1$, the race around condition occurs, i.e it occurs when the time period of the clock pulse is greater than the propagation delay of the flip flop.</p> <p>the output changes or toggles in a single clock period. If it toggles even number of times the output is same but if it toggles odd number of times then the output is complimented.</p> <p>To avoid race around condition we cant make the clock pulse smaller than the propagation delay so we use Master slave JK flip flop</p> <p>Positive or negative edge triggering</p>															
9	<p>Draw the state table and excitation table of T flip-flop. [Nov/Dec-2010](BTL 2)</p>															
10	<p>A 4-bit binary ripple counter is operated with clock frequency of 1KHz. What is the output frequency of its third Flip flop? [Nov/Dec-2011](BTL 4)</p> <p>The output frequency of third flip-flop is: $\frac{1}{2^3} = 1/8\text{KHz}$.</p>															
11	<p>Realize JK flip-flop using D flip-flop. [Nov/Dec-2011](BTL 1)</p> <div style="text-align: center;"> <p>J-K Flip Flop to D Flip Flop</p> <table border="1" style="display: inline-table; margin-right: 20px;"> <caption>Conversion Table</caption> <thead> <tr> <th>D Input</th> <th>Outputs Qp Qp+1</th> <th>J-K Inputs J K</th> </tr> </thead> <tbody> <tr><td>0</td><td>0 0</td><td>0 X</td></tr> <tr><td>0</td><td>1 0</td><td>X 1</td></tr> <tr><td>1</td><td>0 1</td><td>1 X</td></tr> <tr><td>1</td><td>1 0</td><td>X 0</td></tr> </tbody> </table> <div style="display: inline-block; text-align: center;"> <p>K-maps</p>  </div> <div style="display: inline-block; text-align: center;"> <p>Logic Diagram</p>  </div> </div>	D Input	Outputs Qp Qp+1	J-K Inputs J K	0	0 0	0 X	0	1 0	X 1	1	0 1	1 X	1	1 0	X 0
D Input	Outputs Qp Qp+1	J-K Inputs J K														
0	0 0	0 X														
0	1 0	X 1														
1	0 1	1 X														
1	1 0	X 0														
12	<p>Design a 3-bit ring counter and find the mod of the designed counter. [Nov/Dec- 2012] (BTL 6)</p> 															
13	<p>Define latches. [Nov/Dec-2013](BTL 1)</p> <p>Latch is a simple memory element, which consists of a pair of logic gates with their inputs and outputs inter connected in a feedback arrangement, which permits a single bit to be stored.</p>															
14	<p>Write short notes on Digital Clock. [Nov/Dec-2013](BTL 1)</p> <p>A digital clock is a simplified logic diagram of a digital clock that displays seconds, minutes, and hours. First, a 60 Hz sinusoidal ac voltage is converted to a 60 Hz pulse waveform and divided own to a 1Hz pulse waveform by a divide-by-60 counter formed by a divide-by-10 counter allowed by a divide-by-6 counter. Both the seconds and minutes counts are also produced by divide-by-60 counters.</p>															
15	<p>Define latches. [Nov/Dec-2013] (BTL 1)</p> <p>Latch is a simple memory element, which consists of a pair of logic gates with their inputs and outputs inter connected in a feedback arrangement, which permits a single bit to be stored.</p>															
16	<p>Write short notes on Digital Clock. [Nov/Dec-2013] (BTL 1)</p> <p>A digital clock is a simplified logic diagram of a digital clock that displays seconds, minutes, and hours. First, a 60 Hz sinusoidal ac voltage is converted to a 60 Hz pulse waveform and divided own to a 1Hz pulse waveform by a</p>															

	divide-by-60 counter formed by a divide-by-10 counter allowed by a divide-by-6 counter. Both the seconds and minutes counts are also produced by divide-by-60 counters.												
17	<p>Difference between flipflop and latches (BTL 4)</p> <table border="1"> <thead> <tr> <th>Latches</th> <th>Flip Flops</th> </tr> </thead> <tbody> <tr> <td>Latches are building blocks of sequential circuits and these can be built from logic gates</td> <td>Flip flops are also building blocks of sequential circuits. But, these can be built from the latches.</td> </tr> <tr> <td>Latch continuously checks its inputs and changes its output correspondingly.</td> <td>Flip flop continuously checks its inputs and changes its output correspondingly only at times determined by clocking signal</td> </tr> <tr> <td>The latch is sensitive to the duration of the pulse and can send or receive the data when the switch is on</td> <td>Flipflop is sensitive to a signal change. They can transfer data only at the single instant and data cannot be changed until next signal change. Flip flops are used as a register.</td> </tr> <tr> <td>It is based on the enable function input</td> <td>It works on the basis of clock pulses</td> </tr> <tr> <td>It is a level triggered, it means that the output of the present state and input of the next state depends on the level that is binary input 1 or 0.</td> <td>It is an edge triggered, it means that the output and the next state input changes when there is a change in clock pulse whether it may a +ve or -ve clock pulse.</td> </tr> </tbody> </table>	Latches	Flip Flops	Latches are building blocks of sequential circuits and these can be built from logic gates	Flip flops are also building blocks of sequential circuits. But, these can be built from the latches.	Latch continuously checks its inputs and changes its output correspondingly.	Flip flop continuously checks its inputs and changes its output correspondingly only at times determined by clocking signal	The latch is sensitive to the duration of the pulse and can send or receive the data when the switch is on	Flipflop is sensitive to a signal change. They can transfer data only at the single instant and data cannot be changed until next signal change. Flip flops are used as a register.	It is based on the enable function input	It works on the basis of clock pulses	It is a level triggered, it means that the output of the present state and input of the next state depends on the level that is binary input 1 or 0.	It is an edge triggered, it means that the output and the next state input changes when there is a change in clock pulse whether it may a +ve or -ve clock pulse.
Latches	Flip Flops												
Latches are building blocks of sequential circuits and these can be built from logic gates	Flip flops are also building blocks of sequential circuits. But, these can be built from the latches.												
Latch continuously checks its inputs and changes its output correspondingly.	Flip flop continuously checks its inputs and changes its output correspondingly only at times determined by clocking signal												
The latch is sensitive to the duration of the pulse and can send or receive the data when the switch is on	Flipflop is sensitive to a signal change. They can transfer data only at the single instant and data cannot be changed until next signal change. Flip flops are used as a register.												
It is based on the enable function input	It works on the basis of clock pulses												
It is a level triggered, it means that the output of the present state and input of the next state depends on the level that is binary input 1 or 0.	It is an edge triggered, it means that the output and the next state input changes when there is a change in clock pulse whether it may a +ve or -ve clock pulse.												
18	<p>What are the classification of sequential circuits? (BTL 1)</p> <p>The sequential circuits are classified on the basis of timing of their signals into Two types. They are,</p> <ol style="list-style-type: none"> 1)Synchronous sequential circuit. 2)Asynchronous sequential circuit. 												
19	<p>Define Flip flop. What are the different types of flip-flop? (BTL 1)</p> <p>The basic unit for storage is flip flop. A flip-flop maintains its output state either at 1 or 0 until directed by an input signal to change its state.</p> <p>There are various types of flip flops. Some of them are mentioned below they are,</p> <ul style="list-style-type: none"> _RS flip-flop _SR flip-flop _D flip-flop _JK flip-flop _T flip-flop 												
20	<p>What is the operation of RS flip-flop? (BTL 1)</p> <p>When R input is low and S input is high the Q output of flip-flop is set. When R input is high and S input is low the Q output of flip-flop is reset. When both the inputs R and S are low the output does not change When both the inputs R and S are high the output is unpredictable.</p>												
21	<p>What is the operation of SR flip-flop? (BTL 1)</p> <p>When R input is low and S input is high the Q output of flip-flop is set. When R input is high and S input is low the Q output of flip-flop is reset. When both the inputs R and S are low the output does not change. When both the inputs R and S are high the output is unpredictable.</p>												
22	<p>Define race around condition.(BTL 1)</p> <p>In JK flip-flop output is fed back to the input. Therefore change in the output results change in the input. Due to this in the positive half of the clock pulse if both J and K are high then output toggles continuously. This condition is called 'race around condition'.</p>												
23	<p>What is a master-slave flip-flop?(BTL 1)</p> <p>A master-slave flip-flop consists of two flip-flops where one circuit serves as a master and the other as a slave.</p>												
24	<p>Define shift registers.(BTL 1)</p>												

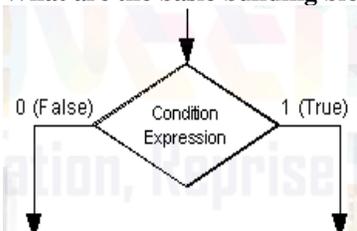
	The binary information in a register can be moved from stage to stage within the register or into or out of the register upon application of clock pulses. This type of bit movement or shifting is essential for certain arithmetic and logic operations used in microprocessors. This gives rise to group of registers called shift registers.		
25	What are the different types of shift type?(BTL 1) There are five types. They are, _Serial In Serial Out Shift Register _Serial In Parallel Out Shift Register _Parallel In Serial Out Shift Register _Parallel In Parallel Out Shift Register _Bidirectional Shift Register		
26	Difference between combinational and sequential circuit (BTL 4)		
	S.NO	Combinational circuit	
	1	It contains no memory	
	2	The present value of it's output are determined solely by the present value of it's input	
	Sequential circuit		
		It contains memory element	
		The present value of it's output are determined by the present value of it's input and it's past value	
		It's behavior is described by the set of next-state(memory) functions and the set of output functions	
27	Difference between moore and mealy (BTL 4)		
		Mealy	Moore
	1	Output depends on the present state and present inputs	Outputs depends only on the present state
	2	The output changes asynchronously with the enabling clock edge	Since the output change when the state changes, and the state change is synchronous with the enabling clock edge.outputs change synchronously with this clock edge
	3	A counter is not a Mealy machine	A counter is a Moore machine
	4	A mealy machine will have the same or fewer states than a Moore machine	
PART * B			
1.	What is SR latch? Explain its operation. (8m) (BTL - 2) Title: Digital Electronics Author: D.Edwin Dhas Page No:4.43 Key Points: SR Latch – (2m) Cases of SR Latch – (4m) Gated SR Latch – (2m)		
	Explain the operation of JK and clocked JK flip-flops with suitable diagrams. (7m) (BTL - 2) Title: Digital Electronics Author: D.Edwin Dhas Page No:4.12 Key Points: J – K Flip Flop – (2m) Operation of JK Flip Flop – (3m) Race – Round Condition – (2m)		
2.	Draw the clocked RS flip – flop and explain with truth table. (8m) (BTL - 2) Title: Digital Electronics Author: D.Edwin Dhas Page No:4.6		

	<p>Key Points: Positive edge triggered SR Flip – Flop – (4m) Operation – (2m) Negative Edge triggered SR Flip – Flop – (3m)</p>
	<p>Draw the logic diagram of a D FF using NAND gates and explain. (7m) (BTL - 2) Title: Digital Electronics Author: D.Edwin Dhas Page No:4.9 Key Points: D Flip – Flop using NAND gates – (3m) Truth Table – (2m) Negative Edge triggered D FF – (2m)</p>
3.	<p>Convert a SR Flip Flop into a D Flip Flop. (7m) (BTL - 3) Title: Digital Electronics Author: D.Edwin Dhas Page No:4.23 Key Points: Excitation table–(3m) K – Map simplification – (2m) Logic Diagram – (2m)</p>
	<p>Convert D Flip – flop to T Flip – Flop. (8m) (BTL - 3) Title: Digital Electronics Author: D.Edwin Dhas Page No:4.24 Key Points: Excitation table – (3m) K – Map simplification – (3m) Logic Diagram – (2m)</p>
4.	<p>How will you convert a D Flip – flop into JK Flip – Flop? (7m) (BTL - 1) Title: Digital Electronics Author: D.Edwin Dhas Page No:4.30 Key Points: Excitation table – (3m) K – Map simplification – (2m) Logic Diagram – (2m)</p>
	<p>A Synchronous Counter with four JK flip – flops has the following connections: (8m) (BTL - 4) $J_A = K_A = 1, J_B = Q_A Q_D, K_B = Q_A$ $J_C = K_C = Q_A Q_B$ $J_D = Q_A Q_B Q_C \text{ and } K_D = Q_A$ Determine the modulus n of the counter and draw the output waveforms of the same. Title: Digital Electronics Author: D.Edwin Dhas Page No:4.137 Key Points: Next state map for JK Flip – Flop –3m Transition table – (3m) Output Waveform's – (2m)</p>
	<p>A sequential circuit with 2D FFs A and B and input X and output Y is specified by the following next state and output equations. (13m) (BTL - 4) $A(t+1) = AX + BX$ $B(t+1) = A'X$</p>

	<p>$Y = (A+B)X'$ Draw the logic diagram Derive the state table Derive the state diagram Title: Digital Electronics Author: D.Edwin Dhas Page No:4.54 Key Points: Logic Diagram – (3m) State table – (3m) Transition Table – (3m) State Diagram – (4m)</p>																																												
5.	<p>Reduce the number of states in the following state table and tabulate the reduced state table</p> <table border="1"> <thead> <tr> <th rowspan="2">Present State</th> <th colspan="2">Next State</th> <th colspan="2">Output</th> </tr> <tr> <th>x = 0</th> <th>x = 1</th> <th>x = 0</th> <th>x = 1</th> </tr> </thead> <tbody> <tr> <td>A</td> <td>f</td> <td>b</td> <td>0</td> <td>0</td> </tr> <tr> <td>B</td> <td>d</td> <td>c</td> <td>0</td> <td>0</td> </tr> <tr> <td>C</td> <td>f</td> <td>e</td> <td>0</td> <td>0</td> </tr> <tr> <td>D</td> <td>g</td> <td>a</td> <td>1</td> <td>0</td> </tr> <tr> <td>E</td> <td>d</td> <td>c</td> <td>0</td> <td>0</td> </tr> <tr> <td>F</td> <td>f</td> <td>b</td> <td>1</td> <td>1</td> </tr> <tr> <td>G</td> <td>g</td> <td>h</td> <td>0</td> <td>1</td> </tr> </tbody> </table> <p>ii) Starting from state a, and input sequence 01110010011, determine the output sequence for the given and reduces state table. (13m) (BTL - 2) Title: Digital Electronics Author: D.Edwin Dhas Page No:4.84 Key Points: Identify the Equivalent states – (6m) Reduced state table – (7m)</p>	Present State	Next State		Output		x = 0	x = 1	x = 0	x = 1	A	f	b	0	0	B	d	c	0	0	C	f	e	0	0	D	g	a	1	0	E	d	c	0	0	F	f	b	1	1	G	g	h	0	1
Present State	Next State		Output																																										
	x = 0	x = 1	x = 0	x = 1																																									
A	f	b	0	0																																									
B	d	c	0	0																																									
C	f	e	0	0																																									
D	g	a	1	0																																									
E	d	c	0	0																																									
F	f	b	1	1																																									
G	g	h	0	1																																									
6.	<p>Design a sequential circuit using RS Flip – Flop for the state table given below using minimum number of flip – flops. (13m) (BTL - 4)</p> <table border="1"> <thead> <tr> <th rowspan="2">Present state</th> <th colspan="2">Next state</th> <th colspan="2">Output</th> </tr> <tr> <th>X = 0</th> <th>X = 1</th> <th>X = 0</th> <th>X = 1</th> </tr> </thead> <tbody> <tr> <td>A</td> <td>A</td> <td>B</td> <td>0</td> <td>0</td> </tr> <tr> <td>B</td> <td>C</td> <td>D</td> <td>0</td> <td>0</td> </tr> <tr> <td>C</td> <td>A</td> <td>D</td> <td>0</td> <td>0</td> </tr> <tr> <td>D</td> <td>E</td> <td>F</td> <td>0</td> <td>1</td> </tr> <tr> <td>E</td> <td>A</td> <td>F</td> <td>0</td> <td>1</td> </tr> <tr> <td>F</td> <td>G</td> <td>F</td> <td>0</td> <td>1</td> </tr> <tr> <td>G</td> <td>A</td> <td>F</td> <td>0</td> <td>1</td> </tr> </tbody> </table> <p>Title: Digital Electronics Author: D.Edwin Dhas Page No:4.84 Key Points: Minimized state table – (4m) K – Map Simplification – (6m) Logic Diagram – (3m)</p>	Present state	Next state		Output		X = 0	X = 1	X = 0	X = 1	A	A	B	0	0	B	C	D	0	0	C	A	D	0	0	D	E	F	0	1	E	A	F	0	1	F	G	F	0	1	G	A	F	0	1
Present state	Next state		Output																																										
	X = 0	X = 1	X = 0	X = 1																																									
A	A	B	0	0																																									
B	C	D	0	0																																									
C	A	D	0	0																																									
D	E	F	0	1																																									
E	A	F	0	1																																									
F	G	F	0	1																																									
G	A	F	0	1																																									
7.	<p>Design a Synchronous sequential circuit using JK for the given state diagram. (13m) (BTL - 4)</p>																																												

	<p>Title: Digital Electronics Author: D.Edwin Dhas Page No:4.82 Key Points: Excitation table – (2m) K – Map Simplification – (4m) Logic Diagram – (2m) Derive Circuit Output and flip – flops considering unused states – (2m) Logic Diagram – (3m)</p>
8.	<p>Draw a 4 – bit serial – in – serial – out shift register and draw its waveforms. (7m) (BTL - 2) Title: Digital Electronics Author: D.Edwin Dhas Page No:4.100 Key Points: Shift Register – (2m) Shift Left operation – (3m) Waveforms – (2m)</p>
	<p>Draw a 4 – bit parallel – in – serial – out shift register and explain briefly. (8m) (BTL -2) Title: Digital Electronics Author: D.Edwin Dhas Page No:4.103 Key Points: PISO Shift Register – (8m)</p>
9	<p>Draw and explain the operation of parallel – in – parallel – out shift registers. (7m) (BTL - 2) Title: Digital Electronics Author: D.Edwin Dhas Page No:4.104 Key Points: PIPO Shift Register – (7m)</p>
	<p>Draw a six stage ring counter and explain its operation. (8m) (BTL - 2) Title: Digital Electronics Author: D.Edwin Dhas Page No:4.107 Key Points: Diagram for six stage ring counter – (4m) Illustrating operation for six – stage ring counter – (4m)</p>
10.	<p>Draw a 4 – bit Johnson counter and explain its operation. (13m) (BTL - 2) Title: Digital Electronics Author: D.Edwin Dhas Page No:4.109 Key Points: Diagram for four – bit Johnson counter – (4m)</p>

	Four – bit Johnson Sequence – (5m) Timing Sequence – (4m)
11.	Explain in detail the operation of a 4 – bit binary ripple counter (13m) (BTL - 2) Title: Digital Electronics Author: D.Edwin Dhas Page No:4.38 Key Points: Diagram of 4 – bit ripple counter – (6m) Timing Diagram – (7m)
	PART C
1	Explain the working of 4 – bit synchronous binary up counter (15m) (BTL - 2) Title: Digital Electronics Author: D.Edwin Dhas Page No:4.43-4.45 Key Points: Three – bit synchronous binary counter – (5m) Timing Diagram – (5m) State sequence – (5m)
2	Design a synchronous 3 bit up/down counter using T flip flop. (15m) (BTL - 4) Title: Digital Electronics Author: D.Edwin Dhas Page No:4.64-4.67 State table – (3m) Excitation table – (3m) Next state table – (3m) Diagram. – (4m)
3	Design and explain the working of an up – down ripple counter (15m) (BTL - 4) Title: Digital Electronics Author: D.Edwin Dhas Page No:4.40-4.41 Key Points: Diagram of 4 – bit up/down ripple counter – (6m) Timing Diagram for up/down counter – (7m)

UNIT IV - ASYNCHRONOUS SEQUENTIAL CIRCUITS							
Stable and Unstable states, output specifications, cycles and races, state reduction, race free assignments, Hazards, Essential Hazards, Pulse mode sequential circuits, Design of Hazard free circuits.							
PART * A							
1	<p>What are hazard free digital circuits? [April/May-2010] (BTL 1) A circuit which has no hazard like static-0-hazard and static-1-hazard is called hazard free digital circuit.</p>						
2	<p>What are the basic building blocks of a algorithmic state machine chart? [April/May-2011](BTL 1)</p> 						
3	<p>What is state table? [April/May-2012] (BTL 1) The state table representation of a sequential circuit consists of three sections labelled present state, next state and output. The present state designates the state of flip-flops before the occurrence of a clock pulse. The next state shows the states of flip-flops after the clock pulse, and the output section lists the value of the output variables during the present state.</p>						
4	<p>What are Hazards? [April/May-2013, Nov/Dec-2009] (BTL 1) The unwanted switching transients (glitches) that may appear at the output of a circuit are called Hazards.</p>						
5	<p>Distinguish between a flowchart and an ASM chart. [April/May-2013, Nov/Dec- 2009] (BTL 1) A conventional flow chart describes the square of procedural steps and decision paths for an algorithm without concern for their time relationship. The ASM chart describes the sequence of event as well as timing relationship between the states of a sequential controller and the events that occur while going from one state to the next.</p>						
6	<p>What is a state diagram? Give an example. [April/May-2014] (BTL 1) A state diagram is a type of diagram used in computer science and related fields to describe the behaviour of systems. State diagrams require that the system described is composed of a finite number of states; sometimes, this is indeed the case, while at other times this is a reasonable abstraction. Many forms of state diagrams exist, which differ slightly and have different semantics.</p>						
7	<p>Under what circumstances asynchronous circuits are prepared. [Nov/Dec-2011] (BTL 1) Fundamental mode asynchronous circuits Pulse mode asynchronous circuits</p>						
8	<p>Differentiate fundamental mode and pulse mode asynchronous sequential circuits. [Nov/Dec-2012](BTL 1)</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 50%;">Fundamental mode sequential circuits</td> <td style="width: 50%;">Pulse mode sequential circuits.</td> </tr> <tr> <td>(i)Memory elements are clocked flip-flops</td> <td>(i) Memory elements are either unlocked flip-flops or time delay elements.</td> </tr> <tr> <td>(ii)Easier to design</td> <td>(ii)More difficult to design</td> </tr> </table>	Fundamental mode sequential circuits	Pulse mode sequential circuits.	(i)Memory elements are clocked flip-flops	(i) Memory elements are either unlocked flip-flops or time delay elements.	(ii)Easier to design	(ii)More difficult to design
Fundamental mode sequential circuits	Pulse mode sequential circuits.						
(i)Memory elements are clocked flip-flops	(i) Memory elements are either unlocked flip-flops or time delay elements.						
(ii)Easier to design	(ii)More difficult to design						
9	<p>What is synchronous sequential circuit? [Nov/Dec-2011] (BTL 1) In synchronous circuits the input are pulses (or levels and pulses) with certain restrictions on pulse width and circuit propagation delay. Therefore synchronous circuits can be divided into clocked sequential circuits and unclocked or pulsed sequential circuits. In a clocked sequential circuit which has flip-flops or, in some instances, gated latches, for its memory elements there is a (synchronizing) periodic clock connected to the clock inputs of all the memory elements of the circuit, to synchronize all internal changes of state</p>						
10	<p>Write short notes on Hazards. [Nov/Dec-2013] (BTL 1) The unwanted switching transients (glitches) that may appear at the output of a circuit are called Hazards. Static-0-Hazard Static-1-Hazard</p>						

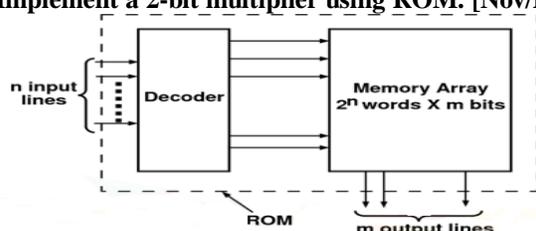
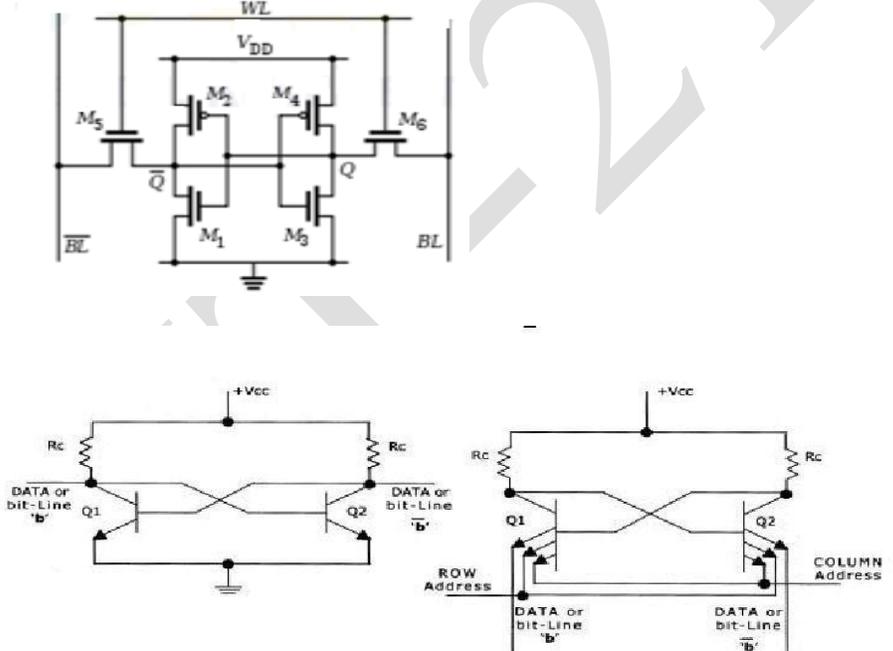
11	When do race condition occur? (BTL 1) -two or more binary state variables change their value in response to the change in i/p Variable		
12	What is non critical race? (BTL 1) -final stable state does not depend on the order in which the state variable changes -race condition is not harmful		
13	What is critical race? (BTL 1) -final stable state depends on the order in which the state variable changes -race condition is harmful		
14	What are the different techniques used in state assignment? (BTL 1) -shared row state assignment -one hot state assignment		
15	What is static 1 hazard? (BTL 1) -output goes momentarily 0 when it should remain at 1		
16	What are static 0 hazards? (BTL 1) -output goes momentarily 1 when it should remain at 0		
17	What is dynamic hazard? (BTL 1) -output changes 3 or more times when it changes from 1 to 0 or 0 to 1		
18	What is the cause for essential hazards? (BTL 1) -unequal delays along 2 or more path from same input		
19	What is a cycle? (BTL 1) A cycle occurs when an asynchronous circuit makes a transition through a series of unstable states. If a cycle does not contain a stable state, the circuit will go from one unstable to stable to another, until the inputs are changed.		
20	Write a short note on fundamental mode asynchronous circuit. (BTL 1) Fundamental mode circuit assumes that. The input variables change only when the circuit is stable. Only one input variable can change at a given time and inputs are levels and not pulses.		
21	Write a short note on pulse mode circuit. (BTL 1) Pulse mode circuit assumes that the input variables are pulses instead of level. The width of the pulses is long enough for the circuit to respond to the input and the pulse width must not be so long that it is still present after the new state is reached.		
22	Define state table. (BTL 1) For the design of sequential counters we have to relate present states and next states. The table, which represents the relationship between present states and next states, is called state table.		
23	What is state equivalence theorem? (BTL 1) Two states SA and SB, are equivalent if and only if for every possible input X sequence, the outputs are the same and the next states are equivalent i.e., if $SA(t+1) = SB(t+1)$ and $ZA = ZB$ then $SA = SB$.		
24	What is the cause for essential hazards? (BTL 1) -unequal delays along 2 or more path from same input		
25	What are the significance of state assignment? (BTL 1) In synchronous circuits-state assignments are made with the objective of circuit Reduction Asynchronous circuits-its objective is to avoid critical races		
26	Difference between synchronous sequential circuit and asynchronous sequential circuit (BTL 4)		
	S.NO	Synchronous sequential	Asynchronous sequential
	1	Synchronous sequential circuit is a system whose behaviour can be defined from the knowledge of the signals at discrete instants of time	The circuit in which the changes in the input signals can affect memory elements at any instants of the time is called asynchronous circuit
	2	The signals can affect the memory elements only at discrete instant of time	In this circuit, clock is absent and hence the state changes can occur according to delay time of the logic
	3	Easier to design	More difficult to design

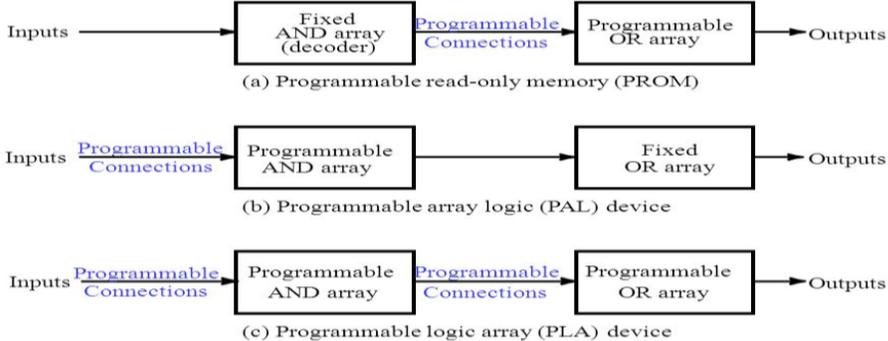
	4	Memory elements are clocked flipflops	Memory elements are either unclocked flipflops or time delay elements
PART * B			
1.	<p>Illustrate the Types of Asynchronous Sequential Circuits(7m) (BTL - 2) Title: Digital Electronics Author: D.Edwin Dhas Page No:6.17-6.29 Key Points: Fundamental Mode Circuits – (3m) Pulse Mode Circuits – (4m)</p>		
2.	<p>An asynchronous sequential circuit is described by the following excitation and output function. (Dec 14) (13M) (BTL 6)</p> $Y = X_1X_2 + (X_1 + X_2)Y, Z = Y$ <p>Draw the logic diagram of the circuit Derive the transition table and output map Describe the behavior of the circuit Title: Digital Electronics Author: D.Edwin Dhas Page No:6.35-6.39 Key Points: Logic Diagram – (13m) State table – (4m) Transition Table – (3m) Output Map – (3m)</p>		
3.	<p>An asynchronous sequential circuit has two internal states and one output. The excitation and output function describing the circuit are as follows. (13m) (BTL - 4)</p> $Y_1 = x_1x_2 + x_1y_2 + x_2y_1$ $Y_2 = x_2 + x_1y_1y_2 + x_1y_1$ $Z = x_2 + y_1$ <p>Title: Digital Electronics Author: D.Edwin Dhas Page No:6.45-6.50 Key Points: Logic Diagram – (3m) State table – (4m) Transition Table – (3m) Output Map – (3m)</p>		
4.	<p>Design an asynchronous sequential circuit with two inputs X and Y and with one output Z. Whenever Y is 1, input X is transferred to Z. When Y is 0, the output does not change in X. (13m) (June – 16 /BTL - 4) Title: Digital Electronics Author: D.Edwin Dhas Page No:6.35-6.39 Key Points: Draw the state Diagram – (3m) Derive the Primitive Flow Table – (3m) State Assignment – (3m) Realization of circuit using logic elements – (2m) Realization of circuit using SR latch – (2m)</p>		
5.	<p>Design a two – input (x_1, x_2), two – output (z_1, z_2) fundamental – mode circuit that has the following specifications. When $x_1x_2 = 00$, $z_1z_2 = 00$. The output 10 will be produced following the occurrence of the input sequence 00 – 01 – 11. The output will remain at 10 until the input returns to 00 at which it becomes 00. An</p>		

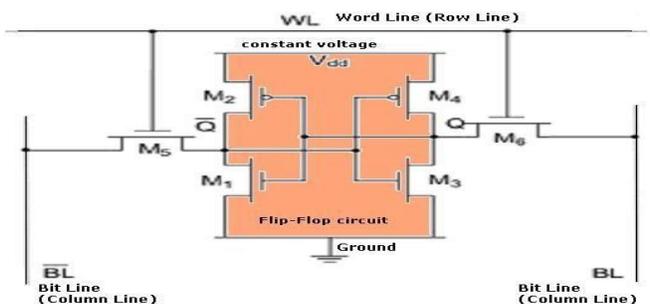
	<p>output of 01 will be produced following the receipt of the input sequence 00 – 10 – 11. And once again, the output will remain at 01 until a 00 input occurs, which returns the output to 00. (13m) (BTL - 4)</p> <p>Title: Digital Electronics Author: D.Edwin Dhas Page No:6.17-6.20 Key Points: Draw the state Diagram – (3m) Derive the Primitive Flow Table – (3m) State Assignment – (3m) K – Map Simplification – (2m) Logic Diagram – (2m)</p>
6.	<p>Design a T Flip – flop from logic gates. (7m) (BTL - 4)</p> <p>Title: Digital Electronics Author: D.Edwin Dhas Page No:4.15-4.17 Key Points: Draw the state Diagram – (2m) Derive the Primitive Flow Table – (1m) State Assignment – (1m) K – Map Simplification – (2m) Logic Diagram – (1m)</p>
7.	<p>Design a asynchronous D – type latch with two inputs G and D and output Q. Assume fundamental mode of operation. (13m) (BTL - 4)</p> <p>Title: Digital Electronics Author: D.Edwin Dhas Page No:6.17-6.20 Key Points: Draw the state Diagram – (3m) Derive the Primitive Flow Table – (3m) State Assignment – (3m) K – Map Simplification – (2m) Logic Diagram – (2m)</p>
8.	<p>What is a hazard? Explain the different types of hazards. What is an essential hazard? Discuss in detail how hazards can be eliminated. (13m) (BTL - 1)</p> <p>Title: Digital Electronics Author: D.Edwin Dhas Page No:6.63-6.70 Key Points: Hazard – Definition-(4M) Types of Hazards(4M) Essential Hazard(3M) Hazard elimination(2M)</p>
9.	<p>Give the hazard – free realization for the Boolean function. $f(A, B, C, D) = \sum m (0, 2, 6, 7, 8, 10, 12)$ (8m) BTL - 4</p> <p>Title: Digital Electronics Author: D.Edwin Dhas Page No:6.70 Key Points: K – Map Simplification(4M) Logic Diagram(4M)</p>
PART C	

1	<p>Find a static and dynamic hazard free realization for the following function using i) NAND gates ii) NOR gates $F(a, b, c, d) = \sum m(1, 5, 7, 14, 15)$. (15m) (BTL - 4) Title: Digital Electronics Author: D.Edwin Dhas Page No:6.67-6.68 Key Points: Circuit realization using NOR gates – (8m) Circuit Realization gates using NAND gates – (7m)</p>
2	<p>Write the analysis procedure for an asynchronous fundamental sequential circuit with example. (15m)(BTL - 4) Title: Digital Electronics Author: D.Edwin Dhas Page No:6.17-6.20 Steps for analysis procedure. – (7m) Example. – (8m)</p>
3	<p>Write the design procedure for an asynchronous fundamental sequential circuit with example. (15m)(BTL - 4) Title: Digital Electronics Author: D.Edwin Dhas Page No:6.34-6.39 Steps for procedure.- (7m) Example –(8m)</p>

UNIT V-MEMORY DEVICES AND DIGITAL INTEGRATED CIRCUITS	
Basic memory structure – ROM -PROM – EPROM – EEPROM –EAPROM, RAM – Static and dynamic RAM Programmable Logic Devices – Programmable Logic Array (PLA) - Programmable Array Logic (PAL) – Field Programmable Gate Arrays (FPGA) - Implementation of combinational logic circuits using PLA, PAL.Digital integrated circuits: Logic levels, propagation delay, power dissipation, fan-out and fan- in, noise margin, logic families and their characteristics-RTL, TTL, ECL, CMOS	
PART * A	
1	What is meant by memory Expansion? Mention its limit. [April/May-2010(BTL 1)] The memory expansion can be achieved in two ways: by expanding word size and expanding memory capacity. Limitations: Memory capacity upto 16Mbytes. 24 address lines and 16 data lines.
2	What are the advantages of static RAM and Dynamic Ram? [April/May- 2010,Nov/Dec-2009](BTL 1) Static RAM: Access time is less. Fast operation. DYNAMIC RAM: It consumes less power. Cost is low.
3	What is difference between PAL and PLA? [April/May-2011, 2013, Nov/Dec- 2010](BTL 4) PLA: Both AND and OR arrays are programmable and Complex Costlier than PAL PAL: AND arrays are programmable OR arrays are fixed Cheaper and Simpler
4	Implement the exclusive or function using ROM. [April/May-2011](BTL 3) Can implement multi-input/multi-output logic functions inside of ROM. Data outputs are the logic functions and the address lines are the logic function inputs. We create a ROM Table to store the logic functions. When an input (or address) is presented, the value stored in the specified memory location appears at the data outputs. Each data output represents the correct value for its logic function
5	Compare Dynamic RAM with Static RAM. [April/May-2012](BTL 4) Static Ram is very costly. Dynamic Ram is cheaper. Static Ram contains Transistors. Dynamic Ram contains Capacitors. Static Ram is used in L1 and L2 cache. Dynamic Ram is used in system RAM.
6	Mention few applications of PLA and PAL. [April/May-2012] (BTL 1) Implement combinational circuits Implement sequential circuits Code converters Microprocessor based systems
7	What are the different types of programmable logic devices? [April/May-2013] (BTL 1) PROM PLA PAL GAL
8	List the advantages of PLDs. [April/May-2014, Nov/Dec-2010](BTL 1) low and fixed (two gate) propagation delays (typically down to 5 ns), simple,

	low-cost (free), design tools.
9	What is PAL? [Nov/Dec-2009] (BTL 1) PAL is programmable array logic, PAL consists of a programmable AND array and a fixed OR array with output logic.
10	What is access time and cycle time of a memory? [Nov/Dec-2010] (BTL 1) Access time is the maximum specified time within which a valid new data is put on the data bus after an address is applied. Cycle time is the minimum time for which an address must be held stable on the address bus in read cycle.
11	Implement a 2-bit multiplier using ROM. [Nov/Dec-2010] (BTL 3) 
12	How the memories are classified? (BTL 1) It is classified into two types: volatile non-volatile memory
13	Draw the logic diagram of a static RAM cell and Bipolar cell. [Nov/Dec-2012] (BTL1) 
14	What is volatile and non-volatile memory? [Nov/Dec-2013] (BTL 1) The memory which cannot hold the data when power is turned off is known as volatile memory. The memory which can hold the data when power is turned off is known as non-volatile memory
15	Give the advantages of RAM. [Nov/Dec-2013](BTL 1) Read and write the data. Data is accessed by using address of the memory location. Higher speed.

<p>16</p>	<p>Difference between RAM and ROM (BTL 4)</p> <table border="1" data-bbox="250 275 911 596"> <thead> <tr> <th>RAM</th> <th>ROM</th> </tr> </thead> <tbody> <tr> <td>1. Temporary Storage.</td> <td>1. Permanent storage.</td> </tr> <tr> <td>2. Store data in MBs.</td> <td>2. Store data in GBs.</td> </tr> <tr> <td>3. Volatile.</td> <td>3. Non-volatile.</td> </tr> <tr> <td>4.Used in normal operations.</td> <td>4. Used for startup process of computer.</td> </tr> <tr> <td>5. Writing data is faster.</td> <td>5. Writing data is slower.</td> </tr> </tbody> </table> <p style="text-align: center;">Difference between RAM and ROM</p>	RAM	ROM	1. Temporary Storage.	1. Permanent storage.	2. Store data in MBs.	2. Store data in GBs.	3. Volatile.	3. Non-volatile.	4.Used in normal operations.	4. Used for startup process of computer.	5. Writing data is faster.	5. Writing data is slower.						
RAM	ROM																		
1. Temporary Storage.	1. Permanent storage.																		
2. Store data in MBs.	2. Store data in GBs.																		
3. Volatile.	3. Non-volatile.																		
4.Used in normal operations.	4. Used for startup process of computer.																		
5. Writing data is faster.	5. Writing data is slower.																		
<p>17</p>	<p>Difference between DRAM and SRAM (BTL 4)</p> <table border="1" data-bbox="243 709 911 1146"> <thead> <tr> <th>DRAM</th> <th>SRAM</th> </tr> </thead> <tbody> <tr> <td>1. Constructed of tiny capacitors that leak electricity.</td> <td>1.Constructed of circuits similar to D flip-flops.</td> </tr> <tr> <td>2.Requires a recharge every few milliseconds to maintain its data.</td> <td>2.Holds its contents as long as power is available.</td> </tr> <tr> <td>3.Inexpensive.</td> <td>3.Expensive.</td> </tr> <tr> <td>4. Slower than SRAM.</td> <td>4. Faster than DRAM.</td> </tr> <tr> <td>5. Can store many bits per chip.</td> <td>5. Can not store many bits per chip.</td> </tr> <tr> <td>6. Uses less power.</td> <td>6.Uses more power.</td> </tr> <tr> <td>7.Generates less heat.</td> <td>7.Generates more heat.</td> </tr> <tr> <td>8. Used for main memory.</td> <td>8. Used for cache.</td> </tr> </tbody> </table> <p style="text-align: center;">Difference between SRAM and DRAM</p>	DRAM	SRAM	1. Constructed of tiny capacitors that leak electricity.	1.Constructed of circuits similar to D flip-flops.	2.Requires a recharge every few milliseconds to maintain its data.	2.Holds its contents as long as power is available.	3.Inexpensive.	3.Expensive.	4. Slower than SRAM.	4. Faster than DRAM.	5. Can store many bits per chip.	5. Can not store many bits per chip.	6. Uses less power.	6.Uses more power.	7.Generates less heat.	7.Generates more heat.	8. Used for main memory.	8. Used for cache.
DRAM	SRAM																		
1. Constructed of tiny capacitors that leak electricity.	1.Constructed of circuits similar to D flip-flops.																		
2.Requires a recharge every few milliseconds to maintain its data.	2.Holds its contents as long as power is available.																		
3.Inexpensive.	3.Expensive.																		
4. Slower than SRAM.	4. Faster than DRAM.																		
5. Can store many bits per chip.	5. Can not store many bits per chip.																		
6. Uses less power.	6.Uses more power.																		
7.Generates less heat.	7.Generates more heat.																		
8. Used for main memory.	8. Used for cache.																		
<p>18</p>	<p>Explain PLA.,PAL and PROM (BTL 1)</p>  <p>(a) Programmable read-only memory (PROM)</p> <p>(b) Programmable array logic (PAL) device</p> <p>(c) Programmable logic array (PLA) device</p>																		
<p>19</p>	<p>Draw the structure of a static RAM cell. [April/May-2014](BTL 6)</p>																		

																													
<p>20</p>	<p>List the Characteristics of Digital IC (BTL 1)</p> <p>Characteristics of Digital IC</p> <ul style="list-style-type: none"> ➤ Propagation Delay ➤ Power dissipation ➤ Fan-in ➤ Fan-out ➤ Noise Margin ➤ Operating temperatures ➤ Speed Power Product 																												
<p>21</p>	<p>Define TTL(BTL 1) Transistor-Transistor Logic (TTL) The TTL is so named because of its independence on transistors alone to perform basic logic operations. The TTL uses transistors operating in saturated mode. It is the fastest of saturated logic families. The basic TTL logic circuit is the NAND gate. Good speed, low manufacturing cost, wide range of circuits and the availability in SSI and MSI are its advantages. Tight VCC tolerance, relatively high power consumption, moderate packing density, generation of noise spikes and susceptibility to power transients are its disadvantages.</p>																												
<p>22</p>	<p>Compare TTL,CMOS and ECL with characteristics(BTL 4)</p> <table border="1" data-bbox="235 1207 1485 1470"> <thead> <tr> <th>Logic Family</th> <th>Propagation delay time (ns)</th> <th>Power dissipation per gate (mW)</th> <th>Noise Margin (V)</th> <th>Fan-in</th> <th>Fan-out</th> <th>Cost</th> </tr> </thead> <tbody> <tr> <td>TTL</td> <td>9</td> <td>10</td> <td>0.4</td> <td>8</td> <td>10</td> <td>Low</td> </tr> <tr> <td>CMOS</td> <td><50</td> <td>0.01</td> <td>5</td> <td>10</td> <td>50</td> <td>Low</td> </tr> <tr> <td>ECL</td> <td>1</td> <td>50</td> <td>0.25</td> <td>5</td> <td>10</td> <td>High</td> </tr> </tbody> </table>	Logic Family	Propagation delay time (ns)	Power dissipation per gate (mW)	Noise Margin (V)	Fan-in	Fan-out	Cost	TTL	9	10	0.4	8	10	Low	CMOS	<50	0.01	5	10	50	Low	ECL	1	50	0.25	5	10	High
Logic Family	Propagation delay time (ns)	Power dissipation per gate (mW)	Noise Margin (V)	Fan-in	Fan-out	Cost																							
TTL	9	10	0.4	8	10	Low																							
CMOS	<50	0.01	5	10	50	Low																							
ECL	1	50	0.25	5	10	High																							
<p>23</p>	<p>Define Emitter-Coupled Logic (ECL)(BTL 1) This logic family is also called Current Mode Logic or Current Steering Logic. It is the fastest of all logic families. ECL operates on the principle of current switching, whereby a fixed bias current less than IC switched from one transistor's collector to another. Because of this mode operation, this logic form is also referred to as Current Mode Logic (CML). It is also called Current Steering Logic (CSL), because current is steered from one device to another. The ECL family is used in very high frequency applications where its speed is superior.</p>																												
<p>24</p>	<p>Compare TTL,CMOS and ECL(BTL 4)</p> <table border="1" data-bbox="235 1743 1112 1816"> <thead> <tr> <th>Characteristic</th> <th>TTL</th> <th>CMOS</th> <th>ECL</th> </tr> </thead> <tbody> <tr> <td>Power Input</td> <td>Moderate</td> <td>Low</td> <td>Moderate-High</td> </tr> </tbody> </table>	Characteristic	TTL	CMOS	ECL	Power Input	Moderate	Low	Moderate-High																				
Characteristic	TTL	CMOS	ECL																										
Power Input	Moderate	Low	Moderate-High																										

	Frequency limit	High	Moderate	Very high
	Circuit density	Moderate-high	High-very high	Moderate
	Circuit types per family	High	High	Moderate

25 **Draw CMOS NAND Gate(BTL 6)**

26 **Draw an active-high tri-state buffer and write its truth table. [April/May-2010](BTL 6)**

Enable	Input	Output
0	X	Z
1	0	0
1	1	1

27 **What is a totem pole output? [April/May-2011](BTL 1)**
 Totem pole output is a standard output of a TTL gate. It is specifically designed to reduce the propagation delay in the circuit and to provide sufficient output power for high fan-out.

28 **Draw the TTL Inverter (NOT) Circuit. [April/May-2012](BTL 6)**

PART B

1 **Give the classification of semiconductor memories. (7m) BTL – 2**
Title: Digital Electronics
Author: D.Edwin Dhas

	<p>The IC gates and other circuits are temperature sensitive being semiconductor devices. However they are designed to operate satisfactorily over a specified range of temperatures. The range specified for commercial applications is 0 to 70°C, for industrial it is 0 to 85°C and for military applications it is -55°C to 125°C.</p> <p>Speed Power Product(2M) A common means for measuring and comparing the overall performance of an IC family is the speed power product which is obtained by multiplying the gate propagation delay by the gate power dissipation. The smaller the product, the better the overall performance.</p>
4.	<p>Determine the single error – correcting codes for the information code 10111 for odd parity. (7m) BTL – 2. Key Points Number of parity bits (2M) Construct a bit location table(2M) Determine the parity bits (3M)</p>
5.	<p>Assume that the even hamming code in example (0110011) is transmitted and that 0100011 is received. The receiver does not know what was transmitted. Determine bit location where error has occurred using received code. (7m) BTL - 4 Key Points Number of parity bits(2M) Construct a bit location table(3M) Determine the parity bits(2M)</p>
6.	<p>Define ROM Cell. Describe in detail about the types of ROM. (8m) BTL – 2 Title: Digital Electronics Author: D.Edwin Dhas Page No:5.1-5.6 Key Points Masked ROM (2M) PROM(2M) EPROM(2M) EEPROM(2M)</p>
7.	<p>Using ROM realize the following expressions. (7m) BTL – 4 $F_1(a, b, c) = \sum m(0, 1, 3, 5, 7) F_2 = \sum m(1, 2, 5, 6)$ Title: Digital Electronics Author: D.Edwin Dhas Page No:5.43-5.44 Key Points Block Diagram (3M) ROM truth Table (2M) Logic Diagram(2M)</p>
8.	<p>Design a combinational circuit using ROM. The circuit accepts 3 – bit number and generates an output binary number equal to square of input number. (7m) BTL - 4 Title: Digital Electronics Author: D.Edwin Dhas Page No:5.44-5.45 Key Points Block Diagram (3M) ROM truth Table (2M) Logic Diagram(2M)</p>
9.	<p>Designing a switching circuit that converts a 4 – bit binary code into a 4 – bit gray code using ROM array. (7m)(BTL - 4) Key Points ROM truth Table – (3m) Implementation – (4m)</p>

10	<p>A combinational circuit is defined by the functions:</p> $F_1 = \sum m(3, 5, 7)$ $F_2 = \sum m(4, 5, 7)$ <p>Implement the circuit with a PLA having 3 inputs, 3 product terms and two outputs. (BTL - 4) (7m)</p> <p>Title: Digital Electronics Author: D.Edwin Dhas Page No:5.20-5.21</p> <p>Key Points Simplify the Boolean functions using K – Map – (2m) Write PLA Program table – (2m) Implementation – (3m)</p>
11	<p>Draw a PLA circuit to implement the logic functions (BTL - 3) (7m)</p> <p>$A'BC+AB'C+AC'$ and $A'B'C'+BC$</p> <p>Key Points Simplify the Boolean functions using K – Map – (3m) Implementation – (4m)</p>
12	<p>Implement the following multiboolean function using 3*4*2 PLA PLD. (BTL - 3) (7m)</p> $f_1(a_2, a_1, a_0) = \sum m(0, 1, 3, 5) \text{ and } f_2(a_2, a_1, a_0) = \sum m(3, 5, 7)$ <p>Title: Digital Electronics Author: D.Edwin Dhas Page No:5.26-5.27</p> <p>Key Points Simplify the Boolean functions using K – Map – (3m) Implementation – (4m)</p>
13	<p>Design a BCD to Excess – 3 code converter and implement using suitable PLA. (BTL - 4) (13m)</p> <p>Title: Digital Electronics Author: D.Edwin Dhas Page No:5.30-5.32</p> <p>Key Points Truth table of BCD to Excess – 3 Converter – (3m) Simplify the Boolean functions using K – Map – (3m) Write PLA Programmable Table – (3m) Implementation – (4m)</p>
14	<p>Design and implement 3 – bit binary to gray code converter using PLA. (BTL - 4) (13m)</p> <p>Title: Digital Electronics Author: D.Edwin Dhas Page No:5.51</p> <p>Key Points Truth table of BCD to Excess – 3 Converter – (4m) Simplify the Boolean functions using K – Map – (4m) Implementation – (5m)</p>
15	<p>A combinational circuit is defined by the functions</p> $F_1(A, B, C) = \sum(3, 5, 6, 7)$ $F_2(A, B, C) = \sum(0, 2, 4, 7)$ <p>Implement the circuit with a PLA having three inputs, four product terms and two outputs. (BTL - 4) (13m)</p> <p>Title: Digital Electronics Author: D.Edwin Dhas Page No:5.45-5.49</p> <p>Key Points Simplify the Boolean functions using K – Map – (6m) Implementation – (7m)</p>
16	<p>Implement the Boolean function with a PLA. (BTL - 4) (13m)</p>

	$F_1(A, B, C) = \sum(0, 1, 2, 4)$ $F_2(A, B, C) = \sum(0, 5, 6, 7)$ $F_3(A, B, C) = \sum(0, 3, 5, 7)$ <p>Title: Digital Electronics Author: D.Edwin Dhas Page No:5.43-5.44 Key Points Simplify the Boolean functions using K – Map – (7m) Implementation – (6m)</p>
17	<p>Implement the switching functions: (BTL - 4) (7m) $Z_1 = ab'd'e + a'b'c'd'e' + bc + de$ $Z_2 = a'c'e$ $Z_3 = bc + de + c'd'e' + bd$ $Z_4 = a'c'e + ce$ Using a 5*8*4 PLA Title: Digital Electronics Author: D.Edwin Dhas Page No:5.45-5.49 Key Points Implementation – (7m)</p>
	PART C
1	<p>Write short notes on FPGA.(BTL - 1) (15m) Title: Digital Electronics Author: D.Edwin Dhas Page No:5.51-5.54 Key Points Basic Architecture of FPGA – (4m) An LUT programmed to produce the SOP function – (3m) Basic block in an FPGA – (4m) A simplified typical FPGA logic element – (4m)</p>
2	<p>Generate the following Boolean functions with a PAL with 4 inputs and 4 outputs (BTL – 4) (15m) $Y_3 = A'BC'D' + A'BCD' + ABC'D$ $Y_2 = A'BCD' + A'BCD + ABCD$ $Y_1 = A'BC' + A'BC + AB'C + ABC'$ $Y_0 = ABCD$</p> <p>Title: Digital Electronics Author: D.Edwin Dhas Page No:5.40-5.43 Key Points Simplify the Boolean functions using K – Map –(6m) Implementation – (7m)</p>
3.	<p>Generate the following Boolean functions with a PAL with 4 inputs and 4 outputs (BTL – 4) (15m) $Y_3 = A'BC'D' + A'BCD' + ABC'D$ $Y_2 = A'BCD' + A'BCD + ABCD$ $Y_1 = A'BC' + A'BC + AB'C + ABC'$ $Y_0 = ABCD$</p> <p>Title: Digital Electronics Author: D.Edwin Dhas Page No:5.40-5.43 Key Points Simplify the Boolean functions using K – Map – (6m)</p>

	Implementation – (7m)
	Implement the following Boolean functions using PLA. (15m) (BTL - 4) (Nov – Dec 2015) $w(A, B, C, D) = \sum m(0, 2, 6, 7, 8, 9, 12, 13)$ $x(A, B, C, D) = \sum m(0, 2, 6, 7, 8, 9, 12, 13, 14)$ $y(A, B, C, D) = \sum m(2, 3, 8, 9, 10, 12, 13)$ $z(A, B, C, D) = \sum m(1, 3, 4, 6, 9, 12, 14)$ Key Points Simplify the Boolean functions using K – Map – (4m) Array Logic for PAL – (4m) PAL Program table – (4m) Implementation – (3m)

EC8391

CONTROL SYSTEMS ENGINEERING**L T P C**
3 0 0 3**OBJECTIVES:**

- To introduce the components and their representation of control systems
- To learn various methods for analyzing the time response, frequency response and stability of the systems.
- To learn the various approach for the state variable analysis.

SYLLABUS:**UNIT I SYSTEMS COMPONENTS AND THEIR REPRESENTATION 9**

Control System: Terminology and Basic Structure-Feed forward and Feedback control theory, Electrical and Mechanical Transfer Function Models-Block diagram Models-Signal flow graphs models-DC and AC servo Systems-Synchronous -Multivariable control system

UNIT II TIME RESPONSE ANALYSIS 9

Transient response-steady state response-Measures of performance of the standard first order and second order system-effect on an additional zero and an additional pole-steady error constant and system- type number-PID control-Analytical design for PD, PI, PID control systems

UNIT III FREQUENCY RESPONSE AND SYSTEM ANALYSIS 9

Closed loop frequency response-Performance specification in frequency domain-Frequency response of standard second order system- Bode Plot - Polar Plot- Nyquist plots-Design of compensators using Bode plots-Cascade lead compensation-Cascade lag compensation-Cascade lag-lead compensation

UNIT IV CONCEPTS OF STABILITY ANALYSIS 9

Concept of stability-Bounded - Input Bounded - Output stability-Routh stability criterion-Relative stability-Root locus concept-Guidelines for sketching root locus-Nyquist stability criterion.

UNIT V CONTROL SYSTEM ANALYSIS USING STATE VARIABLE METHODS 9

State variable representation-Conversion of state variable models to transfer functions-Conversion of transfer functions to state variable models-Solution of state equations-Concepts of Controllability and Observability-Stability of linear systems-Equivalence between transfer function and state variable representations-State variable analysis of digital control system-Digital control design using state feedback.

TOTAL: 45 PERIODS**OUTCOMES:**

Upon completion of the course, the student should be able to:

- Identify the various control system components and their representations.
- Analyze the various time domain parameters.
- Analysis the various frequency response plots and its system.
- Apply the concepts of various system stability criterions.
- Design various transfer functions of digital control system using state variable models.

TEXT BOOK:

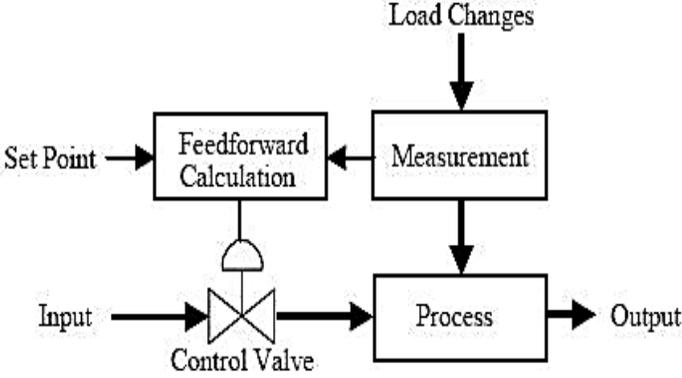
- M.Gopal, —Control System – Principles and Design, Tata McGraw Hill, 4th Edition, 2012.

REFERENCES:

- J.Nagrath and M.Gopal, —Control System Engineering, New Age International Publishers, 5th Edition, 2007.
- K. Ogata, ‘_Modern Control Engineering’, 5th edition, PHI, 2012.
- S.K.Bhattacharya, Control System Engineering, 3rd Edition, Pearson, 2013.
- Benjamin.C.Kuo, —Automatic control systems, Prentice Hall of India, 7th Edition, 1995.

	Subject Code: EC8391 Subject Name: Control Systems Engineering	Year/Semester: II/03 Subject Handler: Mrs. T.Muthukumari
	UNIT I - SYSTEMS COMPONENTS AND THEIR REPRESENTATION	
	Control System: Terminology and Basic Structure-Feed forward and Feedback control theory, Electrical, and Mechanical Transfer Function Models-Block diagram Models-Signal flow graphs models-DC and AC servo Systems-Synchronous -Multivariable control system.	
	PART * A	
Q.No	Questions	
1.	What is a system? BTL1 When a group of elements or components is connected in sequence to perform a specific function, the group thus formed is called a system.	
2.	What is a control system? (Nov Dec 2016) BTL1 A system consists of number of components connected together to perform a specific function. In a system when the output quantity is controlled by varying the input quantity then the system is called control system. The output quantity is called controlled variable Or response and the input quantity is called command signal or excitation. Examples: Control of temperature, liquid level, velocity. Transportation systems, power systems, robotics etc.	
3.	What are the different classifications of control system? BTL4 <ul style="list-style-type: none"> • Open loop control system • Closed loop control system 	
4.	What are the classifications of electrical system? BTL4 <ul style="list-style-type: none"> • Linear and Nonlinear system • Time invariant and Time variant system • Continuous time and Discrete time system • SISO and MIMO system • Lumped and Distributed parameter system • Deterministic and Stochastic system • Static and Dynamic system 	
5.	What are the components of control system? BTL4 The components of control system are plant, feedback path elements, error detector, and controller.	
6.	Define open loop and closed loop control system. BTL1 The control systems in which the output quantity has no effect upon the input quantity are called open loop control system. This means that the output is not feedback to the input for correction. The control systems in which the output quantity has an effect upon the input quantity in order to maintain the desired output value are called closed loop control system.	
7.	Give practical example of open loop systems. BTL3 The practical examples of open loop control systems are, sprinkler used to water a lawn,	

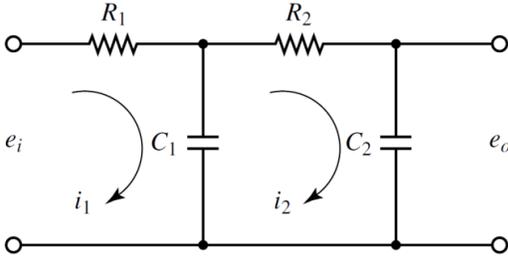
	automatic toaster, traffic light controller, automatic door opening and closing system.															
8.	<p>Give practical example of closed loop systems. BTL3</p> <p>The practical examples of closed loop control systems are, human being, home heating system, speed control systems, ship stabilization system, missile launching system, voltage stabilizer, temperature control systems.</p>															
9.	<p>List the advantages of closed loop system. BTL4</p> <ul style="list-style-type: none"> • Closed loop systems are accurate and reliable. • Changes in output due to external disturbances are corrected automatically. 															
10.	<p>List the advantages of open loop system(Nov/Dec 2015) BTL4</p> <ul style="list-style-type: none"> • The open loop system are simple and economical • The open loop system are easier to construct • Generally the open loop systems are stable 															
11.	<p>Differentiate open loop and closed loop System.(April May 2016),(Nov Dec 2017) BTL4</p> <table border="1"> <thead> <tr> <th>SL no</th> <th>Open loop</th> <th>Closed loop</th> </tr> </thead> <tbody> <tr> <td>1</td> <td>In accurate and unreliable</td> <td>Accurate and reliable</td> </tr> <tr> <td>2</td> <td>Simple and economical</td> <td>Complex and costly</td> </tr> <tr> <td>3</td> <td>Changes in output due to external disturbances are not corrected automatically</td> <td>Changes in output due to external disturbances are corrected automatically</td> </tr> <tr> <td>4</td> <td>They are generally stable</td> <td>Great efforts are needed to design a stable system</td> </tr> </tbody> </table>	SL no	Open loop	Closed loop	1	In accurate and unreliable	Accurate and reliable	2	Simple and economical	Complex and costly	3	Changes in output due to external disturbances are not corrected automatically	Changes in output due to external disturbances are corrected automatically	4	They are generally stable	Great efforts are needed to design a stable system
SL no	Open loop	Closed loop														
1	In accurate and unreliable	Accurate and reliable														
2	Simple and economical	Complex and costly														
3	Changes in output due to external disturbances are not corrected automatically	Changes in output due to external disturbances are corrected automatically														
4	They are generally stable	Great efforts are needed to design a stable system														
12.	<p>What is feedback control system?(April May 2018) BTL1</p> <ul style="list-style-type: none"> • Measure the controlled variable to determine the control strategy • The output of the plant/process is measured with the help of sensor and then given to the controller to take the proper action. • The controller compares the sensor signal with the reference signal and generate the actuating or control signal. • Controller action will be zero until the process variable meets set point. 															
13.	<p>Draw the model for feedback control system. BTL6</p>															
14.	<p>What are the characteristics of negative feedback? BTL2</p> <p>The characteristics of negative feedback are as follows</p> <ul style="list-style-type: none"> • Accuracy in tracking steady state value. • Rejection of disturbance signals. • Low sensitivity to parameter variations. • Reduction in gain at the expense of better stability. 															

15.	<p>What is effect of positive feedback on stability? BTL4</p> <p>The positive feedback increases the error signal and drives the output to instability. The positive feedback is used in minor loops in control systems to amplify certain internal signals or parameters.</p>
16.	<p>Why negative feedback is preferred in control system? BTL4</p> <p>The negative feedback results in better stability in steady state and rejects any disturbance signals. It also has low sensitivity to parameter variations. Hence negative feedback is preferred in closed loop control system.</p>
17.	<p>What is feedforward control system? BTL1</p> <ul style="list-style-type: none"> • Measures disturbance variable to determine the control strategy. • FFC avoids the slowness of the feedback controller • In FFC, a sensor is used to detect process load changes or disturbances as they enter the system. • Sensors measure the values of the load variables, and a computer calculates the correct control signal for the existing load conditions and process set point. • Here set point is fixed in the feed forward controller.
18.	<p>Draw the model for feedforward control system. BTL6</p> 
19.	<p>What is a mathematical model? What are its different types? BTL1</p> <p>A mathematical model consists of a collection of equations describing behaviour of the system. There are two types of mathematical modelling</p> <ul style="list-style-type: none"> • Input /output representations describing relations between the input and output of the system • State model describing the relations between the input ,state variable and output of the system
20.	<p>What is the need to study mathematical modelling of a system? BTL2</p> <p>A control system is a collection of components to meet a required objective. In order to meet the objective, it is very useful to have a mathematical modeling of the system.</p>
21.	<p>Define transfer function of the system.(Nov Dec 2017) BTL1</p> <p>The transfer function of a system is defined as the ratio between Laplace transform of the output and Laplace transform of the input when taking initial condition as zero</p> $TF = \frac{C(S)}{R(S)}$

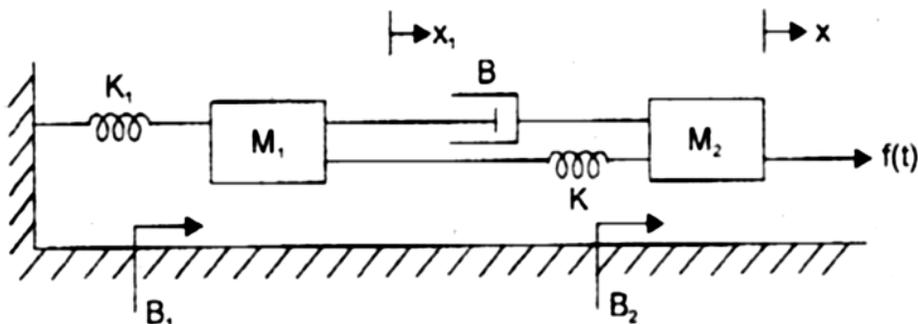
22.	<p>What are the basic elements used for modelling of electrical system? BTL2</p> <ul style="list-style-type: none"> • Resistor (R) • Inductor (L) • Capacitor(C)
23.	<p>State whether transfer function technique is applicable to nonlinear system and whether the transfer function is independent of the input of the system. BTL1</p> <ul style="list-style-type: none"> • The transfer function technique is not applicable to nonlinear system • The transfer function of a system is independent of input and depends only on system parameters but the output of a system depends on input.
24.	<p>What are the basic elements used for modelling of mechanical translational system?(Nov Dec 2016) BTL2</p> <ul style="list-style-type: none"> • Mass(M) • Spring (K) • Dashpot(B)
25.	<p>Write the force balance equation of an ideal mass, dashpot, spring element of an mechanical translational system. BTL1</p> <p>a. $F = M \frac{d^2x}{dt^2}$ for mass element. b. $F = B \frac{dx}{dt}$ for dashpot element. c. $F = kx$ for spring element.</p>
26.	<p>What are the basic elements used for modelling of mechanical rotational system? BTL2</p> <ul style="list-style-type: none"> • Mass with moment of inertia J • Dashpot with rotational friction coefficient B • Torsional spring with stiffness K
27.	<p>Write the torque balance equation of an ideal mass,dashpot and spring element of mechanical rotational system. BTL1</p> <ul style="list-style-type: none"> • $F = M \frac{d^2\theta}{dt^2}$ for mass element. • $F = B \frac{d\theta}{dt}$ for dashpot element. • $F = k\theta$ for spring element.
28.	<p>Name the two types of electrical analogous for mechanical translational system. BTL1</p> <ul style="list-style-type: none"> • Force voltage analogy • Force current analogy
29.	<p>Write the analogous electrical elements in force voltage analogy for the elements of mechanical translational system. BTL1</p> <p>a. Force-voltage e. b. Velocity v-current i. c. Displacement x-charge q. d. Frictional coefficient B-Resistance R. e. Mass M- Inductance L. f. Stiffness K-Inverse of capacitance $1/C$.</p>
30.	<p>Write the analogous electrical elements in force current analogy for the elements of mechanical translational system. BTL1</p> <p>a. Force-current I. b. Velocity v-voltage v.</p>

	<p>c. Displacement x-flux ϕ.</p> <p>d. Frictional coefficient B-conductance $1/R$.</p> <p>e. Mass M- capacitance C.</p> <p>f. Stiffness K-Inverse of inductance $1/L$.</p>
31.	<p>What is Block diagram? What are its basic components? (Nov/Dec 2015) BTL1</p> <p>A block diagram of a system is a pictorial representation of the functions performed by each components of the system and shows the flow of signals. The basic elements of the block diagram are blocks, branch points, and summing points.</p>
32.	<p>What is the basis for framing rules of block diagram reduction technique? BTL1</p> <p>The rules for block diagram reduction technique are framed such that any modification made on the diagram does not alter the input and output relations.</p>
33.	<p>What are the basic components of block diagram representations? BTL2</p> <ul style="list-style-type: none"> • Block • Branch point • Summing point
34.	<p>Write the rule for elimination of negative feedback. BTL1</p>
35.	<p>What are the disadvantages of block diagram representation? BTL2</p> <ul style="list-style-type: none"> • It is a tedious method of calculating transfer function. • Overall gain of the system cannot be computed.
36.	<p>What is a signal flow graph? BTL1</p> <p>A signal flow graph is a diagram that represents a set of simultaneous linear algebraic equations. By taking Laplace, transform the time domain differential equations governing s a control system can be transferred to a set of algebraic equations in s domain. The signal flow graph of the system can be constructed using these equations,</p>
37.	<p>What are the properties of signal flow graph? BTL2</p> <p>The basic properties of signal flow graph are</p> <ul style="list-style-type: none"> • Signal flow graph is applicable to linear systems. • It consists of nodes and branches. A node is a point representing a variable or signal. A branch indicates functional dependence of one signal to other. • A node adds the signals of all incoming branches and transmits this sum to all other branches. • Signals travel along branches only in the marked direction and when it travels it gets multiplied by the gain or transmittance of the branch. • The algebraic equations must be in the form of cause and effect relationship.
38.	<p>State Mason's Gain formula. (April/May 2010) BTL1</p> $\text{Overall gain, } T = \frac{1}{\Delta} \sum_K P_K \Delta_K$

	<p>Where P_k = Forward path gain of Kth forward path K = Number of forward paths in the signal flow graph $\Delta = 1 - (\text{sum of individual loop gains}) + (\text{Sum of gain products of all possible combinations of two non-touching loop}) - (\text{sum of gain products of all possible combination of three non-touching loops}) + \dots$ $\Delta_k = \Delta$ for that part of the graph which is not touching the Kth forward path.</p>																					
39.	<p>What is called servo motor? BTL1</p> <ul style="list-style-type: none"> The motors that are used in automatic control systems are called servomotors. The motors are used for feedback control system are called servomotor It converts electrical signal into angular displacement of the shaft. 																					
40.	<p>What are the features of servomotors? BTL4</p> <ul style="list-style-type: none"> Linear relationship between the speed and electric control signal Steady state stability Wide range of speed control Linearity of mechanical characteristic throughout the entire speed range Low mechanical and electrical inertia Fast response. 																					
41.	<p>What are the classifications of servomotors? BTL2 Depending on the supply required to run the motor, they are broadly classified as</p> <ul style="list-style-type: none"> DC servo motors AC servo motors 																					
42.	<p>What are the applications of DC and AC servomotors? BTL3</p> <ul style="list-style-type: none"> The DC servomotors are generally used for large power applications such as in machine tools and robotics The AC servomotors are best suited for low power applications such as X-Y recorders, Disk drives, tape drivers, printers etc. 																					
43.	<p>Compare AC and DC servo motor BTL2</p> <table border="1"> <thead> <tr> <th>Sl.No</th> <th>DC SERVO MOTOR</th> <th>AC SERVO MOTOR</th> </tr> </thead> <tbody> <tr> <td>1</td> <td>For small size, they deliver high output</td> <td>They are designed for low power output</td> </tr> <tr> <td>2</td> <td>Amplifier is used for DC motor has a drift</td> <td>Amplifier have no drift</td> </tr> <tr> <td>3</td> <td>More efficient</td> <td>Efficiency is less as rotor resistance is large</td> </tr> <tr> <td>4</td> <td>More maintenance is required</td> <td>Less maintenance</td> </tr> <tr> <td>5</td> <td>No slip rings. Hence slip losses are zero</td> <td>Slip losses are not zero</td> </tr> <tr> <td>6</td> <td>Brushes produces radio frequency interference</td> <td>No radio frequency noise</td> </tr> </tbody> </table>	Sl.No	DC SERVO MOTOR	AC SERVO MOTOR	1	For small size, they deliver high output	They are designed for low power output	2	Amplifier is used for DC motor has a drift	Amplifier have no drift	3	More efficient	Efficiency is less as rotor resistance is large	4	More maintenance is required	Less maintenance	5	No slip rings. Hence slip losses are zero	Slip losses are not zero	6	Brushes produces radio frequency interference	No radio frequency noise
Sl.No	DC SERVO MOTOR	AC SERVO MOTOR																				
1	For small size, they deliver high output	They are designed for low power output																				
2	Amplifier is used for DC motor has a drift	Amplifier have no drift																				
3	More efficient	Efficiency is less as rotor resistance is large																				
4	More maintenance is required	Less maintenance																				
5	No slip rings. Hence slip losses are zero	Slip losses are not zero																				
6	Brushes produces radio frequency interference	No radio frequency noise																				
44.	<p>What is a synchro? BTL1</p> <ul style="list-style-type: none"> Synchro's are the electromechanical devices or electromagnetic transducer which produces an output voltage depending upon the angular position of the rotor. It is formed by interconnection of the synchro transmitter and synchro control transformer. They are also called synchro pair. 																					

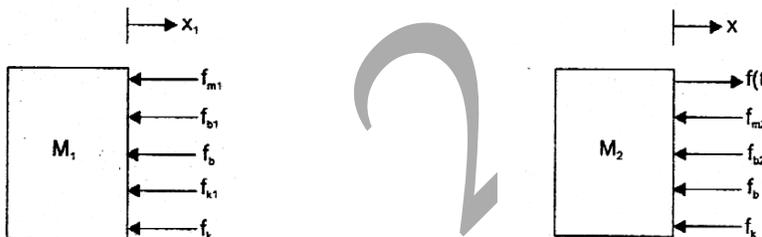
45.	<p>What are the uses of synchro's? BTL3 They can be used in the following two ways.</p> <ul style="list-style-type: none"> To control the angular position of load from a remote place / long distance. For automatic correction of changes due to disturbance in the angular position of the load.
46.	<p>What are the differences between synchro transmitter and synchro control transformer? BTL2</p> <ul style="list-style-type: none"> Rotor of synchro transmitter is of dumb bell shape and the rotor of control transformer is cylindrical. The rotor winding of synchro transmitter is excited by an AC voltage. In control transformer, the induced emf in the rotor is used as an output signal (error signal).
PART * B	
<p>Obtain the transfer function of the electrical network shown in figure.(13M) (April May 2018) BTL6</p> <div style="text-align: center;">  </div> <p>Answer: Page 1.23 to 1.24 -A.Nagoor Kani</p> <p>1. Apply KCL at node 1 (2M)</p> $\frac{v_1}{R_1} + C_1 \frac{dv_1}{dt} + \frac{v_1 - v_2}{R_2} = \frac{e}{R_1} \quad \text{-----(1)}$ <p>Take Laplace transform of the equation(1) (3M)</p> $V_1(s) \left[\frac{1}{R_1} + sC_1 + \frac{1}{R_2} \right] - \frac{V_2(s)}{R_2} = \frac{E(s)}{R_1}$ <p>Apply KCL at node 2 (2M)</p> $\frac{v_2 - v_1}{R_2} + C_2 \frac{dv_2}{dt} = 0 \quad \text{-----(2)}$ <p>Take Laplace transform of the equation(2) (3M)</p> $V_1(s) = [1 + sC_2R_2] V_2(s)$ <p>Substituting V₁(s) from equation(2) in equation(1) we get (3M)</p> $\frac{V_2(s)}{E(s)} = \frac{R_2}{[(1 + sR_2C_2)(R_1 + R_2 + sC_1R_1R_2) - R_1]}$	

Write the differential equation governing the mechanical system shown in fig and also determine the transfer function(13M)(April/May 2015) BTL6



Answer:Page 1.9 to 1.11- A.Nagoor Kani

- Draw the free body diagram for mass M1 and M2 (2M)



- Write the force balance equations for M1 and M2 (2M)

$$f_{m1} + f_{b1} + f_b + f_{k1} + f_k = 0 \qquad f_{m2} - f_{b2} + f_b + f_k = f(t)$$

- Write the differential equations (2M)
- Take Laplace transform (3M)

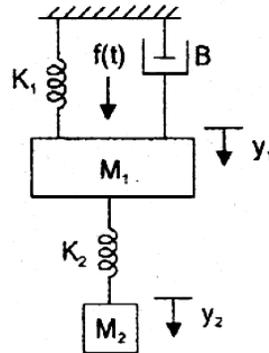
$$X_1(s) = X(s) \frac{Bs + K}{M_1s^2 + (B_1 + B)s + (K_1 + K)}$$

- Rearrange the equations and find the transfer equation (4M)

$$X(s) [M_2s^2 + (B_2 + B)s + K] - X(s) \frac{(Bs + K)^2}{M_1s^2 + (B_1 + B)s + (K_1 + K)} = F(s)$$

$$\frac{X(s)}{F(s)} = \frac{M_1s^2 + (B_1 + B)s + (K_1 + K)}{[M_1s^2 + (B_1 + B)s + (K_1 + K)] [M_2s^2 + (B_2 + B)s + K] - (Bs + K)^2}$$

Write the differential equation governing the mechanical system shown in fig and also determine the transfer function (13M) BTL6



Answer: Page 1.11 to 1.12 -A.Nagoor Kani

- Draw the free body diagram for mass M₁ and M₂ (2M)

3.



- Write the force balance equations for M₁ and M₂ (3M)
- Write the differential equations (2M)
- Take Laplace transform (3M)
- Rearrange the equations and find the transfer equation (3M)

$$f_{m2} + f_{k2} = 0$$

$$f_{m1} + f_b + f_{k1} + f_{k2} = f(t)$$

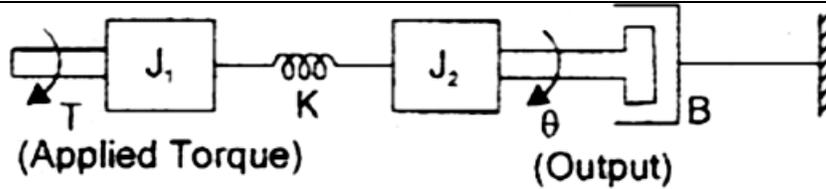
$$Y_1(s)[M_1s^2 + Bs + (K_1 + K_2)] - Y_2(s)K_2 = F(s)$$

$$Y_1(s) = Y_2(s) \frac{M_2s^2 + K_2}{K_2}$$

$$\frac{Y_2(s)}{F(s)} = \frac{K_2}{[M_1s^2 + Bs + (K_1 + K_2)] [M_2s^2 + K_2] - K_2^2}$$

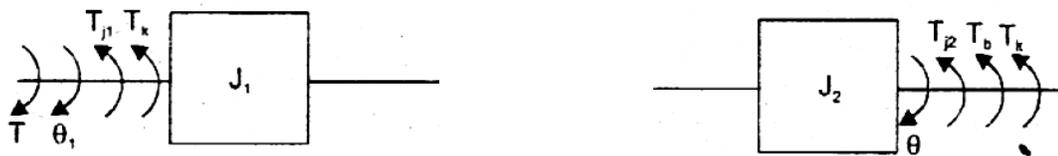
4.

Write the differential equations governing mechanical rotational system shown in figure and find the transfer function of the system (13M)BTL6



Answer: Page 1.19 to 1.20 - A.Nagoor Kani

- Draw the free body diagram (2M)



- Write the torque balance equations for M1 and M2 (3M)

$$T_{j1} + T_k = T$$

$$T_{j2} + T_b + T_k = 0$$

- Write the differential equations (2M)

$$J_1 \frac{d^2\theta_1}{dt^2} + K\theta_1 - K\theta = T$$

$$J_2 \frac{d^2\theta}{dt^2} + B \frac{d\theta}{dt} + K(\theta - \theta_1) = 0$$

- Take Laplace transform (3M)

- $(J_1 s^2 + K) \theta_1(s) - K \theta(s) = T(s)$

- $J_2 s^2 \theta(s) + B s \theta(s) + K \theta(s) - K \theta_1(s) = 0$

- Rearrange the equations and find the transfer equation (3M)

$$\therefore \frac{\theta(s)}{T(s)} = \frac{K}{(J_1 s^2 + K)(J_2 s^2 + B s + K) - K^2}$$

Write the differential equations governing the mechanical system shown in figure. Draw the force voltage and force current electrical analogous circuits and verify by writing mesh and node equations. (13M) (Nov Dec 2015) BTL6

5.

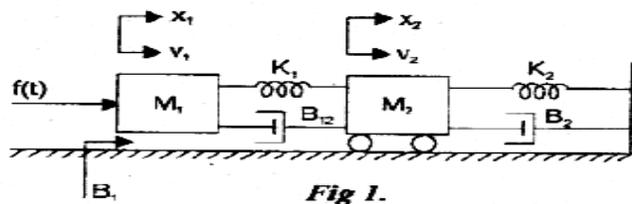
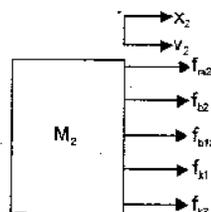
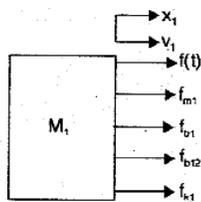


Fig 1.

Answer: Page 1.32 to 1.33 - A.Nagoor Kani

- Draw the free body diagram (1M)



- Write the force balance equations (1M)

$$f_{m1} + f_{b1} + f_{b12} + f_{k1} = f(t) \qquad f_{m2} + f_{b2} + f_{k2} + f_{b12} + f_{k1} = 0$$

- Write the differential equations (1M)

$$M_1 \frac{d^2 x_1}{dt^2} + B_1 \frac{dx_1}{dt} + B_{12} \frac{d}{dt} (x_1 - x_2) + K_1 (x_1 - x_2) = f(t)$$

- Replacing the Displacements by velocity in the differential equations (1M)

$$M_1 \frac{dv_1}{dt} + B_1 v_1 + B_{12} (v_1 - v_2) + K_1 \int (v_1 - v_2) dt = f(t)$$

- Write the differential equations (1M)

$$M_2 \frac{d^2 x_2}{dt^2} + B_2 \frac{dx_2}{dt} + K_2 x_2 + B_{12} \frac{d}{dt} (x_2 - x_1) + K_1 (x_2 - x_1) = 0$$

- Replacing the Displacements by velocity in the differential equations (2M)

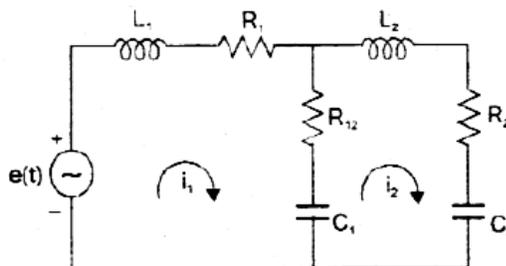
$$M_2 \frac{dv_2}{dt} + B_2 v_2 + K_2 \int v_2 dt + B_{12} (v_2 - v_1) + K_1 \int (v_2 - v_1) dt = 0$$

Force voltage analogy(3M)

$f(t) \rightarrow e(t)$	$M_1 \rightarrow L_1$	$B_1 \rightarrow R_1$	$K_1 \rightarrow 1/C_1$
$v_1 \rightarrow i_1$	$M_2 \rightarrow L_2$	$B_2 \rightarrow R_2$	$K_2 \rightarrow 1/C_2$
$v_2 \rightarrow i_2$		$B_{12} \rightarrow R_{12}$	

$$L_1 \frac{di_1}{dt} + R_1 i_1 + R_{12} (i_1 - i_2) + \frac{1}{C_1} \int (i_1 - i_2) dt = e(t)$$

$$L_2 \frac{di_2}{dt} + R_2 i_2 + \frac{1}{C_2} \int i_2 dt + R_{12} (i_2 - i_1) + \frac{1}{C_1} \int (i_2 - i_1) dt = 0$$

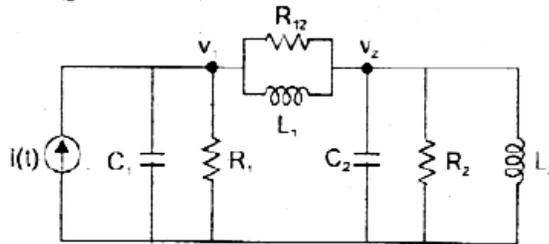


Force current analogy(3M)

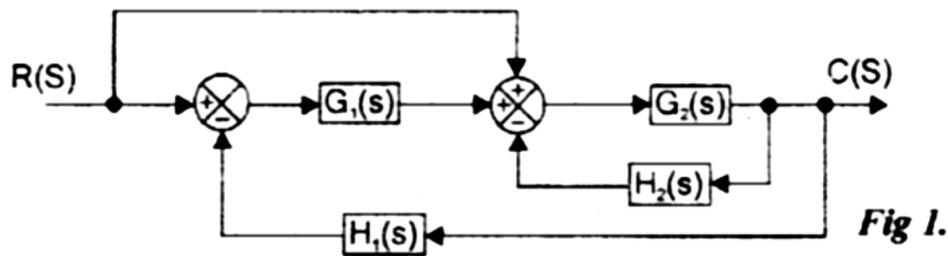
$$\begin{aligned} i(t) \rightarrow i(t) & \quad M_1 \rightarrow C_1 & \quad B_1 \rightarrow 1/R_1 & \quad K_1 \rightarrow 1/L_1 \\ v_1 \rightarrow v_1 & \quad M_2 \rightarrow C_2 & \quad B_2 \rightarrow 1/R_2 & \quad K_2 \rightarrow 1/L_2 \\ v_2 \rightarrow v_2 & \quad B_{12} \rightarrow 1/R_{12} & & \end{aligned}$$

$$C_1 \frac{dv_1}{dt} + \frac{1}{R_1} v_1 + \frac{1}{R_{12}} (v_1 - v_2) + \frac{1}{L_1} \int (v_1 - v_2) dt = i(t)$$

$$C_2 \frac{dv_2}{dt} + \frac{1}{R_2} v_2 + \frac{1}{L_2} \int v_2 dt - \frac{1}{R_{12}} (v_2 - v_1) + \frac{1}{L_1} \int (v_2 - v_1) dt = 0$$



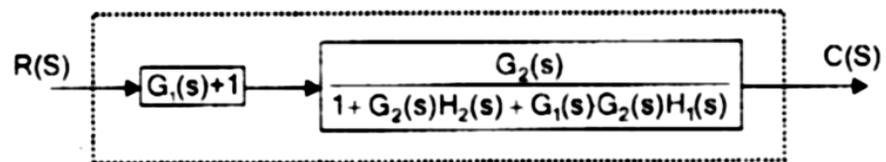
Using block diagram reduction technique find the closed loop transfer function of the system shown in figure.(13M) (April May 2018) BTL5



Answer: Page 1.76 to 1.77 - A.Nagoor Kani

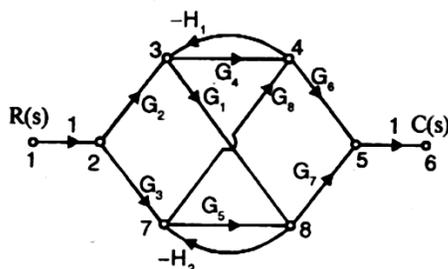
6.

- Step 1:Spilitting the summing point (1M)
- Step 2:Eliminating the feedback path (2M)
- Step 3:Moving the summing point after the block (2M)
- Step 4:Interchanging the summing point and combining the blocks in cascade (2M)
- Step 5:Eliminating the feedback path and feed forward path (1M)
- Step 6:Combining the blocks in cascade (2M)
- The transfer function of the system is given by



$$\frac{C(s)}{R(s)} = \frac{G_2(s) [G_1(s)+1]}{1+G_2(s) H_2(s)+G_1(s) G_2(s) H_1(s)} \quad (3M)$$

Find the overall gain of the system whose signal flow graph shown in figure.12M(Nov Dec 2015) BTL5 (13M)



Answer: Page 1.87 to 1.89 - A.Nagoor Kani

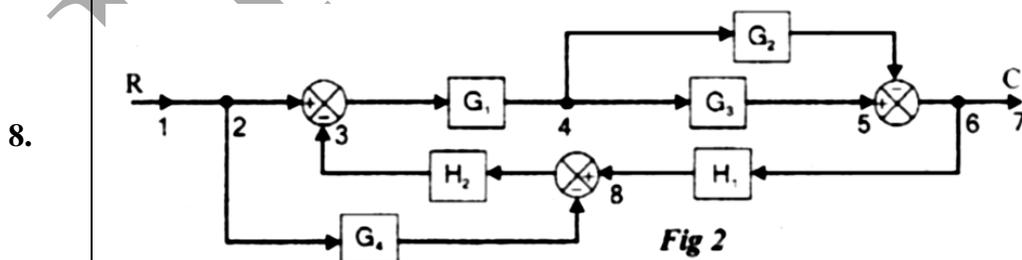
- 7. Step 1:Forward path Gains (2M)
- Step 2:Individual Loop gain (4M)
- Step 3:Gain products of two non-touching loops (4M)
- Step 4.Calculation of Δ and Δk (3M)

$$T = \frac{1}{\Delta} \left(\sum_K P_K \Delta_K \right) \quad (\text{Number of forward paths is six and so } K = 6)$$

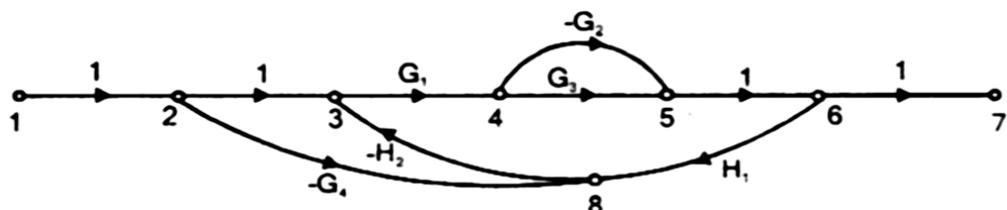
$$= \frac{1}{\Delta} (P_1\Delta_1 + P_2\Delta_2 + P_3\Delta_3 + P_4\Delta_4 + P_5\Delta_5 + P_6\Delta_6)$$

$$= \frac{G_2G_4G_6(1 + G_5H_2) + G_3G_5G_7(1 + G_4H_1) + G_1G_2G_7 + G_3G_6G_8 - G_1G_3G_7G_8H_1 - G_1G_2G_6G_8H_2}{1 + G_4H_1 + G_5H_2 - G_1G_8H_1H_2 + G_4G_5H_1H_2}$$

Draw a signal flow graph and evaluate the closed loop transfer function of a system whose block diagram is shown in figure.(13M) (April/May 2015) Repeated question BTL5



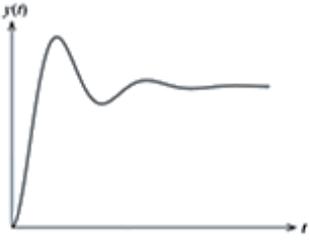
Answer: Page 1.99 to 1.101 - A.Nagoor Kani

	<ul style="list-style-type: none"> • Draw the signal flow graph for the given block diagram by assigning nodes. (3M)  <p>Step 1: Forward path gains (2M) Step 2: Individual loop gain (2M) Step 3: Gain products of Two Non-touching loops (2M) Step 4: Calculation of Δ and Δ_k (2M) Step 5: Transfer function: (2M)</p> $= \frac{G_1(G_3 - G_2) + G_1G_4H_2(G_3 - G_2)}{1 + G_1H_1H_2(G_3 - G_2)} = \frac{G_1(G_3 - G_2)(1 + G_4H_2)}{1 + G_1H_1H_2(G_3 - G_2)}$
<p>9.</p>	<p>Derive the transfer function of AC servomotor in control system.(13M)BTL6</p> <p>Answer: Page 2.29 - A.Nagoor Kani</p> <p>Definition of Servomotor :- (2M)</p> <ol style="list-style-type: none"> 1. Motor used for feedback control systems are called servomotors. It is also called automatic control system. 2. Converts electrical system into angular motion. 3. 2 types: DC servomotor and AC servomotor. <p>Definition of AC Servomotor :- (3M)</p> <ol style="list-style-type: none"> 1. Motor which runs at zero speed as its base speed is driven by error signal with AC supply is called servomotor. 2. Used in closed loop servo systems, high-speed instrument servos, and low power applications. 3. Speed control done using armature voltage control and field control. <p>Operating principle of AC Servomotor (4M) Salient features include rugged construction, Reliable in operation, Light Weight and No Slip rings.</p> <p>Transfer function derivation (4M) $\Theta(s)/V_c(s) = K_m/s(1+stm)$</p>
PART *C	
<p>1.</p>	<p>Summarize about the construction, principle and usage of synchro's in control systems (15M) BTL2</p> <p>Answer: Page 2.5 to 2.10 - A.Nagoor Kani</p> <p>Definition of synchro's (2M)</p> <ul style="list-style-type: none"> • Synchros are the electromechanical devices or electromagnetic transducer which

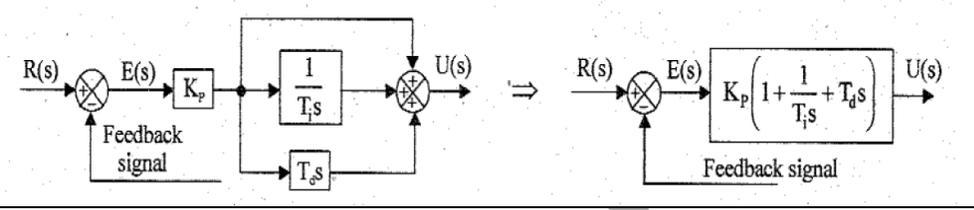
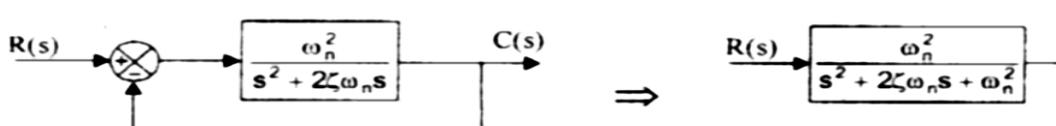
	<p>produces an output voltage depending upon the angular position of the rotor.</p> <ul style="list-style-type: none"> It is formed by interconnection of the synchro transmitter and synchro control transformer. They are also called synchro pair. <p>Explain about synchro transmitter(construction, working principle) (4M)</p> <ul style="list-style-type: none"> The constructional features of synchro control transformer are similar to that of synchro transmitter, except the shape of rotor. The rotor of the control transformer is made cylindrical so that the air gap is practically uniform. This feature of the control transformer minimizes the changes in the rotor impedance with the rotation of the shaft. <p>Explain about synchro control transformer(construction, working principle) (4M)</p> <p>Explain about synchro error detector (5M)</p>
<p>2.</p>	<p>Convert the given block diagram shown in fig. to signal flow graph and determine the closed loop transfer function C(s)/R(s) and verify by block diagram reduction approach. (15M)BTL6</p> <p>Answer: Page 1.95 to 1.97 - A.Nagoor Kani</p> <ul style="list-style-type: none"> Draw the signal flow graph. Give the numbering to input, output, summing point and branching point Find the transfer function using masons gain formula <p>Step 1:Forward path gains(2M)</p> <p>Step 2:Individual loop gain (2M)</p> <p>Step 3:Gain products of Two Non-touching loops (2M)</p> <p>Step 4:Calculation of Δ and Δ_k (2M)</p> <p>Step 5:Transfer function: (2M)</p> <ul style="list-style-type: none"> Apply block diagram reduction rules to find transfer function Find transfer function (5M) $T = \frac{G_1 G_2 G_3 + G_1 G_4}{1 + G_1 G_2 G_3 + G_1 G_2 H_1 + G_2 G_3 H_2 + G_1 G_4 + G_4 H_2}$
<p>3.</p>	<p>What are the basic elements of mechanical rotational and translational systems? Write its torque balance and force balance equations.(15M)(April/May 2015),(Nov Dec 2015) BTL1</p> <p>Answer: Page 1.7 to 1.9 and 1.17-1.19 - A.Nagoor Kani</p> <ul style="list-style-type: none"> Elements of mechanical system (2M)

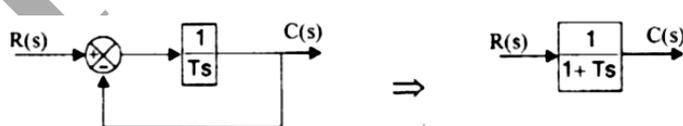
	<p>1. Mass(M), Dashpot(B), Spring(K) 2. Moment of inertia (J), Dashpot(F), Spring(K)</p> <ul style="list-style-type: none"> • Draw the free body diagram (2M) • Apply Newton's second law (1M) • Write differential equations (2M) <p style="text-align: center;">1. $F(t) = M \frac{d^2\theta}{dt^2} + B \frac{d\theta}{dt} + k\theta$ 2. $T(t) = M \frac{d^2\theta}{dt^2} + B \frac{d\theta}{dt} + k\theta$</p> <ul style="list-style-type: none"> • Force balance equation of translational system (4M) <p>$F = M \frac{d^2x}{dt^2}$ for mass element. $F = B \frac{dx}{dt}$ for dash pot element. $F = kx$ for spring element.</p> <ul style="list-style-type: none"> • Force balance equation of rotational system (4M) <p>1. Mechanical Rotational system can be obtained using three basic elements Moment of Inertia (J), Spring (K), Damper (B). 2. $F = M \frac{d^2\theta}{dt^2}$ for mass element. 3. $F = B \frac{d\theta}{dt}$ for dash pot element. 4. $F = k\theta$ for spring element.</p> <ul style="list-style-type: none"> • Torque-voltage rule: <p>1. Angular Velocity v-current i. 2. Angular Displacement x-charge q. 3. Frictional coefficient F-Resistance R. 4. Mass J- Inductance L. 5. Stiffness K-Inverse of capacitance $1/C$.</p> <ul style="list-style-type: none"> • Torque-current rule: <p>1. Angular Velocity v-voltage v. 2. Angular Displacement x-flux ϕ. 3. Frictional coefficient F conductance $1/R$. 4. Mass J- capacitance C.</p>
--	--

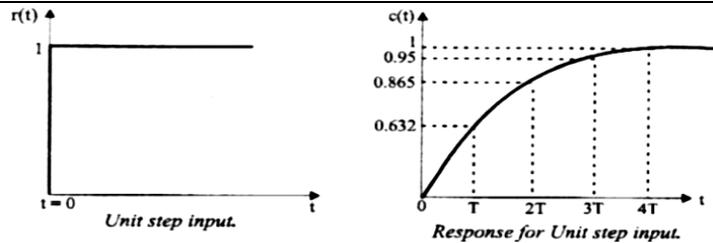
UNIT II – TIME RESPONSE ANALYSIS	
	Transient response-steady state response-Measures of performance of the standard first order and second order system-effect on an additional zero and an additional pole-steady error constant and system- type number-PID control-Analytical design for PD, PI,PID control systems
	PART * A
Q.No	Questions
1.	What is time response analysis?BTL1 The time response of the system is the output of the closed loop system as a function of time. It is denoted by C(t).The time response can be obtained by solving the differential equation governing the system.
2.	What is the need for time domain analysis? BTL2 Most of the control system use time as the independent variable, so it is important to analyze the response given by the system for the applied excitation, which is the function of the time.
3.	Define transient and steady state response BTL1 The transient response The response of the system when the input changes from one state to another Steady state response Response of the system when time t approaches infinity
4.	What are the standard tests signals employed for time domain studies?(April May 2015),(Nov/Dec 2015) repeated question BTL1 <ul style="list-style-type: none"> • Step signal, Unit step signal • Ramp signal, Unit ramp signal • Parabolic signal, Unit parabolic signal • Impulse signal • Sinusoidal signal
5.	Define damping ratio BTL1 The damping ratio is defined as the ratio of actual damping to the critical damping
6.	Define order of a system BTL 1 <ul style="list-style-type: none"> • Order of the differential equation governing the system. • If the system is governed by nth order differential equation then the system is called nth order system.
7.	Classify the system based on the value of damping? BTL2 Case(i):Undamped system $\delta=0$ Case(ii):Critically damped system $\delta=1$ Case(iii):Under damped system $0<\delta<1$ Case(iv):Over damped system $\delta>1$
8.	What will be the nature of the response of the second order system with different types of damping? BTL2

	<ul style="list-style-type: none"> • For undamped system the response is oscillatory • For under damped system the response is damped oscillatory • For critically damped system the response is exponential rising • For over damped system the response is exponentially rising but the rise time will be very large
9.	<p>Sketch the response of a second order under damped system? BTL3</p>  <p>($0 < \zeta < 1$) underdamped</p>
10.	<p>What is damped frequency of oscillation? BTL1 In underdamped system, the response is damped oscillatory. The frequency of damped oscillation is given by $\omega_d = \omega_n \sqrt{1 - \delta^2}$</p>
11.	<p>What is the effect of adding a pole to a second order system? BTL4 The second order system is generally stable. If a pole is added to it, it becomes third order due to which it becomes less stable in nature. It increases peak overshoot and settling time.</p>
12.	<p>What is type number of the system?(April/May 2015) BTL2 The type number is given by number of poles of loop transfer function at the origin. The type number of the system decides the steady state error.</p>
13.	<p>What is type 0 and type 1 system? BTL2 The value of N in the denominator polynomial of loop transfer function decides the type number of the system</p> <ul style="list-style-type: none"> • N- Number of poles at origin. • N = 0, then the system is type 0 system, • N = 1, the system is type 1 system. • N = 2, then the system is type 2 system and so on.
14.	<p>What is the difference between type and order of the system BTL2 Type number indicates the number of poles at the origin whereas the order of the system indicates the order of the differential equation governing the dynamics of the system.</p>
15.	<p>What are static error constants ? BTL1 The K_p, K_v, K_a are called static error constants.</p> <p>Positional error constant, $K_p = \lim_{s \rightarrow 0} G(s) H(s)$</p> <p>Velocity error constant, $K_v = \lim_{s \rightarrow 0} s G(s) H(s)$</p> <p>Acceleration error constant, $K_a = \lim_{s \rightarrow 0} s^2 G(s) H(s)$</p>
16.	<p>Outline the time domain specifications. (Nov Dec 2016) BTL2 The transient response characteristics of a control system to a unit step input is specified in terms of the following specifications</p>

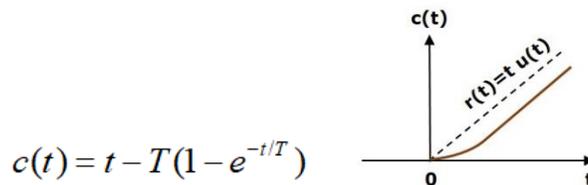
	<ul style="list-style-type: none"> • Delay time t_d • Rise time t_r • Peak time t_p • Maximum overshoot M_p • Settling time t_s
17.	<p>Draw the unit step response curve for the second order system and show the time domain specifications.(April May 2018) BTL3</p>
18.	<p>Write the definition for peak overshoot? BTL1 Maximum overshoot (M_p) is straight way difference between the magnitude of the highest peak of time response and magnitude of its steady state. Maximum overshoot is expressed in term of percentage of steady-state value of the response.</p>
19.	<p>Define peak time. BTL1 The time at which the peak overshoot occurs in the time response of a second order system is called a peak time.</p>
20.	<p>How would you define rise time? BTL 1 It is the time required for the response to rise from 10% to 90% of the final value for over damped systems and 0 to 100% of the final value for under damped systems. The rise time is reciprocal of the slope of the response at the instant, the response is equal to 50% of the final value.</p>
21.	<p>How can the maximum overshoot of a system be decreased without affecting the steady state error? BTL4 With the use of PD i.e. proportional plus derivative controller, it can be observed that transient response and value of damping ratio increases without affecting steady state error. As damping ratio increases, the maximum overshoot decreases. So, using PD controller it is possible to decrease maximum overshoot without affecting the steady state error.</p>
22.	<p>Define steady state error.(April May 2017),(Nov Dec 2015) repeated question BTL1 The steady state error is the value of error signal $e(t)$ when t tends to infinity. The steady state error is a measure of system accuracy. These errors arise from the nature of inputs, type of the system and from the non-linearity of the system components.</p>
23.	<p>What are generalized error coefficients?(April May 2018) (Nov Dec 2017) BTL1 They are coefficients of generalised error series. The generalised error series is given by</p> $e_{ss} = \lim_{t \rightarrow \infty} \left[r(t) C_0 + \dot{r}(t) C_1 + \ddot{r}(t) \frac{C_2}{2!} + \dots + \overset{n}{r}(t) \frac{C_n}{n!} + \dots \right]$
24.	<p>State the advantages of generalized error coefficients. BTL 2</p> <ul style="list-style-type: none"> • It gives variation of error as a function of time. • It uses any input other than the standard input.

	<ul style="list-style-type: none"> As variation of error as a function of time is available, the design of the system becomes easy and optimum
25.	<p>What is the function of controller? BTL1 A controller accepts error as its input, manipulates the error according to the requirement of the system, and gives output to the plant or the process to be controlled.</p>
26.	<p>What did you infer when a proportional controller is introduced in a system? BTL4 The following aspects of the system behavior are improved by increasing the loop gain</p> <ul style="list-style-type: none"> Steady state tracking accuracy Disturbance signal rejection Relative stability <p>The drawback of the P controller is, it produces the constant the steady state error.</p>
27.	<p>Draw the transfer function model for PID control (April May 2017) BTL6</p> 
28.	<p>Mention the characteristics of PI controller. (April May 2015) BTL2</p> <ul style="list-style-type: none"> The advantages of both P and I controller are combined in PI controller The proportional action increases the loop gain and makes the system less sensitive to variations of system parameter. The integral action eliminates or reduces the steady state error
29.	<p>Why derivative controller is not used in the control system? BTL2 The derivative controller acts only during transient period when the error varies with time and does not produce any corrective action for a constant error as derivative of a constant error is zero. Hence the derivative controller is never used alone but always used along with some other type of controller.</p>
30.	<p>What is the effect of PI controller on the system performance? BTL 2 The PI controller increases the order of the system by one, which results in reducing, the steady state error. But the system becomes less stable than the original system.</p>
PART * B	
Q.No	Questions
	<p>Draw the block diagram of second order system. Classify it. Derive the time response of any one of the damped system for unit step input. (13 M) (Nov/Dec2018) BTL6</p> <p>Answer: Page 3.9 to 3.16 - A.Nagoor Kani</p>
1.	<ul style="list-style-type: none"> Block diagram of second order system (3M)  <ul style="list-style-type: none"> Classification of second order system based on damping ratio (3M)

	<p>Case(i):Undamped system $\delta=0$ Case(ii):Critically damped system $\delta=1$ Case(iii):Under damped system $0<\delta<1$ Case(iv):Over damped system $\delta>1$</p> <ul style="list-style-type: none"> • Derivation of time response (7M) <p>Consider the unit step signal as an input to the second order system. Laplace transform of the unit step signal is,</p> $R(s) = \frac{1}{s}$ <p>We know the transfer function of the second order closed loop control system is,</p> $\frac{C(s)}{R(s)} = \frac{\omega_n^2}{s^2 + 2\delta\omega_n s + \omega_n^2}$ <p>Substitute, $\delta = 0$ in the transfer function.</p> $\frac{C(s)}{R(s)} = \frac{\omega_n^2}{s^2 + \omega_n^2}$ $\Rightarrow C(s) = \left(\frac{\omega_n^2}{s^2 + \omega_n^2} \right) R(s)$
2.	<p>Derive the time response of first order system for unit step input and ramp input(13M) (April May 2016) ,(Nov Dec 2015) BTL6</p> <p>Answer: Page 3.8 to 3.9 - A.Nagoor Kani</p> <ul style="list-style-type: none"> • Block diagram of first order system (3M)  <p style="text-align: center;"><i>Closed loop for first order system.</i></p> <ul style="list-style-type: none"> • Derivation of time response for step input and its graph (5M) $c(t) = \mathcal{L}^{-1}\{C(s)\} = \mathcal{L}^{-1}\left\{ \frac{1}{s} - \frac{1}{s + \frac{1}{T}} \right\} = 1 - e^{-\frac{t}{T}}$



- Derivation of time response for ramp input (5M)



$$c(t) = t - T(1 - e^{-t/T})$$

With a neat block diagram and derivation explain how PI, PD and PID compensation will improve the time response of a system (13M) (April/May 2016) - Repeated question BTL1

Answer: Page 3.21 to 3.23 - A.Nagoor Kani

Controllers (3M)

A controller is a device introduced in the system to modify the error signal and to produce a control signal.

The controller modifies the transient response of the system.

The following six basic control actions are very common among industrial analog controllers

- 3.
- Two position or ON-OFF control action
 - Proportional control action
 - Integral control action
 - Proportional plus integral control action
 - Proportional plus derivative control action
 - Proportional plus integral plus derivative control action.

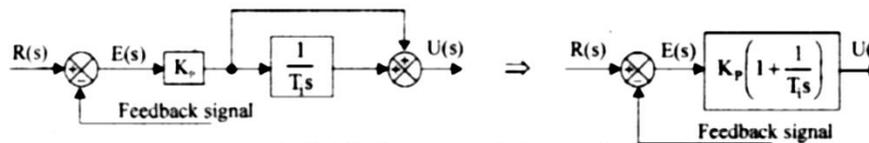
Response with PI controller (3M)

- Output signal consisting of two terms: one proportional to error signal and the other proportional to the integral of error signal

$$\text{In PI-controller, } u(t) \propto \left[e(t) + \int e(t) dt \right]; \quad \therefore u(t) = K_p e(t) + \frac{K_p}{T_i} \int e(t) dt$$

$$U(s) = K_p E(s) + \frac{K_p}{T_i} \frac{E(s)}{s}$$

$$\therefore \text{Transfer function of PI-controller, } \frac{U(s)}{E(s)} = K_p \left(1 + \frac{1}{T_i s} \right)$$



Response with PD controller (3M)

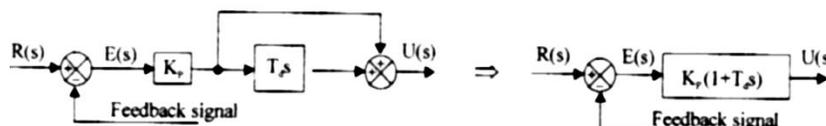
- Output signal consisting of two terms: one proportional to error signal and the other proportional to the derivative of error signal

In PD - controller, $u(t) \propto \left[e(t) + \frac{d}{dt} e(t) \right]$; $\therefore u(t) = K_p e(t) + K_p T_d \frac{d}{dt} e(t)$

where, K_p = Proportional gain

T_d = Derivative time

\therefore Transfer function of PD - controller, $\frac{U(s)}{E(s)} = K_p (1 + T_d s)$



Response with PID controller (4M)

- Output signal consisting of three terms: one proportional to error signal, another one proportional to integral of error signal and the third one proportional to derivative of error signal.

In PID - controller, $u(t) \propto \left[e(t) + \int e(t) dt + \frac{d}{dt} e(t) \right]$
 $\therefore u(t) = K_p e(t) + \frac{K_p}{T_i} \int e(t) dt + K_p T_d \frac{d}{dt} e(t)$

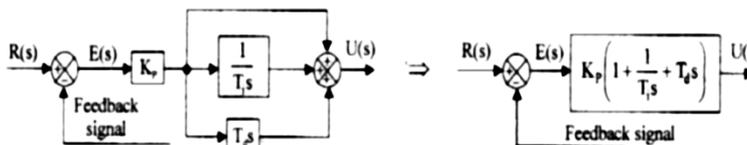
where, K_p = Proportional gain

T_i = Integral time

T_d = Derivative time

$U(s) = K_p E(s) + \frac{K_p}{T_i} \frac{E(s)}{s} + K_p T_d s E(s)$

\therefore Transfer function of PID - controller, $\frac{U(s)}{E(s)} = K_p \left(1 + \frac{1}{T_i s} + T_d s \right)$



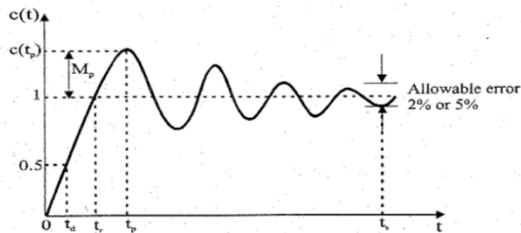
4. Define the following terms of time domain analysis of a control system
 1.Delay time 2.Rise time 3.Over shoot 4.Settling time(13M) BTL1

Answer: Page 3.16 to 3.21 - A.Nagoor Kani

Time domain specification

(2M)

The time response characteristics of the system at under damped condition is drawn below.



The transient response characteristics of a control system to a unit step input is specified in terms of the following specifications

- Delay time
- Rise time
- Peak time
- Maximum overshoot
- Settling time

Delay time

(2M)

Delay time (t_d) is the time required to reach at 50% of its final value by a time response signal during its first cycle of oscillation.

Rise time

(3M)

Rise time (t_r) is the time required to reach at final value by a under damped time response signal during its first cycle of oscillation. If the signal is over damped, then rise time is counted as the time required by the response to rise from 10% to 90% of its final value.

$$\therefore \text{Rise Time, } t_r = \frac{\pi - \theta}{\omega_d}$$

where

$$\theta = \tan^{-1} \frac{\sqrt{1-\zeta^2}}{\zeta}$$

$$\therefore \text{Rise time, } t_r = \frac{\pi - \tan^{-1} \frac{\sqrt{1-\zeta^2}}{\zeta}}{\omega_n \sqrt{1-\zeta^2}} \text{ in sec}$$

Peak overshoot

(3M)

Maximum overshoot (M_p) is straight way difference between the magnitude of the highest peak of time response and magnitude of its steady state. Maximum overshoot is expressed in term of percentage of steady-state value of the response. As the first peak of response is normally maximum in magnitude, maximum overshoot is simply normalized difference between first peak and steady-state value of a response.

$$\% \text{Peak overshoot, } \%M_p = \frac{c(t_p) - c(\infty)}{c(\infty)} \times 100$$

$$\therefore \text{Percentage Peak Overshoot, } \%M_p = e^{-\frac{\zeta\pi}{\sqrt{1-\zeta^2}}} \times 100$$

Settling time

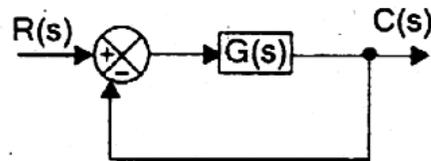
(3M)

Settling time (t_s) is the time required for a response to become steady. It is defined as the time required by the response to reach and steady within specified range of 2 % to 5 % of its final value.

	<div style="border: 1px solid black; padding: 5px; margin-bottom: 5px;"> Settling time, $t_s = \frac{1}{\zeta\omega_n} = 4T$ (for 2% error) </div> <div style="border: 1px solid black; padding: 5px; margin-bottom: 5px;"> Settling time, $t_s = \frac{3}{\zeta\omega_n} = 3T$ (for 5% error) </div> <div style="border: 1px solid black; padding: 5px;"> \therefore Settling time, $t_s = \frac{\ln(\% \text{ error})}{\zeta\omega_n} = \frac{\ln(\% \text{ error})}{T}$ </div>
5.	<p>The response of a servomechanism is $c(t) = 1 + 0.2e^{-60t} - 1.2e^{-10t}$ when subjected to a unit step input. Obtain an expression for closed loop transfer function. Determine the undamped natural frequency and damping ratio. (13M) BTL4</p> <p>Answer: Page 3.26 to 3.27 - A.Nagoor Kani</p> <ul style="list-style-type: none"> • Take Laplace transform (3M) • Find closed loop response of the system (5M) • Determine the undamped natural frequency and damping ratio (5M) <p>Given that $c(t) = 1 + 0.2e^{-60t} - 1.2e^{-10t}$</p> <p>On taking Laplace transform of $c(t)$ we get</p> $C(s) = \frac{1}{s} + 0.2 \frac{1}{(s+60)} - 1.2 \frac{1}{(s+10)} = \frac{(s+60)(s+10) + 0.2s(s+10) - 1.2s(s+60)}{s(s+60)(s+10)}$ $= \frac{s^2 + 70s + 600 + 0.2s^2 + 2s - 12s^2 - 72s}{s(s+60)(s+10)} = \frac{600}{s(s+60)(s+10)} = \frac{1}{s} \frac{600}{(s+60)(s+10)}$ <p>Since the input is unit step input $R(s) = 1/s$</p> $C(s) = R(s) \frac{600}{(s+60)(s+10)} = R(s) \frac{600}{s^2 + 70s + 600}$ <p>The closed loop transfer function of the system is $\frac{C(s)}{R(s)} = \frac{600}{s^2 + 70s + 600}$</p> <p>The damping ratio and natural frequency of oscillation can be estimated by comparing the system transfer function with standard form of second order transfer function</p> $\frac{C(s)}{R(s)} = \frac{\omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} = \frac{600}{s^2 + 70s + 600}$ <p>On comparing we get</p> $\omega_n^2 = 600 \quad \left \quad 2\zeta\omega_n = 70 \right.$ $\therefore \omega_n = \sqrt{600} = 24.49 \text{ rad/sec} \quad \left \quad \therefore \zeta = \frac{70}{2\omega_n} = \frac{70}{2 \times 24.49} = 1.43 \right.$
6.	<p>A unity feed back control system has an open loop transfer function $G(s) = 10/s(s+2)$. Find the rise time, percentage over shoot, peak time and settling</p>

time for a step input of 12 units(13M) BTL4.

Answer: Page 3.35 to 3.36 - A.Nagoor Kani



- Find the closed loop transfer function (2M)

$$\therefore \frac{C(s)}{R(s)} = \frac{\frac{10}{s(s+2)}}{1 + \frac{10}{s(s+2)}} = \frac{10}{s(s+2)+10} = \frac{10}{s^2+2s+10}$$

- The standard form of second order transfer function is (1M)

$$\frac{C(s)}{R(s)} = \frac{\omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2}$$

- Compare both the transfer function (3M)

$$\omega_n^2 = 10 \quad \left| \quad 2\zeta\omega_n = 2\right. \\ \therefore \omega_n = \sqrt{10} = 3.162 \text{ rad/sec} \quad \left| \quad \therefore \zeta = \frac{2}{2\omega_n} = \frac{1}{3.162} = 0.316$$

$$\theta = \tan^{-1} \frac{\sqrt{1-\zeta^2}}{\zeta} = \tan^{-1} \frac{\sqrt{1-0.316^2}}{0.316} = 1.249 \text{ rad}$$

$$\omega_d = \omega_n \sqrt{1-\zeta^2} = 3.162 \sqrt{1-0.316^2} = 3 \text{ rad/sec}$$

- Find the time domain specifications (7M)

$$\text{Rise time } t_r = \frac{\pi - \theta}{\omega_d} = \frac{\pi - 1.249}{3} = 0.63 \text{ sec}$$

$$\text{Percentage overshoot \%Mp} = e^{\frac{-\zeta\pi}{\sqrt{1-\zeta^2}}} \times 100 = e^{\frac{-0.316\pi}{\sqrt{1-0.316^2}}} \times 100 \\ = 0.3512 \times 100 = 35.12\%$$

$$\text{Peak overshoot} = \frac{35.12}{100} \times 12 \text{ units} = 4.2144 \text{ units}$$

$$\text{Peak time } t_p = \frac{\pi}{\omega_d} = \frac{\pi}{3} = 1.047 \text{ sec}$$

$$\text{Time constant } T = \frac{1}{\zeta\omega_n} = \frac{1}{0.316 \times 3.162} = 1 \text{ sec}$$

$$\text{For 5\% error, settling time } t_s = 3T = 3 \text{ sec}$$

- For 2% error, settling time $t_s = 4T = 4 \text{ sec}$

PART * C	
Q.No	Questions
1.	<p>For a unity feedback control system the open loop transfer function $G(s) = 10(s+2) / s^2(s+1)$ Find, (a) The position, velocity and acceleration error constant. (b) The steady state error when the input is $R(s) = \frac{3}{s} + \frac{2}{s^2} + \frac{1}{3s^3}$ (15M) BTL3</p> <p>Answer: Page 3.45 to 3.48 - A.Nagoor Kani</p> <p>➤ Find static error constants (position error constant, Velocity error constant, Acceleration error constant) (8M)</p> <p>Position error constant, $K_p = \lim_{s \rightarrow 0} G(s)H(s) = \lim_{s \rightarrow 0} G(s) = \lim_{s \rightarrow 0} \frac{10(s+2)}{s^2(s+1)} = \infty$</p> <p>Velocity error constant, $K_v = \lim_{s \rightarrow 0} s G(s)H(s) = \lim_{s \rightarrow 0} s G(s) = \lim_{s \rightarrow 0} s \frac{10(s+2)}{s^2(s+1)} = \infty$</p> <p>Acceleration error constant, $K_a = \lim_{s \rightarrow 0} s^2 G(s)H(s) = \lim_{s \rightarrow 0} s^2 G(s)$ $= \lim_{s \rightarrow 0} s^2 \frac{10(s+2)}{s^2(s+1)} = \frac{10 \times 2}{1} = 20$</p> <p>➤ Find steady state error The error signal is (7M)</p> $e(t) = r(t)C_0 + \dot{r}(t)C_1 + \frac{\ddot{r}(t)}{2!}C_2 + \dots + \frac{r^{(n)}(t)}{n!}C_n + \dots$ $r(t) = \mathcal{L}^{-1}\{R(s)\} = \mathcal{L}^{-1}\left\{\frac{3}{s} - \frac{2}{s^2} + \frac{1}{3s^3}\right\}$ $= 3 - 2t + \frac{1}{3} \frac{t^2}{2!} = 3 - 2t + \frac{t^2}{6}$ <p>$C_0 = \lim_{s \rightarrow 0} F(s); \quad C_1 = \lim_{s \rightarrow 0} \frac{d}{ds} F(s); \quad C_2 = \lim_{s \rightarrow 0} \frac{d^2}{ds^2} F(s)$ $C_0=0, C_1=0$ and $C_2=0.1$ then $ess=1/60$</p>
2.	<p>For servomechanism with open loop transfer function given below explains what type input signal give rise to a constant steady state error and calculate their values</p> <p>a) $G(s) = \frac{20(s+2)}{s(s+1)(s+3)}$; b) $G(s) = \frac{10}{(s+2)(s+3)}$; c) $G(s) = \frac{10}{s^2(s+1)(s+2)}$ (15M) (5M+5M+5M) BTL3</p> <p>Answer: Page 3.48 to 3.49 - A.Nagoor Kani</p>

$$(i) \quad G(s) = \frac{20(s+2)}{s(s+1)(s+3)}$$

Let us assume unity feedback system $H(s)=1$.

The open loop system has a pole at origin. Hence it is a type 1 system. In systems with type number 1, the velocity (ramp) input will give a constant steady state error.

The steady state error with unit velocity input, $e_{ss} = \frac{1}{K_v}$

Velocity error constant

$$\begin{aligned} K_v &= \lim_{s \rightarrow 0} s G(s) H(s) = \lim_{s \rightarrow 0} s G(s) \\ &= \lim_{s \rightarrow 0} s \frac{20(s+2)}{s(s+1)(s+3)} = \frac{20 \times 2}{1 \times 3} = \frac{40}{3} \\ e_{ss} &= \frac{1}{K_v} = \frac{3}{40} = 0.075 \end{aligned}$$

$$(ii) \quad G(s) = \frac{10}{(s+2)(s+3)}$$

Let us assume unity feedback system $H(s)=1$.

The open loop system has no pole at origin. Hence it is a type 0 system. In systems with type number 0, the step input will give a constant steady state error.

The steady state error with unit step input $e_{ss} = \frac{1}{1+K_p}$

$$\text{Position error constant } K_p = \lim_{s \rightarrow 0} G(s) H(s) = \lim_{s \rightarrow 0} G(s) = \lim_{s \rightarrow 0} \frac{10}{(s+2)(s+3)} = \frac{10}{2 \times 3} = \frac{5}{3}$$

$$\text{Then } e_{ss} = 0.375$$

$$(iii) \quad G(s) = \frac{10}{s^2(s+1)(s+2)}$$

Let us assume unity feedback system $H(s)=1$

The open loop system has two poles at origin. Hence it is a type 2 system. In systems with type number 2, the acceleration (parabolic) input will give a constant steady state error.

The steady state error with unit acceleration input, $e_{ss} = \frac{1}{K_a}$

Acceleration error constant,

$$e_{ss} = \frac{1}{K_a} = \frac{1}{5} = 0.2$$

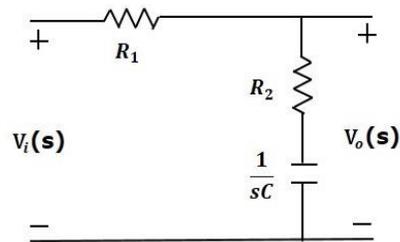
UNIT III FREQUENCY RESPONSE ANALYSIS	
	Closed loop frequency response-Performance specification in frequency domain-Frequency response of standard second order system- Bode Plot - Polar Plot- Nyquist plots-Design of compensators using Bode plots-Cascade lead compensation-Cascade lag compensation-Cascade lag-lead compensation
	PART * A
Q.No	Questions
1.	What is frequency response? BTL1 The frequency and phase function of sinusoidal transfer function of a system are real function of frequency so they are called frequency response.
2.	What are the advantages of frequency response analysis? BTL2 <ul style="list-style-type: none"> • The absolute and relative stability of the closed loop system can be estimated from the knowledge of their open loop frequency response • The practical testing of the systems can be easily done with available sinusoidal generators and precise measurements equipments. • The transfer function of the complicated systems can be determined experimentally by frequency response tests. • The effects of noise disturbances and parameter variations are relatively easy to visualize and incorporate corrective measures. • Analysis can be extended to certain non linear system.
3.	State any four-frequency domain specification. (April May 2016,Nov Dec 2015) BTL1 <ul style="list-style-type: none"> • Resonant Peak • Resonant frequency • Cut-off region • Phase Margin • Gain Margin • Phase cross over frequency • Gain cross over frequency
4.	Define gain Margin. (April May 2017, April May 2018) BTL1 The gain margin (G.M.) is defined as the margin in gain allowable by which gain can be increased till system reaches on the verge of instability. Mathematically it can be defined as reciprocal of the magnitude of the $G(j\omega)H(j\omega)$ measured at phase crossover frequency.
5.	Define phase margin. (April May 2018) BTL1 The amount of additional phase lags which can be introduced in the system till the system reaches on the verge of instability is called phase margin.
6.	What is gain crossover frequency and phase crossover frequency? BTL1 Gain crossover frequency (ω_{gc}): The frequency at which magnitude of $G(j\omega)H(j\omega)$ is unity is called gain crossover frequency. Phase crossover frequency (ω_{pc}): The frequency at which phase angle of $G(j\omega)H(j\omega)$ is -180 deg. is called phase crossover frequency.
7.	What is meant by corner frequency in frequency response analysis? BTL 1 A frequency up to which the magnitude contribution of a factor is negligible and can be

	neglected is called its corner frequency. It is the frequency at which low frequency and high frequency asymptotes intersect each other. At the corner frequency, a change in the slope of a magnitude plot occurs. Frequency range and the number of points is chosen automatically.
8.	How the resonant peak (M_r), resonant frequency (ω_r), and band width are determined from Nichols chart? BTL2 The resonant peak is given by the value of μ . Contour which is tangent to $G(j\omega)$ locus. The resonant frequency is given by the frequency of $G(j\omega)$ at the tangent point. The bandwidth is given by frequency corresponding to the intersection point of $G(j\omega)$ and $-3\text{dB } M$ -contour.
9.	What is meant by Cut of frequency? BTL 1 it is denoted by ω_b . the frequency at which the magnitude of the closed loop response is 3 dB down from its zero-frequency value is called cut-off frequency.
10.	What is meant by resonant peak? (Nov Dec 2018) BTL1 Resonant peak (M_r): It is the maximum value of magnitude of the closed loop frequency response.
11.	What is meant by resonant frequency? (Nov Dec 2018) BTL1 Resonant frequency (ω_r): The frequency at which resonant peak M_r occurs in closed loop frequency response is called resonant frequency.
12.	Write a short note on correlation between the time and frequency response? BTL1 Correlation between time and frequency response of first order or second order systems. The frequency domain specifications can be expressed in terms of the time domain parameters δ and ω_n . For a peak overshoot in time domain there is a corresponding resonant peak in frequency domain. For higher order systems, there is no explicit correlation between time and frequency response. But if there is a pair of dominant complex conjugate poles, then the system can be approximated to second order system and the correlation between time and frequency response can be estimated.
13.	What are the graphical techniques available for the frequency response analysis? BTL1 <ul style="list-style-type: none"> • Bode plot • Polar plot • Nichols plot • M and N circles • Nichols chart
14.	What are the advantages of Bode plot? BTL 2 <ul style="list-style-type: none"> • It shows both low and high frequency characteristics of transfer function in single diagram. • The plots can be easily constructed using some valid approximations. • Relative stability of system can be studied by calculating G.M. and P.M. from the bode plot. • The various other frequency domain specifications like cut-off frequency, bandwidth etc. can be determined. • Data for constructing complicated polar and Nyquist plots can be easily obtained from Bode plot.

	<ul style="list-style-type: none"> Transfer function of system can be obtained from the bode plot.
15.	<p>What is polar plot? BTL1</p> <p>The polar plot of a sinusoidal transfer function $G(j\omega)$ is a plot of the magnitude of $G(j\omega)$ versus the phase angle/argument of $G(j\omega)$ on polar or rectangular coordinates as ω is varied from zero to infinity</p>
16.	<p>What is minimum phase system? BTL1</p> <p>The minimum phase systems are system with minimum phase transfer functions. In minimum phase transfer functions, all poles and zeros will lie on the left half of s plane.</p>
17.	<p>In minimum phase system, how start and end of polar plots are identified? BTL2</p> <p>For minimum phase transfer functions, with only poles, the type number of the system determines the quadrant in which the polar plot starts and the order of the system determines the quadrant in which the polar plot ends.</p> <p>The left diagram shows a Cartesian coordinate system with the following labels: <ul style="list-style-type: none"> Start of type-3 system: arrow pointing up from the origin. Start of type-2 system: arrow pointing right from the origin. Start of type-1 system: arrow pointing down from the origin. Start of type-0 system: arrow pointing left from the origin. Start of polar plot of all pole minimum phase system: arrow pointing from the origin towards the bottom-left quadrant. </p> <p>The right diagram shows a Cartesian coordinate system with the following labels: <ul style="list-style-type: none"> End of 3rd order system: arrow pointing up from the origin. End of 4th order system: arrow pointing right from the origin. End of 2nd order system: arrow pointing down from the origin. End of 1st order system: arrow pointing left from the origin. Start of polar plot of all pole minimum phase system: arrow pointing from the origin towards the bottom-left quadrant. </p>
18.	<p>What is the use of Nichol's chart in control system? (April May 2015 ,Nov Dec 2016) BTL2</p> <p>Nichol's chart used to find closed loop frequency response from open loop frequency response.</p> <p>The frequency domain specifications can be determined from Nichols chart.</p> <p>➤ The gain of the system can be adjusted to satisfy the given specifications.</p>
19.	<p>What are the characteristics of phase lead network? (April May 2015) BTL4</p> <p>Increases system bandwidth which usually correlates to reduce rise and settling times and a susceptibility to high frequency noise.</p> <p>The phase of the forward path transfer function in the vicinity of the zero-gain crossover frequency. This increases the phase margin of the closed loop system and hence the relative stability.</p>
20.	<p>What is compensation?(April May 2017, April May 2018, Nov Dec 2018) BTL1</p> <p>The compensation is the design procedure in which the system behaviour is altered to meet the desired specifications, by introducing additional device called compensator.</p>
21.	<p>What are compensators? What are the different types of compensator? BTL1</p> <p>A device inserted into the system for the purpose of satisfying the specifications is called compensator. The different types of compensators are lag, lead and lag lead compensators.</p>
22.	<p>What is the basis for selection of a compensator for a system? BTL2</p> <p>When the system is to be redesigned to meet the required specifications, it is necessary to alter the system by adding an external device to it. The system must provide,</p> <ul style="list-style-type: none"> Attenuation in the high frequency range to give a system enough phase margins. Large bandwidth, short rise time and less settling time.
23.	<p>What is series compensation?(Nov Dec 2016) BTL1</p>

	If a compensator is placed in series with the forward path transfer function of the plant is called as series compensation.
24.	What is parallel compensation? BTL1 Feedback is taken from some internal element and compensator is introduced in such a feedback path to provide an additional internal feedback loop is called parallel compensation.
25.	What is series parallel compensation? BTL1 In some cases, it is necessary to provide both types of compensations series as well as feedback. Such scheme is called series parallel compensation.
26.	When lag/lead/lag lead compensation is employed? BTL2 Lag compensation is employed for a stable system for improvement in steady state performance Lead compensation is employed for stable /unstable system for improvement in transient state performance Lag lead compensation is employed for stable/unstable system for improvement in both steady state and transient state performance.
27.	Discuss the effect of adding a pole to open loop transfer function of a system? BTL2 The addition of a pole to open loop transfer function of a system will reduce the steady state error. The closer the pole to origin lesser will be the steady state error. Thus, the steady state performance of the system is improved. In addition, the addition of pole will increase the order of the system, which in turn makes the system less stable than the original system.
28.	Discuss the effect of adding a zero to open loop transfer function of a system. BTL2 The addition of a zero to open loop transfer function of a system will improve the transient response. The addition of zero reduces the rise time. If the zero is introduced close to origin then the peak overshoot will be larger. If the zero is introduced far away from the origin in the left half of the s plane then the effect of zero on the transient response will be negligible.
29.	What is lag compensation? BTL1 A compensator having the characteristics of lag network is called lag compensator. The Lag Compensator is an electrical network which produces a sinusoidal output having the phase lag when a sinusoidal input is applied.
30.	What is lead compensation? BTL1 A compensator having the characteristics of a lead network is called a lead compensator. If a sinusoidal is applied to the lead network then in steady state the output will have a phase lead with respect to input.
31.	What is lag lead compensation? BTL1 Lag-Lead compensator is an electrical network which produces phase lag at one frequency region and phase lead at other frequency region. It is a combination of both the lag and the lead compensators.
	PART * B
Q.No	Questions
1.	Sketch bode plot for the following transfer function and determine the system gain K for the gain cross over frequency to be 5 rad/sec(13M)BTL3

	$G(s) = \frac{Ks^2}{(1+0.2s)(1+0.02s)}$ <p>Answer: Page 4.22 to 4.24 - A.Nagoor Kani</p> <ul style="list-style-type: none"> The sinusoidal transfer function $G(j\omega)$ is obtained by replacing S by $j\omega$ in the given S domain transfer function (1M) The corner frequencies are 5 and 50 rad/sec (1M) Find slope and change in slope and tabulate the same (2M) Find gain for different values of corner frequencies (2M) Draw the magnitude plot (3M) Draw the phase plot for different values of phase angles. (3M) Calculate gain $K=0.0398$ (1M)
2.	<p>The open loop transfer function of a unity feedback system is given by $G(s)=1/s(s+1)(1+2s)$. Sketch the polar plot and determine the gain margin and phase margin(13M)BTL3</p> <p>Answer: Page 4.44 to 4.46 - A.Nagoor Kani</p> <ul style="list-style-type: none"> The sinusoidal transfer function $G(j\omega)$ is obtained by replacing S by $j\omega$ in the given S domain transfer function (1M) The corner frequencies are 0.5 and 1 rad/sec (1M) Find magnitude and phase at different frequencies (6M) Calculate gain and phase margin from the polar plot (5M) <p>Gain margin is 1.4286 Phase margin is 12°</p>
3.	<p>Discuss about lag,Lead,Lag lead compensator.(13M)(Nov Dec 2017)BTL2</p> <p>Answer: Page 6.4,6.20,6.53 - A.Nagoor Kani</p> <p>An external device which is used to alter the behavior of the system so as to achieve given specifications is called compensator. The compensator provides whatever missing in a system so as to achieve required performance.</p> <p>Lag compensators (4M)</p> <p>A compensator having the characteristics of lag network is called lag compensator. The Lag Compensator is an electrical network which produces a sinusoidal output having the phase lag when a sinusoidal input is applied. The lag compensator circuit in the 's' domain is shown in the following figure.</p>



The transfer function of the lag compensator

$$\frac{V_o(s)}{V_i(s)} = \frac{1}{\alpha} \left(\frac{s + \frac{1}{\tau}}{s + \frac{1}{\alpha\tau}} \right)$$

where

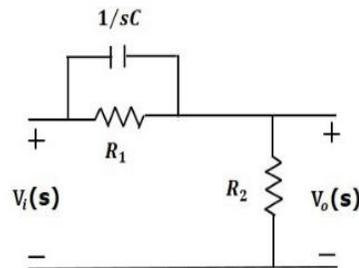
$$\tau = R_2 C$$

$$\alpha = \frac{R_1 + R_2}{R_2}$$

Lead compensators

(4M)

A compensator having the characteristics of a lead network is called a lead compensator. If a sinusoidal is applied to the lead network then in steady state the output will have a phase lead with respect to input. The lead compensator circuit in the 's' domain is shown in the following figure.



The transfer function of the lead compensator is

$$\frac{V_o(s)}{V_i(s)} = \beta \left(\frac{s\tau + 1}{\beta s\tau + 1} \right)$$

Where,

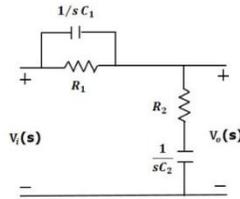
$$\tau = R_1 C$$

$$\beta = \frac{R_2}{R_1 + R_2}$$

Lag Lead compensators

(5M)

Lag-Lead compensator is an electrical network which produces phase lag at one frequency region and phase lead at other frequency region. It is a combination of both the lag and the lead compensators. The lag-lead compensator circuit in the 's' domain is shown in the following figure.



The transfer function of this network is the product of transfer function of the lag and lead network.

$$\frac{V_o(s)}{V_i(s)} = \beta \left(\frac{s\tau_1 + 1}{\beta s\tau_1 + 1} \right) \frac{1}{\alpha} \left(\frac{s + \frac{1}{\tau_2}}{s + \frac{1}{\alpha\tau_2}} \right)$$

We know $\alpha\beta = 1$.

$$\Rightarrow \frac{V_o(s)}{V_i(s)} = \left(\frac{s + \frac{1}{\tau_1}}{s + \frac{1}{\beta\tau_1}} \right) \left(\frac{s + \frac{1}{\tau_2}}{s + \frac{1}{\alpha\tau_2}} \right)$$

Where,

$$\tau_1 = R_1 C_1$$

$$\tau_2 = R_2 C_2$$

Write the procedure for lag compensator design using bode plot. (13M)(Nov Dec 2016)BTL1

Answer: Page 6.9 to 6.11 - A.Nagoor Kani

The following steps may be followed to design a lag compensator using bode plot and to be connected in series with the transfer function of uncompensated system

Step 1: Choose the value of K of uncompensated system to meet the steady state requirements

Step 2: Sketch the bode plot for the uncompensated system

Step 3: Determine the phase margin of the uncompensated system from the bode plot. If the margin does not satisfy the requirement then lag compensation is required.

4.

Step 4: Choose a suitable value for the phase margin of the uncompensated system.

$$\gamma_n = \gamma_d + \xi$$

Step 5: Determine the new gain cross over frequency ω_{gcn}

Step 6: Determine the parameter β of the compensator. Find db gain at new gain cross over frequency

Step 7: Determine the transfer function of the lag compensator.

Step 8: Determine the open loop transfer function of the compensated system

Step 9: Determine the actual phase margin of the compensated system. If the actual phase margin is satisfies the given specification then the design is accepted. Otherwise the procedure from step 4 to 9 by taking $\xi = 5^\circ$ more than previous design.

5.

Consider the following system, $G(s) = K/S(1+2S)$. Design a lag compensator so that the phase margin (PM) is at least 40° and steady state error to a unit step input is ≤ 0.2 (13M)BTL6

	<p>Answer: Page 6.11 to 6.15 - A.Nagoor Kani</p> <p>Step 1: Choose the value of K of uncompensated system to meet the steady state requirements K=5</p> <p>Step 2: Sketch the bode plot for the uncompensated system (2M)</p> <p>Step 3: Determine the phase margin of the uncompensated system from the bode plot. If the margin does not satisfy the requirement then lag compensation is required. (2M)</p> <p style="text-align: center;">Phase margin =18°</p> <p>Step 4: Choose a suitable value for the phase margin of the uncompensated system. (1M)</p> $\gamma_n = \gamma_d + \xi$ $=45^\circ$ <p>Step 5: Determine the new gain cross over frequency ω_{gc} (2M)</p> $=0.5 \text{ rad/sec}$ <p>Step 6: Determine the parameter β of the compensator. Find db gain at new gain cross over frequency (1M) $\beta =10$</p> <p>Step 7: Determine the transfer function of the lag compensator. (2M)</p> $G(s)=10(1+20S)/(1+200S)$ <p>Step 8: Determine the open loop transfer function of the compensated system (2M)</p> $G(S)=5(1+20S)/S(1+200S)(1+2S)$ <p>Step 9: Determine the actual phase margin of the compensated system. (2M)</p> <p style="text-align: center;">Phase margin =18°</p> <p>The actual phase margin of the compensated system satisfies the requirement. Hence, the design is acceptable.</p>
6.	<p>Write the procedure for lead compensator design using bode plot.(13 M) (April May 2016) BTL1</p> <p>Answer: Page 6.32 to 6.333 - A.Nagoor Kani</p> <p>The following steps may be followed to design a lead compensator using bode plot and to be connected in series with the transfer function of uncompensated system</p> <p>Step 1: Choose the value of K of uncompensated system to meet the steady state requirements</p> <p>Step 2: Sketch the bode plot for the uncompensated system</p> <p>Step 3: Determine the phase margin of the uncompensated system from the bode plot. If the margin does not satisfy the requirement then lag compensation is required.</p> <p>Step 4: Choose a suitable value for the phase margin of the uncompensated system.</p> $\gamma_n = \gamma_d - \gamma + \xi$ <p>Step 5: Determine the transfer function of the lead compensator.</p> <p>Step 6: Determine the open loop transfer function of the compensated system</p> <p>Step 7: Verify the design</p>
7.	<p>Write the procedure for lag lead compensator design using bode plot(13M)(Nov Dec 2018) BTL1</p> <p>Answer: Page 6.55 to 6.57 - A.Nagoor Kani</p>

	<p>The following steps may be followed to design a lag compensator using bode plot and to be connected in series with the transfer function of uncompensated system</p> <p>Step 1: Choose the value of K of uncompensated system to meet the steady state requirements</p> <p>Step 2: Sketch the bode plot for the uncompensated system</p> <p>Step 3: Determine the phase margin of the uncompensated system from the bode plot. If the margin does not satisfy the requirement then lag compensation is required.</p> <p>Step 4: Choose a suitable value for the phase margin of the uncompensated system.</p> $\gamma_n = \gamma_d + \xi$ <p>Step 5: Determine the new gain cross over frequency ω_{gcn}</p> <p>Step 6: Determine the parameter β of the lag compensator. Find db gain at new gain cross over frequency</p> <p>Step 7: Determine the transfer function of the lag compensator.</p> <p>Step 8: Determine the transfer function of the lead compensator.</p> <p>Step 9: Determine the transfer function of the lag lead compensator</p> <p>Step 10: Determine the open loop transfer function of the compensated system</p> <p>Step 11: Draw the bode plot of the compensated system and verify whether the specifications are satisfied or not. If the specifications are not satisfied then choose another choice of α such that $\alpha < 1/\beta$ and repeat steps 8 to 11</p>
	PART * C
Q.No	Questions
1.	<p>Sketch the bode plot for the following transfer function and determine phase margin and gain margin(15M)BTL3.</p> $G(s) = \frac{75(1+0.2s)}{s(s^2+16s+100)}$ <p>Answer: Page 4.25 to 4.28 - A.Nagoor Kani</p> <ul style="list-style-type: none"> • The sinusoidal transfer function $G(j\omega)$ is obtained by replacing S by $j\omega$ in the given S domain transfer function (1M) • The corner frequencies are 5 and 10 rad/sec (2M) • Find slope and change in slop and tabulate the same (1M) • Find gain for different values of corner frequencies (2M) • Draw the magnitude plot (3M) • Draw the phase plot for different values of phase angles. (3M) • Find phase margin and gain margin from the bode plot (3M) <p>Phase margin=92° Gain margin=Infinity</p>
2.	<p>The open loop transfer function of a unity feedback system is given by the following. Sketch the polar plot and determine the phase margin (15M) BTL3.</p> $G(s) = \frac{(1+0.2s)(1+0.025s)}{s^3(1+0.005s)(1+0.001s)}$

	<p>Answer: Page 4.50 to 4.52 - A.Nagoor Kani</p> <ul style="list-style-type: none"> The sinusoidal transfer function $G(j\omega)$ is obtained by replacing S by $j\omega$ in the given S domain transfer function (1M) Find magnitude and phase at different frequencies (8M) Calculate gain and phase margin from the polar plot (6M) <p>Phase margin is -77°</p>
3.	<p>Consider the following system with transfer function Design a lag lead compensator $C(s)$ such that the phase margin of the compensated system is at 35 degree .and the velocity error constant K_v is 80 (15M) BTL6.</p> <p>$G(S)=K/s(s+3)(s+6)$</p> <p>Answer: Page 6.59 to 6.65 - A.Nagoor Kani</p> <p>Step 1: Choose the value of K of uncompensated system to meet the steady state requirements (1M)</p> <p style="text-align: center;">$K=1440$</p> <p>Step 2: Sketch the bode plot for the uncompensated system (2M)</p> <p>Step 3: Determine the phase margin of the uncompensated system from the bode plot. If the margin does not satisfy the requirement then lag compensation is required. (1M)</p> <p style="text-align: center;">Phase margin = -46° (from the bode plot)</p> <p>Step 4: Choose a suitable value for the phase margin of the uncompensated system. (1M)</p> <p style="text-align: center;">$\gamma_n = \gamma_d + \xi$ Phase margin = 40°</p> <p>Step 5: Determine the new gain cross over frequency ω_{gc} (1M)</p> <p style="text-align: center;">$=4 \text{ rad/sec}$</p> <p>Step 6: Determine the parameter β of the lag compensator. Find db gain at new gain cross over frequency (1M)</p> <p style="text-align: center;">$=14$</p> <p>Step 7: Determine the transfer function of the lag compensator. (2M)</p> <p>$G_1(s)=14(1+2.5s)/(1+35s)$</p> <p>Step 8: Determine the transfer function of the lead compensator. (2M)</p> <p>$G_2(s)=0.07(1+0.22s)/(1+0.0154s)$</p> <p>Step 9: Determine the transfer function of the lag lead compensator (2M)</p> <p>$G_c(s)=(1+2.5s)(1+0.22s)/(1+35s)(1+0.0154s)$</p> <p>Step 10: Determine the open loop transfer function of the compensated system (1M)</p> <p>$G_c(s)=80(1+2.5s)(1+0.22s)/s(1+35s)(1+0.0154s)(1+0.33s)(1+0.167s)$</p> <p>Step 11: Draw the bode plot of the compensated system and verify whether the specifications are satisfied or not. (1M)</p> <p>Phase margin = 36°</p> <p>The phase margin of the compensated system is satisfactory. Hence the design is acceptable.</p>

UNIT IV CONCEPTS OF STABILITY ANALYSIS	
	Concept of stability-Bounded - Input Bounded - Output stability-Routh stability criterion-Relative stability-Root locus concept-Guidelines for sketching root locus-Nyquist stability criterion.
	PART * A
Q.No	Questions
1.	Define BIBO stability(Nov Dec 2016) BTL1 A linear relaxed system is said to have BIBO stability if every bounded input results in a bounded output
2.	How the roots of the characteristics equation are related to stability? BTL2 If the roots of the characteristics equation has real part then the impulse response of the system is not bounded .Hence the system will be unstable. If the roots has negative real part then the impulse response is bounded .Hence the system will be stable.
3.	What is the necessary condition for stability(April May 2016) BTL1 The necessary condition for stability is that all the coefficient of the characteristics polynomial be positive.
4.	What is Routh stability criterion? BTL1 The necessary and sufficient condition for stability is that all of the elements in the first column of the routh array be positive. If this condition is not met the system is unstable and the number of sign changes in the elements of the first column of the routh array corresponds to the number of roots of the characteristics equation in the right half of S plane
5.	What is auxiliary polynomial? BTL1 In the construction of Routh array a row of all zero indicates the existence of an even polynomial as a factor of the given characteristics equation. In an even polynomial, the exponents of s are even integers are zero only. This even polynomial factor is called auxiliary polynomial. The coefficient of auxiliary polynomial is given by the elements of the row just above the row of all zeros.
6.	What is root locus? BTL1 The path taken by a root locus of characteristics equation when open loop gain K is verified from 0 to infinity is called root locus.
7.	How will you find root locus on real axis?(April May 2016) BTL2 To find the root locus on real axis, choose a test point on real axis. If the total number of poles and zeros on the real axis to the right of this test point is odd number, then the test point lies on the root locus. If it is even then the test point does not lie on the root locus.
8.	What are asymptotes? How will you find the angle of asymptotes? BTL1 Asymptotes are straight lines which are parallel to the root locus going to infinity and meet the root locus at infinity. Angle of Asymptotes = $\frac{\pm 180^\circ(2q+1)}{n-m}$; $q = 0, 1, 2, \dots, (n-m)$
9.	What is centroid?How the centroid is calculated? BTL1 The meeting point of asymptotes with real axis is called centroid. The centroid is given by Centroid = $= \frac{\text{Sum of poles}-\text{Sum of zeros}}{n-m}$

10.	<p>How will you find the value of gain K at a point on a root locus?(April May 2015) BTL1</p> <p>The gain K at a point $S=S_a$ on root locus is given by</p> $K = \frac{\text{Product of length of vector from open loop poles to the point } S_a}{\text{Product of length of vector from open loop zeros to the point } S_a}$
11.	<p>What is breakaway and break-in points? How to determine them? BTL1</p> <p>At breakaway points, the root locus breaks from the real axis to enter into the complex plane. At break-in point, the root locus enters the real axis from the complex plane.</p> <p>To find the breakaway or break in points from an equation for K from the characteristics equation and differentiate the equation of K with respect to S. Then find the roots of equation $dK/ds=0$. The roots of dK/ds are breakaway or break-in points, provided for this value of gain K should be positive and real.</p>
12.	<p>How to find the crossing points of root locus in imaginary axis? BTL1</p> <p>By Routh Hurwitz criterion</p>
13.	<p>What is dominant pole?(Nov Dec 2015,Nov Dec 2016) Repeated question BTL1</p> <p>The dominant pole is a pair of complex conjugate pole which decides transient response of the system. In higher order systems the dominant poles are very close to the origin and all other poles of the system are widely separated and so they have less effect on transient response of the system.</p>
14.	<p>What is the relation between stability and coefficient of characteristics polynomial? BTL3</p> <p>If the coefficients of the characteristics polynomial are negative or zero, then some of the roots lies on right half of s plane. Hence the system is unstable, If the coefficients of characteristics polynomial are positive and if no efficient is zero then there is a possibility of the system to be stable provided all the roots of are lying on left half of S plane.</p>
15.	<p>What is the nature of impulse response when the roots of characteristics equation are lying on imaginary axis? BTL4</p> <p>If the roots of characteristics equation lie on imaginary axis the nature of the impulse response is oscillatory.</p>
16.	<p>What is the principle of argument? BTL1</p> <p>The principle of argument states that let $F(s)$ be an analytic function and if an arbitrary, closed contour in the clockwise direction is chosen in the s plane so that $F(s)$ is analytic at every point of the contour. Then the corresponding $F(S)$ plane contour mapped in the $F(s)$ plane will encircle the origin times in the anticlockwise direction where N is the difference between the number of poles, P and zeros Z of $F(s)$ that are enclosed by the chosen closed contour in the S plane.</p>
17.	<p>What is Nyquist stability criterion?(April May 2017,Nov Dec 2015, Nov Dec 2017) BTL1 Repeated question</p> <p>Consider an open-loop transfer function $GOL(s)$ that is proper and has no unstable pole-zero cancellations. Let N be the number of times that the Nyquist plot for $GOL(s)$ encircles the -1 point in the clockwise direction. Also let P denote the number of poles of $GOL(s)$ that lie to the right of the imaginary axis. Then, $Z = N + P$ where Z is the number of roots of the characteristic equation that lie to the right of the imaginary axis (that is, its number of "zeros"). The closed-loop system is stable if and only if $Z = 0$</p>

18.	<p>Write some important properties of Nyquist stability criterion.(April May 2018) BTL2</p> <ol style="list-style-type: none"> 1. It provides a necessary and sufficient condition for closed-loop stability based on the open-loop transfer function. 2. The reason the -1 point is so important can be deduced from the characteristic equation, $1 + G_{OL}(s) = 0$. This equation can also be written as $G_{OL}(s) = -1$, which implies that $AR_{OL} = 1$, as noted earlier. The -1 point is referred to as the <i>critical point</i>. 3. Most process control problems are open-loop stable. For these situations, $P = 0$ and thus $Z = N$. Consequently, the closed-loop system is unstable if the Nyquist plot for $G_{OL}(s)$ encircles the -1 point, one or more times. 												
19.	<p>What are the advantages of Nyquist stability criterion over that of Routh's criterion BTL2</p> <ul style="list-style-type: none"> • Routh criterion does not give the sufficient information about relative stability of the system • It does not help much in design problems in which the designer is required to achieve the desired performance by varying one or more system parameters. • Nyquist stability criterion gives information about both absolute stability and relative stability • Nyquist plot of open loop transfer function can be easily obtained.From this plot closed loop stability can be determined. 												
20.	<p>What will be the stability of the system when the roots of the characteristics equation are lying on imaginary axis?(Nov Dec 2017, April May 2018) Repeated question BTL2 Marginally stable or limitedly stable.</p>												
PART * B													
Q.No	Questions												
1.	<p>Construct the Routh array and determine the stability of the system whose characteristics equation is $s^4 + 8s^3 + 18s^2 + 16s + 5 = 0$. Also determine the number of roots lying on right half of S plane, left half of S plane and on imaginary axis.(13M) (Nov Dec 2018) Repeated question BTL 2</p> <p>Answer: Page 5.13 - A.Nagoor Kani</p> <p>The characteristics equation is $s^4 + 8s^3 + 18s^2 + 16s + 5 = 0$ The given characteristics equation is of 4th order hence it has 4 roots</p> <table style="margin-left: 20px;"> <tr> <td>s^4</td> <td>:</td> <td>1</td> <td>18</td> <td>5</td> <td>.... Row-1</td> </tr> <tr> <td>s^3</td> <td>:</td> <td>8</td> <td>16</td> <td></td> <td>.... Row-2</td> </tr> </table> <p>The elements of S3 row can be divided by 8 to simplify the computations.</p>	s^4	:	1	18	5 Row-1	s^3	:	8	16	 Row-2
s^4	:	1	18	5 Row-1								
s^3	:	8	16	 Row-2								

s^4 :	1	18	5 Row-1
s^3 :	1	2	 Row-2
s^2 :	16	5	 Row-3
s^1 :	1.7		 Row-4
s^0 :	5		 Row-5

↑
Column-1

The elements of the first column of Routh array, all the elements are positive and there is no sign change. All the roots are lying on left half of S plane and system is stable.

Construct the Routh array and determine the stability of the system whose characteristics equation is $s^6 + 2s^5 + 8s^4 + 12s^3 + 20s^2 + 16s + 16 = 0$. Also determine the number of roots lying on right half of S plane, left half of S plane and on imaginary axis. (13M) BTL2

Answer: Page 5.13 to 5.14 - A.Nagoor Kani

The characteristics equation is $s^6 + 2s^5 + 8s^4 + 12s^3 + 20s^2 + 16s + 16 = 0$

The given characteristics equation is of 6th order hence it has 6 roots.

s^6 :	1	8	20	16 Row-1
s^5 :	2	12	16	 Row-2

The elements of S5 row can be divided by 2 to simplify the computations.

2.

s^6 :	1	8	20	16 Row-1
s^5 :	1	6	8	 Row-2
s^4 :	1	6	8	 Row-4
s^3 :	0	0		 Row-4
s^3 :	1	3		 Row-4
s^2 :	3	8		 Row-5
s^1 :	0.33			 Row-6
s^0 :	8			 Row-7

↑
Column-1

On examining the 1st column of Routh array it is observed that there is no sign change. The rows with all zeros indicate the possibility of roots on imaginary axis. Hence, the system is limitedly or marginally stable.

The auxiliary polynomial is

$$s^4 + 6s^2 + 8 = 0$$

	<p>Let, $s^2 = x$</p> $\therefore x^2 + 6x + 8 = 0$ <p>The roots of quadratic are, $x = \frac{-6 \pm \sqrt{6^2 - 4 \times 8}}{2}$</p> $= -3 \pm 1 = -2 \text{ or } -4$ <p>The roots of auxiliary polynomial is,</p> $s = \pm \sqrt{x} = \pm \sqrt{-2} \text{ and } \pm \sqrt{-4}$ $= +j\sqrt{2}, -j\sqrt{2}, +j2 \text{ and } -j2$ <p>Four roots are lying on the imaginary axis and two roots are lying on the left half of s plane.</p>
3.	<p>A unity feedback control system has an open loop transfer function. sketch the root locus $G(s) = K / s(s^2 + 4s + 13)$ (13M) BTL3</p> <p>Answer: Page 5.71 to 5.74 - A.Nagoor Kani</p> <p>Step 1: Locate the poles and zeros of $G(s)H(s)$ on the s plane. The root locus branch starts from the open loop poles and terminates at zeros. (1M)</p> <ul style="list-style-type: none"> The poles are lying at $s=0, -2+j3, -2-j3$ <p>Step 2: Determine the root locus on real axis (1M)</p> <p>Step 3: Determine the asymptotes of root locus branches and meeting point of asymptotes with real axis and find the centroid (2M)</p> <ul style="list-style-type: none"> Angle of asymptotes = $\frac{\pm 180^\circ(2q+1)}{n-m}$; $q = 0, 1, 2, \dots, (n-m)$ <p>($\pm 60, \pm 180$)</p> <ul style="list-style-type: none"> Centroid = $\frac{\text{Sum of poles} - \text{Sum of zeros}}{n-m} = -1.33$ <p>Step 4: Find the breakaway and break-in points. (3M)</p> <ul style="list-style-type: none"> The root locus has neither breakaway nor break in points. <p>Step 5: If there is a complex pole then determine the angle of departure from the complex pole, If there is a complex zero then determine the angle of arrival at the complex zero (2M)</p> <ul style="list-style-type: none"> Angle of departure from the complex pole $P_2 = -33.7^\circ$ Angle of departure from complex pole $P_3 = +33.7^\circ$ Mark the angle of departure at complex poles using protractor. <p>Step 6: Find the points where the root loci may cross the imaginary axis. (2M)</p> <ul style="list-style-type: none"> The crossing point of root locus is The value of K at this crossing point is $K=52$.

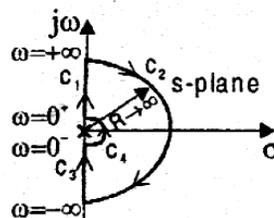
Step 7: Take a series of test points in the broad neighborhoods of the region of the S plane and adjust the test point to satisfy the angle criterion. Sketch the root locus by joining the test point by smooth curve. (2M)

Draw the Nyquist plot for the system whose open loop transfer function is given below. $G(s)H(s) = K / s(s+2)(s+10)$. Determine the range of K for which the closed loop system is stable.(13M) (April May 2015) Repeated question. BTL3

Answer: Page 5.36 to 5.39 - A.Nagoor Kani

$$G(s)H(s) = \frac{K}{s(s+2)(s+10)} = \frac{K}{s \times 2 \left(\frac{s}{2} + 1\right) \times 10 \left(\frac{s}{10} + 1\right)} = \frac{0.05K}{s(1+0.5s)(1+0.1s)}$$

Nyquist contour



The Nyquist contour has four sections C_1 , C_2 , C_3 and C_4 . The mapping of each section is performed separately and the overall Nyquist plot is obtained by combining the individual sections.

4. Mapping of Section C1:

In section C_1 , ω varies from 0 to +infinity.

Let $s = j\omega$

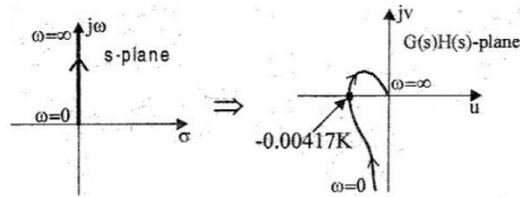
$$\begin{aligned} \therefore G(j\omega)H(j\omega) &= \frac{0.05K}{j\omega(1+j0.5\omega)(1+j0.1\omega)} \\ &= \frac{0.05K}{j\omega(1+j0.6\omega-0.05\omega^2)} = \frac{0.05K}{-0.6\omega^2 + j\omega(1-0.05\omega^2)} \end{aligned}$$

When the locus of $G(j\omega)H(j\omega)$ crosses real axis the imaginary term will be zero and the corresponding frequency is the phase cross over frequency ω_{pc} .

$$\therefore \text{At } \omega = \omega_{pc}, \quad \omega_{pc}(1-0.05\omega_{pc}^2) = 0 \Rightarrow 1-0.05\omega_{pc}^2 = 0 \Rightarrow \omega_{pc} = \sqrt{\frac{1}{0.05}} = 4.472 \text{ rad/sec}$$

$$\text{At } \omega = \omega_{pc} = 4.472 \text{ rad/sec}, \quad G(j\omega)H(j\omega) = \frac{0.05K}{-0.6\omega^2} = -\frac{0.05K}{0.6 \times (4.472)^2} = -0.00417K$$

The open loop is Type 1 and third order system. Hence the polar plot of $G(j\omega)H(j\omega)$ starts at -90° axis at infinity crosses real axis at $-0.00417K$ and ends at origin in second quadrant.



Mapping of Section C2:

(2M)

The mapping of section C2 from S plane to G(s)H(s) plane is obtained by letting $s = \lim_{R \rightarrow \infty} Lt R e^{j\theta}$ in G(s)H(s) and varying θ from $+\pi/2$ to $-\pi/2$. Since $s \rightarrow R e^{j\theta}$ and $R \rightarrow \infty$, the G(s)H(s) can be approximated. [i.e., $(1+sT) \approx sT$].

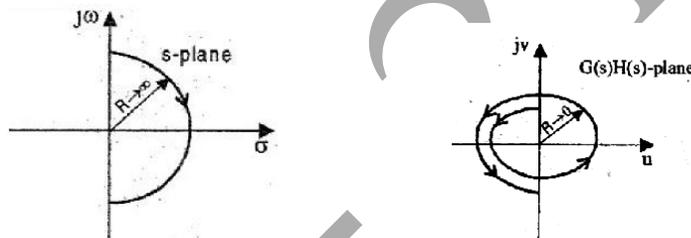
$$G(s) H(s) = \frac{0.05K}{s(1+0.5s)(1+0.1s)} \approx \frac{0.05K}{s \times 0.5s \times 0.1s} = \frac{K}{s^3}$$

Let, $s = \lim_{R \rightarrow \infty} Lt R e^{j\theta}$.

$$\therefore G(s)H(s) \Big|_{s = \lim_{R \rightarrow \infty} Lt R e^{j\theta}} = \frac{K}{s^3} \Big|_{s = \lim_{R \rightarrow \infty} Lt R e^{j\theta}} = \frac{K}{\lim_{R \rightarrow \infty} Lt (R e^{j\theta})^3} = 0e^{-j3\theta}$$

When $\theta = \frac{\pi}{2}$, $G(s)H(s) = 0e^{-j\frac{3\pi}{2}}$

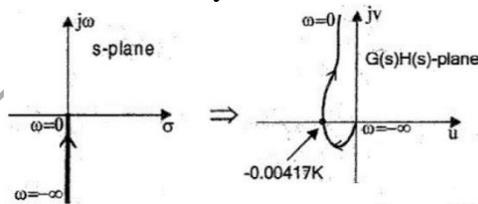
When $\theta = -\frac{\pi}{2}$, $G(s)H(s) = 0e^{+j\frac{3\pi}{2}}$



Mapping of section C3:

(2M)

In section C3, ω varies from $-\infty$ to 0. The mapping of section C3 is given by the locus of $G(j\omega)H(j\omega)$ as ω is varied from $-\infty$ to 0.



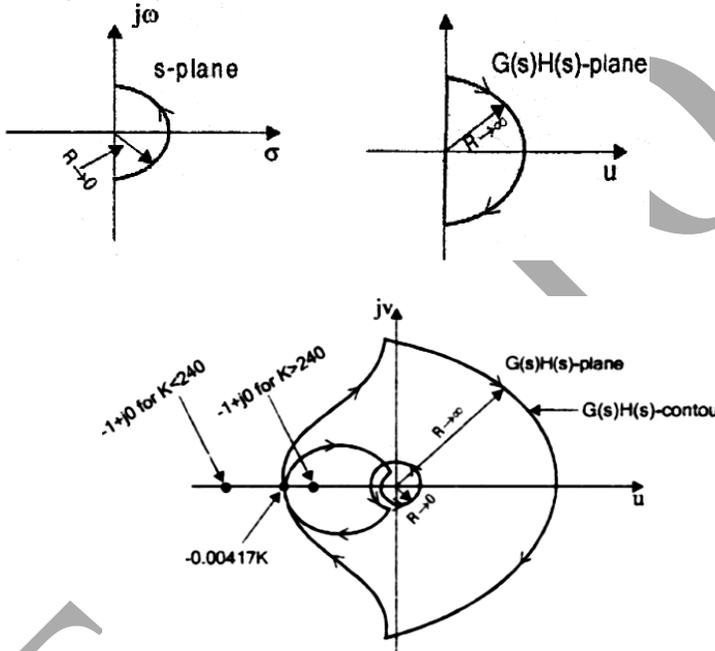
Mapping of section C4

(3M)

The mapping of section C4 from S plane to G(s)H(s) plane is obtained by letting

$s = \lim_{R \rightarrow 0} Lt R e^{j\theta}$ in obtained by letting $s = \lim_{R \rightarrow 0} Lt R e^{j\theta}$

[i.e., $(1+sT) \approx 1$].

	$G(s)H(s) = \frac{0.05K}{s(1+0.5s)(1+0.1s)} \approx \frac{0.05K}{s \times 1 \times 1} = \frac{0.05K}{s}$ <p>Let $s = \lim_{R \rightarrow 0} R e^{j\theta}$.</p> $\therefore G(s)H(s) \Big _{s = \lim_{R \rightarrow 0} R e^{j\theta}} = \frac{0.05K}{s} \Big _{s = \lim_{R \rightarrow 0} R e^{j\theta}} = \frac{0.05K}{\lim_{R \rightarrow 0} (R e^{j\theta})} = \infty e^{-j\theta}$ <p>When $\theta = -\frac{\pi}{2}$, $G(s)H(s) = \infty e^{+j\frac{\pi}{2}}$</p> <p>When $\theta = \frac{\pi}{2}$, $G(s)H(s) = \infty e^{-j\frac{\pi}{2}}$</p>  <p>Limiting value of K is 240 (2M)</p>
PART * C	
Q.No	Questions
1.	<p>Explain briefly about the steps to be followed to construct a root locus plot of a given transfer function(15M) (Nov Dec 2016, April May 2017) Repeated question BTL2</p> <p>Answer: Page 5.67 to 5.71 - A.Nagoor Kani</p> <p>Step 1: Locate the poles and zeros of G(s)H(s) on the s plane. The root locus branch starts from the open loop poles and terminates at zeros</p> <p>Step 2: Determine the root locus on real axis</p> <p>Step 3: Determine the asymptotes of root locus branches and meeting point of asymptotes with real axis</p> <p>Step 4: Find the breakaway and break-in points.</p> <p>Step 5: If there is a complex pole then determine the angle of departure from the complex pole, If there is a complex zero then determine the angle of arrival at the complex zero</p>

	<p>Step 6: Find the points where the root loci may cross the imaginary axis.</p> <p>Step 7: Take a series of test points in the broad neighborhoods of the region of the S plane and adjust the test point to satisfy the angle criterion. Sketch the root locus by joining the test point by smooth curve.</p> <p>Step 8: The value of gain K at any point on the locus can be determined from the magnitude condition. The value of K at a point $S = S_a$ is given by</p> $K = \frac{\text{Product of length of vector from open loop poles to the point } S_a}{\text{Product of length of vector from open loop zeros to the point } S_a}$
2.	<p>State Nyquist stability criterion and explain the three situations while examining the stability of the linear control system (15M) (Nov Dec 2016) BTL2</p> <p>Answer: Page 5.30 to 5.5.33 - A.Nagoor Kani</p> <p>Nyquist stability criterion: (5M)</p> <ul style="list-style-type: none"> • The Nyquist stability criterion is similar to the Bode criterion in that it determines closed-loop stability from the open-loop frequency response characteristics. • The Nyquist stability criterion is based on two concepts from complex variable theory, <i>contour mapping</i> and the <i>Principle of the Argument</i>. • Nyquist Stability Criterion. Consider an open-loop transfer function $GOL(s)$ that is proper and has no unstable pole-zero cancellations. Let N be the number of times that the Nyquist plot for $GOL(s)$ encircles the -1 point in the clockwise direction. Also let P denote the number of poles of $GOL(s)$ that lie to the right of the imaginary axis. Then, $Z = N + P$ where Z is the number of roots of the characteristic equation that lie to the right of the imaginary axis (that is, its number of "zeros"). The closed-loop system is stable if and only if $Z = 0$. <p>Examining the stability of the linear control system: (10M)</p> <p>No encirclement of -1+j0 point: This implies that the system is stable if there are no poles of $G(s)H(s)$ in the right half of S plane. If there are poles on right half of S plane then the system is unstable</p> <p>Anticlockwise encirclement of -1+j0 point: In this case the system is stable if the number of anticlockwise is same as the number of poles of $G(S)H(S)$ in the right half of S plane. If the number of anticlockwise encirclement is not equal to number of poles on right half of S plane then the system is unstable.</p> <p>Clockwise encirclement of the -1+j0 point: In this case the system is always unstable. Also in this case if no poles of $G(s)H(s)$ in right half of S plane, then the number of clockwise encirclement is equal to number of poles of closed loop system on right half of S plane.</p>
3.	<p>Define stability .With an example explain the steps to be followed for Routh Hurwitz criterion (15M) (Nov Dec 2017) Repeated question BTL1</p>

Answer: Page 5.1 to 5.9 - A.Nagoor Kani**Stability**

(3M)

- The term STABILITY refers to the stable working condition of a control system
- The response or output is predictable ,finite and stable for a given input (for any changes in system parameters)
- A system is STABLE if its output is bounded for any bounded input
- If a system output is stable for all variations of its parameters, then the system is called ABSOLUTELY STABLE system
- If a system output is stable for a limited range of variations of its parameters then the system is called CODITIONALLY STABLE system.

Routh Hurwitz criterion

(6M)

- The Routh stability criterion is based on ordering the coefficients of the characteristics equation into a schedule called the Routh array.
- The Routh stability can be stated as follows”The necessary and sufficient condition for stability is that all of the elements in the first column of the routh array be positive.If this condition is not met the system is unstable and the number of sign changes in the elements of the first column of the routh array corresponds to the number of roots of the characteristics equation in the right half of S plane.”

Construction of Routh array

(6M)

- Let the characteristics polynomial

$$a_0s^n + a_1s^{n-1} + a_2s^{n-2} + a_3s^{n-3} + \dots + a_{n-1}s^1 + a_n s^0$$

- The coefficients of the polynomial are arranged in two rows as below

$$s^n : a_0 \quad a_2 \quad a_4 \quad a_6 \quad \dots$$

$$s^{n-1} : a_1 \quad a_3 \quad a_5 \quad a_7 \quad \dots$$

- When n is even ,Sⁿ row is formed by the coefficients of even order terms and row is formed by coefficients of odd order terms
- When n is odd , Sⁿ row is formed by the coefficients of odd order terms and row is formed by coefficients of even order terms

The other rows of Routh array upto S⁰ can be formed by the following procedure.

$$s^{n-x} : x_0 \quad x_1 \quad x_2 \quad x_3 \quad x_4 \quad x_5 \dots$$

$$s^{n-x-1} : y_0 \quad y_1 \quad y_2 \quad y_3 \quad y_4 \quad y_5 \dots$$

$$s^{n-x-2} : z_0 \quad z_1 \quad z_2 \quad z_3 \quad z_4 \quad \dots$$

- The elements of S^{n-x-2} row are given by

$$z_0 = \frac{(-1) \begin{vmatrix} x_0 & x_1 \\ y_0 & y_1 \end{vmatrix}}{y_0} = \frac{y_0 x_1 - y_1 x_0}{y_0}$$

$$z_2 = \frac{(-1) \begin{vmatrix} x_0 & x_3 \\ y_0 & y_3 \end{vmatrix}}{y_0} = \frac{y_0 x_3 - y_3 x_0}{y_0}$$

$$z_1 = \frac{(-1) \begin{vmatrix} x_0 & x_2 \\ y_0 & y_2 \end{vmatrix}}{y_0} = \frac{y_0 x_2 - y_2 x_0}{y_0}$$

$$z_3 = \frac{(-1) \begin{vmatrix} x_0 & x_4 \\ y_0 & y_4 \end{vmatrix}}{y_0} = \frac{y_0 x_4 - y_4 x_0}{y_0}$$

- All the elements of any row can be multiplied or divided by a positive constant to simplify the computational work

In the construction of routh array one may come across the following three cases

	<ul style="list-style-type: none">• Case (i) Normal Routh array (Non-zero elements in the first column of routh array)• Case (ii) A row of all zeros• Case(iii) First elements of a row is zero but same or other elements are not zero
--	---

JIT - 2106

UNIT V CONTROL SYSTEM ANALYSIS USING STATE VARIABLE METHODS	
	State variable representation-Conversion of state variable models to transfer functions-Conversion of transfer functions to state variable models-Solution of state equations-Concepts of Controllability and Observability-Stability of linear systems-Equivalence between transfer function and state variable representations-State variable analysis of digital control system-Digital control design using state feedback.
	PART * A
Q.No	Questions
1.	<p>What are the advantages of state space analysis? BTL2</p> <ul style="list-style-type: none"> • State space analysis is applicable to any type of systems. They can be used for modeling and analysis of linear & nonlinear system, time variant & time invariant systems and multiple input and multiple output systems • The state space analysis can be performed with initial conditions. • The variables used to represent the system can be any variables in the system • Using this analysis, the internal states of the system at any instant can be predicted.
2.	<p>What are the drawbacks of transfer function analysis? BTL2</p> <ul style="list-style-type: none"> • Transfer function is defined under zero initial conditions. • Transfer function is applicable to linear time invariant systems. • Transfer function analysis is restricted to single input and single output systems. • The transfer function modeling is a terminal approach where we can find only the output and not the state of the other variables inside the system.
3.	<p>What is state and state variable?(April May 2016) BTL1</p> <p>State: It is a group of variables, which summarizes the history of the system in order to predict the future values (outputs).</p> <p>State Variable: The number of the state variables required is equal to the number of the storage elements present in the system.</p>
4.	<p>What is state vector? BTL1</p> <p>It is a vector, which contains the state variables as elements.</p>
5.	<p>Write the state model for nth order system(Nov Dec 2017) BTL1</p> <p>The most general state-space representation of a linear system with m inputs, p outputs and n state variables are written in the following form:</p> $\dot{X} = AX + BU$ $Y = CX + DU$ <p>Where X= state vector of order n X₁.</p> <p>U = input vector of order n X₁.</p> <p>A=System matrix of order n X_n.</p> <p>B=Input matrix of order n X_m</p> <p>C =output matrix of order p X_n</p> <p>D = transmission matrix of order p X_m.</p>
6.	<p>What is state space? BTL1</p> <p>The set of all possible values which the state vector x(t) can have at time t forms the state space of the system</p>
7.	<p>Define observability of the system.(April May 2015) BTL1</p>

	A control system is said to be observable if it is able to determine the initial states of the control system by observing the outputs in finite duration of time. We can check the observability of a control system by using Kaman's test.
8.	What is state transition matrix and how it is related to state of the system? BTL1 The matrix exponential e^{AT} is called state transition matrix. In the expanded form $e^{AT} = 1 + At + \frac{1}{2!} A^2 t^2 + \frac{1}{3!} A^3 t^3 + \dots + \frac{1}{i!} A^i t^i$
9.	List the main properties of state transition matrix (Nov Dec 2016) BTL2 1. $\Phi(0) = I$ 2. $\Phi^{-1}(t) = \Phi(-t)$ 3. $x(0) = \Phi(-t)x(t)$ 4. $\Phi(t_2 - t_1)\Phi(t_1 - t_0) = \Phi(t_2 - t_0)$ 5. $\Phi(t)^k = \Phi(kt)$
10.	What are phase variables? BTL1 The phase variables are defined as the state variables which are obtained from one of the system variables and its derivatives.
11.	What is observability? BTL1 A system is said to be completely observable if every state $X(t)$ can be completely identified by measurements of the output $Y(t)$ over a finite time interval.
12.	What is the necessary condition to be satisfied for design using state feedback? BTL1 The state feedback design requires arbitrary pole placements to achieve the desired performance. The necessary and enough condition to be satisfied for arbitrary pole placement is that the system is completely state controllable.
13.	What is the need for controllability test? BTL2 The controllability test is necessary to find the usefulness of a state variable. If the state variables are controllable then by controlling (i.e. varying) the state variables the desired outputs of the system are achieved.
14.	What is the need for observability test? BTL2 The observability test is necessary to find whether the state variables are measurable or not. If the state variables are measurable then the state of the system can be determined by practical measurements of the state variables.
15.	State the condition for controllability by Gilbert's method. BTL2 Case (i) when the Eigen values are distinct Consider the canonical form of state model shown below which is obtained by using the transformation $X=MZ$. $\dot{X} = \Lambda Z + U$ $Y = Z + DU$ Where, $\Lambda = M^{-1}AM$; $C = CM$, $B = M^{-1}B$ and $M =$ Modal matrix. In this case the necessary and enough condition for complete controllability is that, the matrix must have no row with all zeros. If any row of the matrix is zero, then the corresponding state variable is uncontrollable. Case (ii) when Eigen values have multiplicity In this case the state modal can be converted to Jordan canonical form shown below: $Z = JZ + U$

	<p>$Y=Z + DU$ Where, $J = M-1AM$</p> <p>In this case the system is completely controllable, if the elements of any row of that correspond to the last row of each Jordan block are not all zero.</p>
16.	<p>State the condition for observability by Gilbert's method. BTL2</p> <p>Consider the transformed canonical or Jordan canonical form of the state model shown below:</p> <p>which is obtained by using the transformation, $X =MZ$</p> <p>$Z= \Lambda Z + U$</p> <p>$Y=Z + DU$ (Or)</p> <p>$Z= JZ + U$</p> <p>$Y=Z + DU$ where $=CM$ and M=modal matrix.</p> <p>The necessary and enough condition for complete observability is that none of the columns of the matrix be zero. If any of the column has all zeros, then the corresponding state variable is not observable.</p>
17.	<p>State the duality between controllability and observability. BTL2</p> <p>The concept of controllability and observability are dual concepts and it is proposed by Kalman as principle of duality. The principle of duality states that a system is completely state controllable if and only if its dual system is completely state controllable if and only if its dual system is observable or vice versa.</p>
18.	<p>What is state diagram? Draw the block diagram representation of state model. BTL3</p> <p>The pictorial representation of the state model of the system is called state diagram. The state diagram of the system can be either in block diagram or in signal flow graph form.</p>
19.	<p>What are the basic elements used to construct the state diagram. BTL2</p> <p>The basic elements used to construct the state diagram are scalar, adder, and Integrator.</p>
20.	<p>Sketch the basic elements used to construct the block diagram of a state model. BTL2</p> <p>The basic elements used to construct the state diagram are scalar, adder, and Integrator.</p>
21.	<p>What are phase variable?1</p> <p>The phase variables defined as those particular state variables, which are obtained from one of the system variables and its derivatives. Usually the variables used are the system output and the remaining state variables are then derivatives of the output.</p>
22.	<p>What are the advantages of state space modeling using phase variable? BTL2</p> <ul style="list-style-type: none"> • The state variable can be utilized for the purpose of feedback • The implementation of design with state variable feedback becomes straight forward • The solution of state equation gives time variation of variables, which have direct relevance to the physical system.
23.	<p>What are the disadvantages in choosing phase variable for state space modelling? BTL2</p> <p>The disadvantage in choosing phase variable is that the phase variables are not physical variables of the system and therefore are not available for measurement and control</p>

	purposes
24.	What is the advantage and the disadvantage in canonical form of state model? BTL2 The advantages of canonical form are that the state equations are independent of each other. The disadvantage is that the canonical variables are not physical variables and so they are not available for measurement and control.
25.	What is the solution of homogeneous state equation? BTL1 The solution of homogeneous state equation is $X(t)=e^{At}X_0$
26.	What is Jordan canonical form? BTL1 When the eigen values have multiplicity the system matrix cannot be diagonalized. But the transformation $X=MZ$ will transform the system matrix to a form called Jordan matrix. Where $J=M^{-1}AM$. The transformed state model in this case is called Jordan canonical form.
PART * B	
Q.No	Questions
1.	<p>Construct the state model for a system characterized by the differential equation $d^3y/dt^3+6d^2y/dt^2+11dy/dt+6y+u=0$. Give the block diagram representation of the state model. (13M)BTL6</p> <p>Answer: Page 7.26 - A.Nagoor Kani</p> <ul style="list-style-type: none"> • Convert differential equations in to dot variables (2M) $x_1 = y$ $x_2 = \frac{dy}{dt} = \dot{x}_1 \quad x_2 = \frac{d^2y}{dt^2} = \dot{x}_2$ • Apply the state variables to dot variables (2M) 1. $\dot{x}_1 = x_2$ 2. $\dot{x}_2 = x_3$ 3. $\dot{x}_3 = -6x_1 - 11x_2 - 6x_3 - u$ • Rearrange the equation and derive state model (3M) • Draw the block diagram for state equation and output equation (6M)
2.	<p>Obtain the state model of the system whose open loop transfer function is given as, $Y(s)/U(s)=10/s^3+4s^2+2s+1$. (13M)BTL6</p> <p>Answer: Page 7.29 to 7.30 - A.Nagoor Kani</p> <ul style="list-style-type: none"> • Use inspection, cascade, signal flow graph method (1M) • Take inverse Laplace transform & Convert differential equations in to dot variables (2M) • Apply the state variables to dot variables (2M) • Rearrange the equation and derive state model (3M) • Draw the block diagram for state equation and output equation (5M)
3.	A feedback system has a closed loop transfer function $Y(s)/U(s) = 10(s+4)/s(s+1)(s+3)$, construct block diagram representation of each state model. (13M)BTL6

	<p>Answer: Page 7.33 to 7.36 - A.Nagoor Kani</p> <ul style="list-style-type: none"> • Use inspection, cascade, signal flow graph method (1M) • Take inverse Laplace transform & Convert differential equations into dot variables (2M) • Apply the state variables to dot variables (2M) • Rearrange the equation and derive state model (3M) • Draw the block diagram for state equation and output equation (5M).
4.	<p>Determine the canonical state model of the system, whose transfer function is $T(s) = \frac{2(s+5)}{(s+1)(s+3)(s+4)}$. (13M)BTL6</p> <p>Answer: Page 7.36 to 7.37 - A.Nagoor Kani</p> <ul style="list-style-type: none"> • Use inspection, cascade, signal flow graph method (1M) • Take inverse Laplace transform & Convert differential equations in to dot variables (2M) • Apply the state variables to dot variables (2M) • Rearrange the equation and derive state model (3M) • Draw the block diagram for state equation and output equation (5M)
5.	<p>Compute state transition matrix $A = \begin{bmatrix} 0 & -1 \\ -2 & -3 \end{bmatrix}$ (13M) BTL6</p> <p>Answer: Page 7.42 to 7.44 - A.Nagoor Kani</p> <ul style="list-style-type: none"> • Find eigen values by using $SI - A = 0$ (4M) • Find inverse matrix of $SI - A$ (4M) • Use partial fraction method to find A, B, C (2M) • Find inverse Laplace of $\phi(s)$ to get $\phi(t)$ (3M)
6.	<p>Test the controllability and observability by using any one method of the given state space representation model. (13M)BTL4</p> $\begin{bmatrix} \dot{x}_1 \\ \dot{x}_2 \\ \dot{x}_3 \end{bmatrix} = \begin{bmatrix} 0 & 0 & 1 \\ -2 & -3 & 0 \\ 0 & 2 & -3 \end{bmatrix} \begin{bmatrix} x_1 \\ x_2 \\ x_3 \end{bmatrix} + \begin{bmatrix} 0 \\ 2 \\ 0 \end{bmatrix} u; y = [1 \ 0 \ 0] \begin{bmatrix} x_1 \\ x_2 \\ x_3 \end{bmatrix}$ <p>Answer: Page 7.61 to 7.65- A.Nagoor Kani</p>

	<ul style="list-style-type: none"> From the state model identify A, B, C Matrix (2M) Use Gilberts method or Kalman's method (2M) In Gilberts method Find \dot{B} and C. The value of \dot{B} does not contain zero value then the system is completely controllable. The value of C does not contain zero value then the system is completely observable. (5M) In Kalman's method Find Q_0 and Q_c. The value of Q_0 does not contain zero value then the system is completely controllable. The value of Q_0 does not contain zero value then the system is completely observable. (4M)
	PART * C
Q.No	Questions
1.	<p>Test the controllability of the following state model by using both the methods. (15M) BTL4</p> $\begin{bmatrix} \dot{x}_1 \\ \dot{x}_2 \\ \dot{x}_3 \end{bmatrix} = \begin{bmatrix} 0 & 0 & 1 \\ -2 & -3 & 0 \\ 0 & +2 & -3 \end{bmatrix} \begin{bmatrix} x_1 \\ x_2 \\ x_3 \end{bmatrix} + \begin{bmatrix} 0 \\ 2 \\ 0 \end{bmatrix} u; y = [1 \ 0 \ 0] \begin{bmatrix} x_1 \\ x_2 \\ x_3 \end{bmatrix}.$ <p>Answer: Page 7.57 to 7.61- A.Nagoor Kani</p> <ul style="list-style-type: none"> From the state model identify A, B, C Matrix (2M) Use Gilberts method or Kalman's method (2M) In Gilberts method Find \dot{B} and C. The value of \dot{B} does not contain zero value then the system is completely controllable. The value of C does not contain zero value then the system is completely observable. (6M) In Kalman's method Find Q_0 and Q_c. The value of Q_0 does not contain zero value then the system is completely controllable. The value of Q_0 does not contain zero value then the system is completely observable. (5M) The system is completely observable.
2.	<p>Verify the system is completely controllable and observable.(15M) BTL4</p> $\dot{x}(t) = \begin{bmatrix} 0 & 0 & 1 \\ -2 & -3 & 0 \\ 0 & 2 & -3 \end{bmatrix} \begin{bmatrix} x_1(t) \\ x_2(t) \\ x_3(t) \end{bmatrix} + \begin{bmatrix} 0 \\ 2 \\ 0 \end{bmatrix} u(t); y(t) = [1 \ 0 \ 0] \begin{bmatrix} x_1(t) \\ x_2(t) \\ x_3(t) \end{bmatrix}.$ <p>Answer: Page 7.57 to 7.61- A.Nagoor Kani</p> <ul style="list-style-type: none"> From the state model identify A, B, C Matrix (2M) Use Gilberts method or Kalman's method (2M) In Gilberts method Find \dot{B} and C. The value of \dot{B} does not contain zero value then the system is completely controllable. The value of C does not contain zero value

	<p>then the system is completely observable. (6M)</p> <ul style="list-style-type: none">• In Kalman's method Find Q_0 and Q_c. The value of Q_0 does not contain zero value then the system is completely controllable. The value of Q_0 does not contain zero value then the system is completely observable. (5M)
--	---

JIT - 2106